A HIGH POWER WIDE BANDWIDTH SWITCHMODE AMPLIFIER

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A HIGH POWER WIDE BANDWIDTH SWITCH MODE AMPLIFIER

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A HIGH POWER WIDE BANDWIDTH SWITCH MODE AMPLIFIER.

ABSTRACT: This thesis describes the development of a 45kVA, 20kHz bandwidth switching amplifier. The amplifier is a subsection of a controlled source audiomagnetelluric (AMT) system primarily aimed at exploration of mineral deposits and geophysical deposits associated with oil and gas fields. However this amplifier has applications in many other areas.

A number of design innovations contributing to the body of knowledge in power electronics were implemented in the course of the development of the AMT amplifier. In particular, a new bridge inverter topology has been developed which supports five level pulsewidth modulation with only four switches. In the past eight switches have been required to achieve the same result. The five level modulation has allowed extension of the bandwidth and improvement in the output quality of the amplifier without increase in the switch frequency.

The new bridge topology consists of four buck converter sub units coupled by transformers. The buck converters supply a maximum current of 100A from a 560V nominal bus and switch at 50kHz. Each buck converter employs an Insulated Gate Bipolar Transistor and high speed power diodes together with a regenerative snubbing and clamp system to achieve this high power frequency product. New techniques have been developed to accurately predict diode reverse recovery performance during of the buck converter design process.

The new converter topology requires a specialised control system. The design of this control system, as well as important design rules developed during the project, are presented.

Computer simulation studies have been extensively used in the design of both the buck converters and the control system. This design approach has resulted in a significant reduction in time consuming prototype modifications.

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ACKNOWLEDGEMENTS

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DECLARATION

The work contained in this thesis has not been previously submitted for a degree or diploma at any tertiary education institution. To the best of my knowledge this thesis contains no material previously published by another person except where due reference is made.

Signature Redacted

Frank Flinders.

PUBLICATIONS

The following publications have been produced during the course of this thesis

(i) P.J.Wolfs, F.M.Flinders, "An Improved Phase Leg", Australian Provisional Patent Specification No PK7430, 26th July 1991.

(ii) F.M. Flinders, P.J.Wolfs and K.Kwong, "An Improved Modulation Capability Inverter", Conference on Industrial Drives, University of Central Queensland, 18th–20th September 1991, pp 273–277.

(iii) F.M. Flinders, P.J.Wolfs and K.Kwong, "Prediction of Diode Reverse Recovery from Limited Data", AUPCEC 1992 Conference, Queensland University of Technology, 1st–2nd October 1992, pp 414–419.

(iv) F.M. Flinders, P.J. Wolfs, K.Kwong, "Improved techniques for Switching Power Amplifiers", James Goldstone School of Engineering Research Report Series, No. EE5, June 1992.

(v) F.M. Flinders, P.J. Wolfs, "A Charge Control Equation Based Method for Predicting Power Diode Reverse Recovery Behaviour", James Goldstone School of Engineering Research Report Series, No. EE6, August 1992.

Additionally the following paper has been accepted for publication in the IEEE Transactions on Power Electronics.

(vi) F.M.Flinders, P.J.Wolfs, K.Kwong, "Improved Techniques for Switching Amplifiers", IEEE Transactions on Power Electronics, Log No. #C182–HP–21, April 1992, accepted January 1993.

1. INTRODUCTION

This thesis covers the development of a 45kVA, 0–20kHz audio frequency switching amplifier. The project was supported by part of a NERDEC grant made to the University of Queensland for the development of a controlled source audiomagnetelluric, (CSAMT), system for geophysical exploration. The system is primarily targeted at economically exploitable mineral deposits and geophysical deposits associated with oil and gas fields, [1]. In the audiomagnetelluric system the region of earth of interest is illuminated using an artificial electromagnetic source. The surface electric and magnetic fields are measured at a distance in three orthogonal directions and the results recorded as impedances. The variation of input impedance with frequency is then used to construct a model for the depth resistivity structure. The nature of the underlying mineral deposits can be interpreted from this data.

The amplifier forms the artificial source in the system. The output current from the amplifier can be passed directly through the earth via two stakes. Alteratively the source can be coupled via a large diameter magnetic loop laid over the ground. The 45kVA switching amplifier is at present being constructed at the University of Central Queensland.

Although this amplifier was developed for a specific task its application is more broad ranging. Because the output waveform is of high quality up to a frequency of 10kHz it would be suitable as a modulator for shortwave and medium wave AM radio transmitters. Another important application is a source for driving electromagnetically driven shakers and vibrating tables. Because the output distortion is low the unit would also be ideal as a high power bass amplifier. It is also likely that the amplifier would be useful as standard equipment in scientific laboratories for conducting various physical experiments, [2].

In addition to the many applications for this amplifier there has also been several innovative techniques developed which will contribute to improvement of technology in other areas. The power circuit topology uses only four switches to provide five level modulation capability. Previously this could only be obtained with the use of eight switches requiring either two standard single phase bridges or the neutral point clamped, (NPC), configuration, [2–5]. Within the new topology greater utilisation of each switch is achieved by the use of a coupling transformer in each phase leg. The power circuit consists of four independent buck converters. This new topology is believed to be a new concept and is the subject of a patent application, [6]. The topology could be employed in three phase variable speed motor drives. By appropriate phase shifting of the modulation carriers the switch frequency component can be eliminated from the output spectrum, [7]. This could be of great importance in multi–megawatt drives where switching frequencies are normally less than 500Hz. Another very significant advantage of the new topology is that the shoot through fault which can occur in standard phase legs is eliminated. The coupling transformer together with the control system prevents any uncontrolled shoot through current from occurring. This will prove to be a very large benefit in the high power motor drive area.

In 1987 a 15kVA amplifier was developed for the same application by the University of Queenslands Physics Department, [1]. It was based upon a pulsewidth modulated bridge inverter supplied from a 560Vdc nominal bus. The inverter switching elements operated at a frequency of 20kHz. A uni–polar pulsewidth modulation scheme was adopted. This produces three distinct output levels and an effective output switching frequency of 40kHz. After extensive field testing this amplifier was shown to be deficient in several areas for the CSAMT application. The output current available proved inadequate in some situations. The need existed to increase the rating from 15kVA to 45kVA. Although the amplifier was capable of reproducing signals up to 10kHz the waveform quality and control performance was poor.

Only low open loop gains are possible near 10kHz. At higher gains the 40 kHz output switching frequency ripple component caused erratic behavior of the modulator. An open loop bandwidth of 20kHz would be necessary to obtain adequate control loop performance at 10kHz.

To obtain the performance levels desired the second generation amplifier would require a substantial increase in the power frequency product over the original unit. Meanwhile, semiconductor technology has advanced considerably over the last five years. However, analysis showed that the increased performance of the semiconductor devices alone could not provide the required power frequency product. This lead to the development of a new inverter topology. This new topology allows a five level modulation strategy to be implemented, extending the maximum bandwidth and reducing the output peak to peak ripple current amplitude. The output ripple frequency becomes four times the device switching frequency.

With the new topology a device switching frequency of 50kHz was required to obtain the necessary control bandwidth. The power devices used were 200A 1200V Insulated Gate Bipolar Transistors (IGBT's), [8]. These devices represent state of the art power switching semiconductor technology at the time of the project. However at a switch frequency of 50kHz, snubbing to reduce switching power loss, was a necessity.

The snubbing system chosen is an innovative combination of several published techniques, [9],[10–14]. Each buck converter has a self contained snubbing system. The design of this buck converter with snubbing system to obtain optimum overall results is a complex task, [15], requiring a number of iterative steps. Factors such as overall power loss, individual device power loss, device temperature rise, device maximum current/voltage stress and circuit complexity must all be considered. High power converters require considerable effort at the design stage.

Design errors in high power converters, unlike low power converters, are expensive to correct. Extensive use of the software package PSPICE, [16], was made to verify device current and voltage stresses prior to construction of the prototype. Very few problems were encountered in the full scale buck converter prototype.

The content of each chapter will now be described briefly.

Chapter Two of this report focuses on the new converter topology. It begins by reviewing conventional techniques used to construct switching amplifiers, [17],[1–2]. The suitability of each for this application is discussed. A detailed comparison of two, three and five level modulation schemes is presented. A TUTSIM simulation of a five level scheme was conducted to obtain the voltage and current output spectrum, [18]. The simulation shows that components at the switch frequency and two times the switch frequency can be eliminated. Spectral components are found to be centered around a 200kHz suppressed carrier at intervals of the modulation frequency for a 50kHz switch frequency. The operation of the new converter topology offering the capability of five level modulation is discussed in detail. Important converter design rules such as those relating to the coupling transformers are developed.

Because this converter is new, a new set of control strategies need to be developed. To maintain the five level modulation properly all buck converters must always remain in conduction. In addition to regulating the output current the controller must maintain conduction in all buck converters. Each buck converter consists of the main switching device and freewheel diode assembly plus associated snubbers. Because of the converter's high power rating and high operating frequency the snubbers are a significant system component. The buck converter employs both resonant reversing lossless snubbers and a voltage clamping system for the IGBT. The clamping system uses a pair of 500watt self oscillating inverters, (SOI's), to return energy to the dc supply.

The choice of topology and operation of the Buck converters is thoroughly discussed and includes a set of typical system waveforms.

The third chapter presents a detailed study of the power semiconductors employed in the converter. A full understanding of the semiconductor device characteristics is fundamental to a good converter design. While it is possible to design and develop low power converters with little knowledge of semiconductor properties, this luxury can not be afforded at high powers and high switch frequencies. In large converters semiconductor performance dictates physical construction and layout. Therefore modifications due to unexpected variations in semiconductor performance are not easily accommodated in the prototyping stage. The key to a successful design is an accurate assessment of semiconductor performance in the design stage.

The converter uses a large number of high current high speed diodes. Because of the high switching frequency these diodes must have good reverse recovery characteristics. Where possible it was decided to standardise on one type of diode. After an extensive review of the latest manufacturers' data books the diode chosen was a 1000V 60A (DSE1–60–10A) device which was a new release by ABB–IXYS, [19–22]. The reverse recovery data indicated that this diode was significantly better than any similar rated device that was reviewed. However only data for one operating condition was available. The four major parameters that affect the reverse recovery performance are the forward current prior to commutation, the commutation dI/dt, junction temperature, and minority carrier life time. While the former three are essentially a function of the converter design the latter is a characteristic of the diode. In this case a reverse maximum current of 32A was specified for a forward current of 60A, commutation dI/dt of 480A/μS and a junction temperature of 100°C. To be able to accurately design the converter it was necessary to know the reverse recovery current at significantly different operating conditions to those given.

Thus, it was considered essential that an accurate method of determining diode reverse recovery current be found. Review of the literature indicated that the most common method of approaching this problem was by formulation of models and subsequent simulation, [23–26]. While this yields good simulation results it is not a closed solution and thus inadequate for the design purpose. As part of this thesis relationships for the reverse maximum current are derived. The relationships are based on the charge control model of the P–N junction, [27–29]. Implicit equations that allow the calculation of the minority carrier lifetime from manufacturers data and then use this parameter to determine the reverse maximum current at other operating points have been developed. These equations are presented graphically and in lookup table form. When applied to diodes with comprehensive data a good match between predicted and actual characteristics has been found. The procedure though based on well known theory is presented in a unique and efficacious form for use in general power electronics design. The calculation of the minority carrier lifetime also allows an unbiased comparison of diode reverse recovery performance between devices from competing manufacturers. This new technique is believed to be a valuable tool to the power electronics designer, [30].

Another diode characteristic which is less widely documented but is of significant importance in large high frequency converters is transient forward recovery, [24,29,31]. In this case at high application rates of forward current the forward voltage exceeds its normal steady state level. In some cases the transient voltage may be greater than 50V. Because this overshoot voltage normally causes stress on other semiconductor devices it becomes an important design consideration. Section 3.3 is devoted to the discussion of the forward recovery process, its effect and estimation in various sections of the converter. The main switching device in the power circuit is a Toshiba MG200Q1US1 IGBT, [8]. Sections 3.5, 3.6 and 3.7 are devoted to a discussion of its characteristics, and method of calculation of its power loss.

Chapter Four gives a detailed description of the power circuit design, which is a long iterative task because of the complex interdependence of component values. Rather than presenting the full design process the selected values for the major components are presented and the choice in terms of worst case junction temperature, current stress or voltage stress is verified. The selection of each major component in each module is examined. Throughout the design extensive use is made of the results from Chapter Three with respect to diode reverse recovery. Two important components are the main snubber capacitor ,C_s ,and the dI/dt limiting inductor, L_f. These two components to a large extent govern the design of most of the remainder of the converter. Their selection is a complex task involving many variables with many iterative steps. In particular, the following factors must be considered: Main and auxiliary semiconductor device power loss, current stress and voltage stress; overall power loss and converter efficiency; IGBT minimum on and off times. Previous research has been found to focus primarily on optimisation of the overall IGBT switch and snubber efficiency., [15]. The choice of components a dictated by these other constraints is discussed in Chapter Four.

Chapter Four also describes the IGBT gate drive system. The design uses one gate drive module for each IGBT. These modules are electrically isolated from the control circuit. The control signals from the main control board are isolated by fiber optic links. Power is supplied at 100 kHz from a switch–mode power supply via transformers. This approach eliminates disturbance to the main controller due to coupled electrical interference from the power circuit. The design of well isolated, interference tolerant drivers is considered mandatory in high power, high frequency converters. The gate drive circuit also provides complete IGBT protection independent of the action of the main control system. The design philosophy adopted was to use all discrete circuitry operating at high current levels.

The design and operation of the clamping system SOI is also discussed. These SOI's use mosfets with a special driving circuit rather than the traditional bipolar transistor as the switching devices. The self oscillation is generated by the partial saturation of an auxiliary transformer, [12]. This results in greater efficiency in comparison with the more common approach of using main transformer saturation. At the close of Chapter Four the overall power loss is calculated at the rated output current of 100A with a 50% duty ratio with nominal bus voltage of 560V. This is used to calculate the cooling requirements.

A full rating prototype buck converter was constructed to verify the design. The test results from this converter are presented in section 4.8. The measured efficiency figures were found to contain a large tolerance because of the limited accuracy of the measurement equipment. In terms of component and heatsink temperature rises the performance of the converter was found to be adequate and in reasonable agreement with the design values.

Chapter Five describes the control system operation and design. Because the converter topology is new, unique control strategies were developed. To obtain the five level PWM feature a four phase symmetrical ramp generator has been implemented. Each phase is responsible for generating the PWM signals for one buck converter. Multiple phase PWM has been applied in DC power supplies to reduce input and output ripple current, but does not appear to be well known to inverter designers, [32]. The techniques developed for this inverter could with some adaptation be applied to the neutral point clamped topology. Further research is being conducted into this technique. To maintain the five level modulation all buck converters must remain in conduction. This is equivalent to maintaining a bias current flowing down each leg. To achieve this the coupling transformer magnetising current must always be maintained above one half the output current.

A control loop which senses and regulates the bias current via manipulation of the coupling transformer magnetising current has been implemented. A second control loop senses and regulates the inverter output current. Due to the IGBT minimum on and off time constraints the inverter output voltage saturates at 75% of the bus voltage. This represents a severe restriction which traditionally has been a problem with high switching frequency converters. It has been overcome in this design by the use of a frequency dropping strategy. Once the minimum off or on time constraint is reached the control action is diverted to linearly reducing the frequency. The result is that the duty ratio, and hence the average output voltage, continues to increase. Using this technique the five level modulation properties are maintained. The resulting ripple current is kept low. The performance of this system has been found to be exceptionally good. It is believed that this innovative technique will be of significant benefit in variable speed motor drive systems.

The chapter develops the relevant design methods and analysis for the new control system. This includes derivation of equations which describe the interaction between control loops. Control loop performance verification was also carried out using the "MATLAB" mathematical analysis package, [33]. The results of the analysis are used to size system components and set parameters.

Detailed simulation of the combined controller and power circuit was carried out using the dynamic systems analysis package "TUTSIM", [18]. The model was constructed so that on a functional level it would resemble closely the hardware design. The purpose was twofold, first it was used to verify the predicted performance, secondly because of the model's detail it was effectively a pre–hardware prototype. Using this procedure labor intensive hardware redesign is avoided. In a large converter it is not practical nor advisable to debug the control system using the full scale power circuit.

A tenth scale model of the power circuit was designed and constructed for the purposes of debugging and tuning the control system. The controller sends and receives signals identical to those in the full scale unit. Chapter Six is devoted to the presentation of results of the "TUTSIM" simulation and the tenth scale model. The very good agreement of the two serves to illustrate the power of systems level simulation. The use of dynamic systems packages for simulation of power electronic systems appears to be under exploited. Using the ideas developed as a part of this project there is great potential for further work in this area. The scale model and simulation results verify the predicted operational characteristics. The output waveform quality up to a modulating frequency of 1kHz is exceptionally good with the total harmonic distortion being less than 0.35%. Performance between 1 and 10 kHz deteriorates with increasing frequency but is still more than adequate for the application.

At this time the full scale amplifier power circuit is not complete. However few difficulties are expected during the commissioning stage because of the methodical design and subsequent verification procedures that have been followed.

2. CONVERTER TOPOLOGY

This chapter focuses on the new five level converter topology. It begins with a review of known techniques which have been used to construct switching amplifiers. These include the Ćuk converter, standard bridge inverter, neutral point clamped inverter and multiple bridge inverter configurations. The suitability of these approaches in relation to the CSAMT application is discussed. In terms of extending bandwidth and improvement of waveform quality multilevel PWM schemes are of benefit in switching amplifier applications. A detailed comparison of two, three and five level schemes is presented. The five level modulation system is simulated with the results being presented. The new five level converter topology uses four switches compared with traditional inverter configurations which require eight. Better switch utilisation is obtained by the use of four buck converters linked by two coupling transformers. The operation and important design parameters of the new topology are discussed.

The buck converter snubbing system topology and operation are also described. The main switch snubbing system is a resonant reversing lossless configuration combined with an active clamp. The snubbing system design equations together with typical buck converter waveforms are presented.

2.1 Conventional Converter Topologies

The choice of the switching converter topology is a critical part of the overall amplifier design. If state of the art semiconductor technology is used then the topology will determine the equipment performance limitations. Since the performance requirements are particularly demanding for this design the topology selection is very important.

The following topologies have been previously used for four quadrant wide bandwidth switching amplifiers:

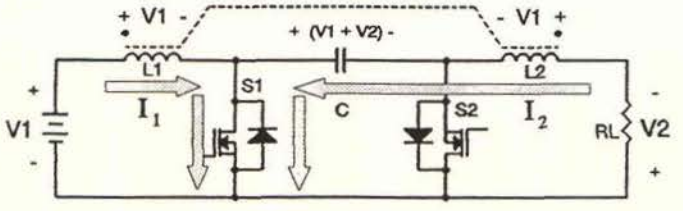
(a) Ĉuk Converter, [17]

(b) Bridge Converter, [1]

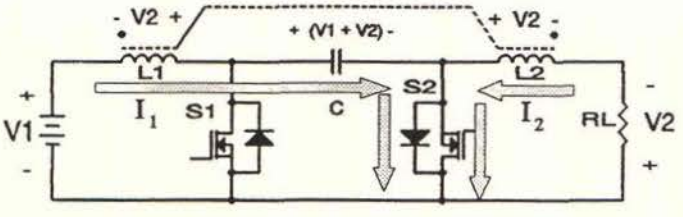
(c) Multi level modified Bridge Converters, [2]

The two quadrant Ĉuk converter is illustrated in Figure 2.1. The Ĉuk converter which is a reasonably new development in converter topologies has some important advantages over conventional Buck and Boost converters. The most significant property which makes it very useful for switching amplifiers is its property of having zero output ripple current, provided coupled inductors (L1 and L2) are used. This gives the possibility of wide control bandwidths and therefore excellent performance. A 40 watt amplifier using this topology has been documented, [17]. This amplifier gave very good performance with a flat frequency response to 20kHz and a Total Harmonic Distortion of 0.1%. However this converter has some serious short comings when a design is attempted at the power levels required in this unit. To aid in the appreciation of this, a brief discussion of the converter operation is included.

Under steady state operating conditions the coupling capacitor, C, has an average voltage of $(V_1 + V_2)$ across it. The capacitor is normally sized such that the ripple voltage over it is relatively small and can be neglected. This condition is forced on the designer in order to keep the capacitor dielectric losses low as well as to keep the output ripple current low. When S_1 is turned on (S_2 off) V_1 is applied across L_1 and current I_2 flows through S_1. The current I_2 flows through L_2 and C also via S_1. Notice that the voltage V_1 is also applied across L_2, this is the reason why the two windings can be coupled. While S_2 is on (S_1 is off) the voltage V_2 is applied across L_2 and L_1. The current I_1 flows through L_1 and C via S_2. The current I_2 flows through L_2 also via S_2. During the entire cycle energy is transferred between the source and the load via the capacitor and there is an interchange of energy between the capacitor and the magnetic core.



Switch S1 ON;Switch S2 OFF



Switch S1 OFF;Switch S2 ON

Figure 2.1 Ćuk Converter Operation

By consideration of charge conservation in the capacitor and input to output power equality the D.C. transfer ratio can be easily shown to be:

$$V_2 = V_1 \frac{D}{1 - D} \qquad 2.1\text{–}1$$

$$D = \frac{T_1}{T_1 + T_2} \qquad 2.1\text{–}2$$

The variables T_1 and T_2 are the on times for S_1 an S_2 respectivly.

An important property of the coupled inductor configuration is that if the turns ratio $\sqrt{\frac{L_1}{L_2}}$ is adjusted to be equal to the coupling factor then the effective output inductance can be shown to approach infinity. This means that in the ideal case the output ripple can be forced to zero. This is an excellent property which makes this converter ideal for switching amplifier applications. However the coupling capacitor at high power levels is of considerable physical size since it is effectively transferring the entire converter load and must be rated at least two times the input voltage. In addition to this the two switching devices must be capable of handling twice the rated load current at twice the input voltage making any design difficult at higher power levels. The switch snubbing requirements are as a result considerable.

Although the topology has some very good advantages it is not a practical solution at high powers. A more practical four quadrant topology is the standard bridge inverter as shown in Figure 2.2. The simplest switching strategy for the bridge inverter is to alternately switch diagonal pairs of switches. For a bus voltage of 2E there are two possible output levels, 2E and –2E. This gives rise to two level pulse width modulation as illustrated. The output frequency in this case is the same as the switch frequency. Phase shifted leg switching can also be used to obtain double the output ripple frequency.

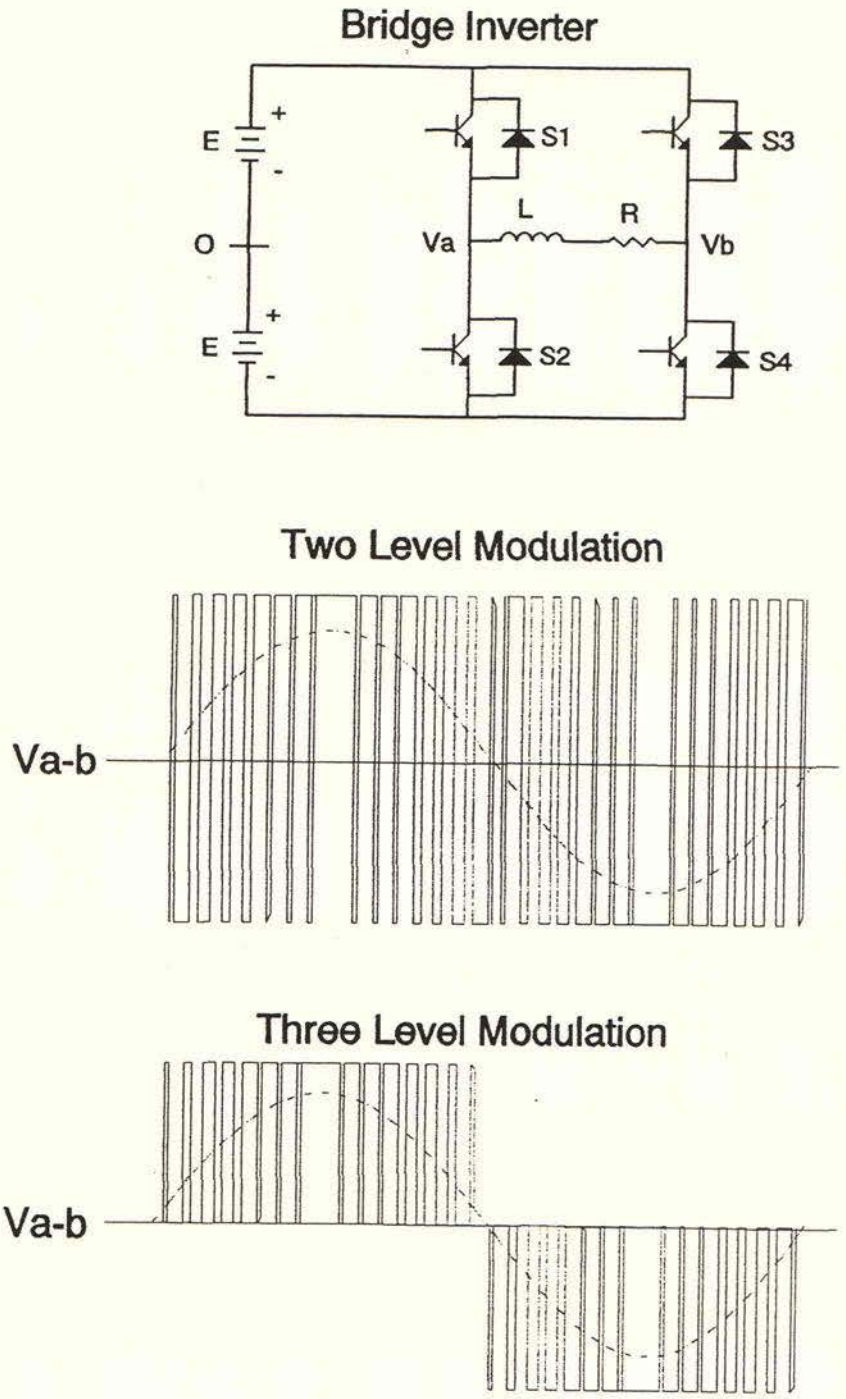


Figure 2.2 Bridge Inverter Modulation Techniques

This also results in the production of three output levels, +2E, 0, –2E. The same technique was used in the earlier amplifier design, [1]. Because the effective frequency is doubled and the voltage step is halved the maximum ripple current in the output inductor is one quarter that of the two level case. This gives a significant advantage for a little extra complexity in the control system. A further extension of this is five level modulation which results in an output frequency of four times the switch frequency and a voltage step of one quarter that of the two level case. The result of this is a sixteen fold reduction in the maximum ripple current. This is a large advantage which has been exploited in a number of high power converters. In particular Marchesoni, [2], has applied the technique in amplifiers with a rating of 3.6 MVA and a bandwidth of 10kHz for application in nuclear fusion experiments. It is quite clear then that this technique would yield acceptable results in the case of this amplifier. The two extra switching levels are normally obtained by the addition of two phase legs in either the neutral point clamped configuration or the series connected bridge configuration as illustrated in Figure 2.3. A typical sine wave modulated five level waveform is shown in Figure 2.4. Marchesoni has proposed a quite complex control system to obtain the correct switch sequence to give the five levels. However it was believed that a simple phase shifting strategy was all that was required, this was later confirmed by simulation and a scale model.

2.2 Multilevel Modulation

The benefits of multilevel switching using phase displaced legs is illustrated in Figure 2.5. Part(a) shows a two level inverter supplied at 2E. This can be modeled as one source $V_a(t)$ which switches between +2E and –2E. Part (b) shows a three level inverter which can be modeled by two sources which switch 180^0 out of phase and are added to produce the output voltage. Each source represents one inverter leg. Three output levels are produced and the output frequency is twice the switch frequency. A five level inverter model is shown in Part (c).

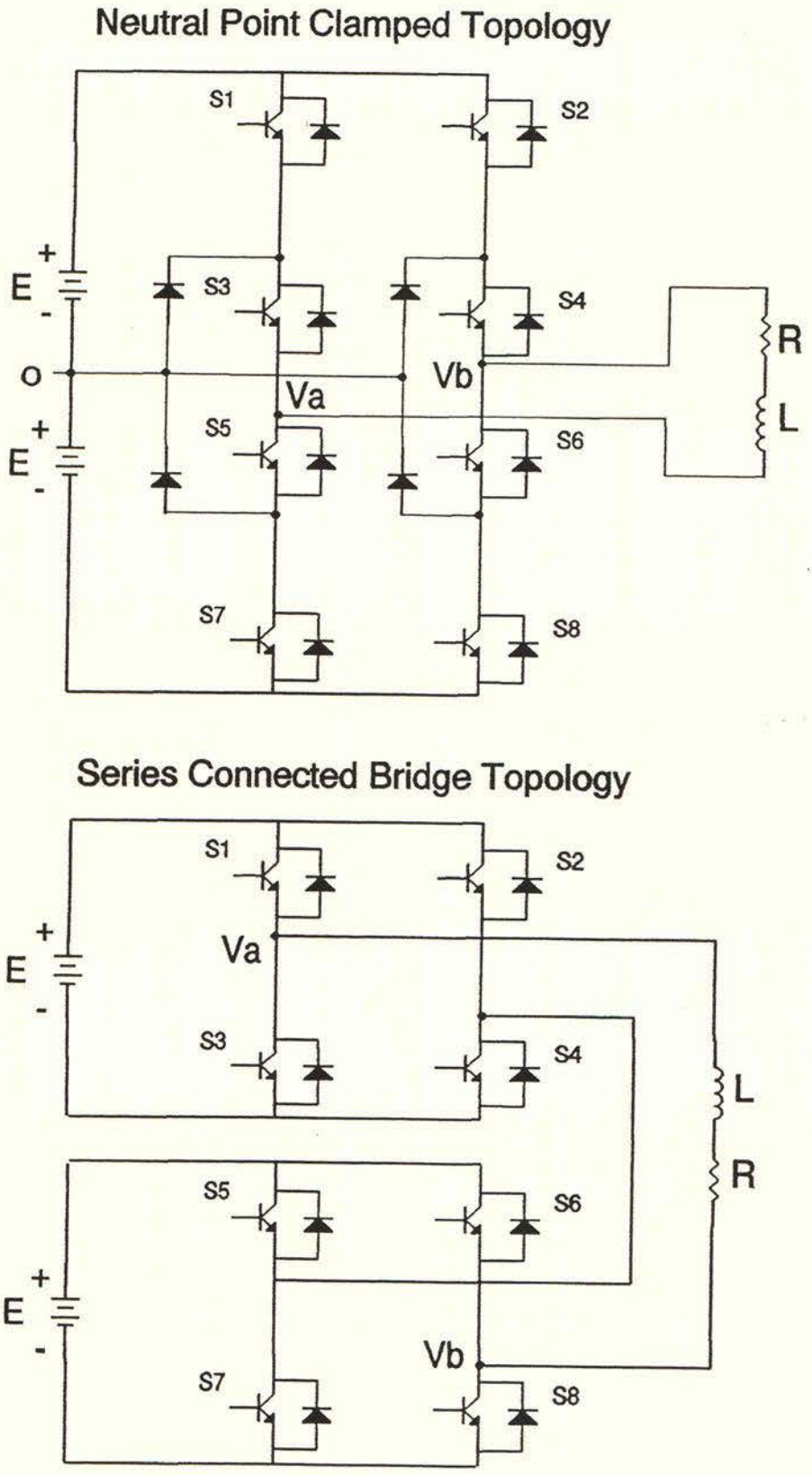


Figure 2.3 Conventional Five Level Topologies

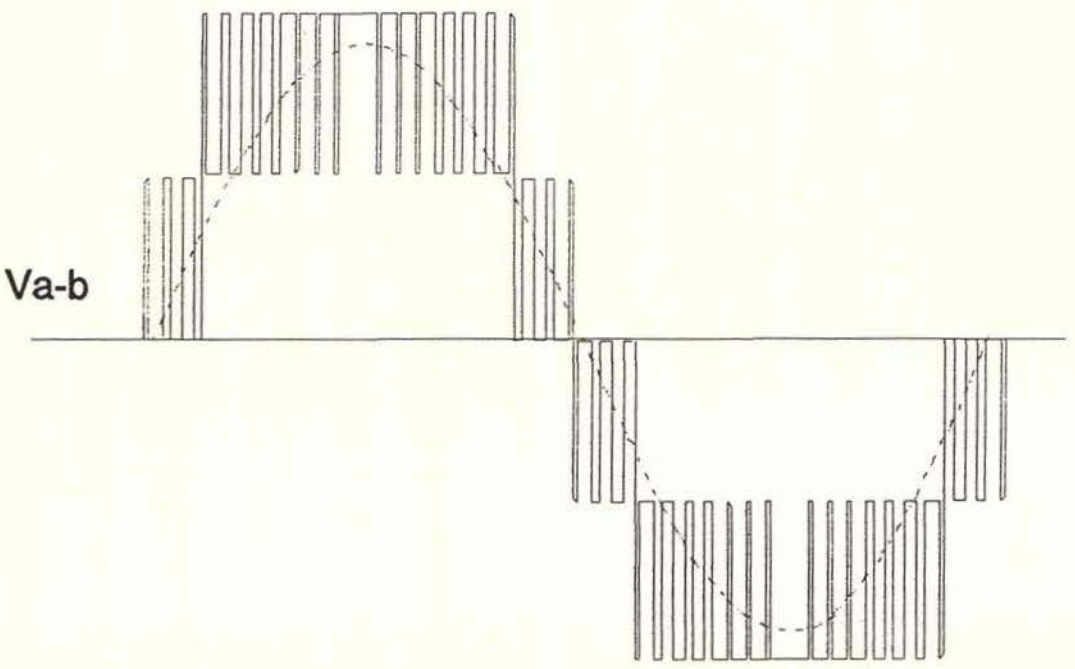


Figure 2.4 Five Level Modulation Waveform

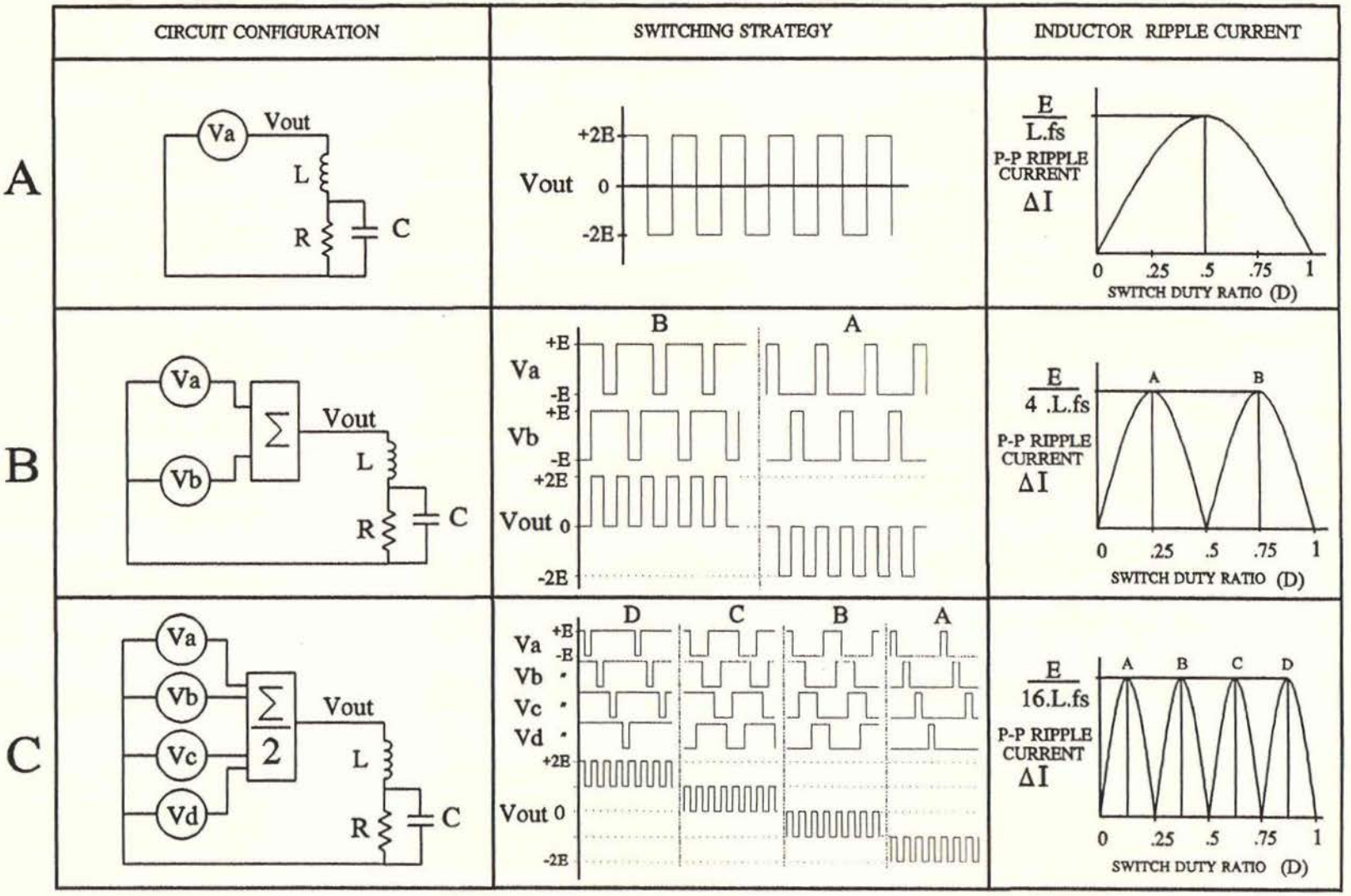


Figure 2.5 Two, Three and Five Level Switching Strategy Comparison

Two more sources are introduced, with all sources being phase displaced by 90^{o}. The addition of the four sources produces the five possible levels as illustrated. In each case each level is produced in a different duty cycle range. The output inductor ripple current as a function of the duty ratio is also shown for each case. For the two level inverter the maximum occurs at a duty ratio of one half and has a value of:

$$\Delta I = \frac{E}{L\ f_s} \qquad 2.2\text{–}1$$

For the three level inverter the maximum ripple occurs at one quarter and three quarters duty ratio and has a value of:

$$\Delta I = \frac{E}{4\ L\ f_s} \qquad 2.2\text{–}2$$

For the five level inverter maximums occur at duty ratios of one eighth, three eighths, five eighth an seven eighths with a value of:

$$\Delta I = \frac{E}{16L\ f_s} \qquad 2.2\text{–}3$$

Figure 2.6 gives a better appreciation of the overall improvement in output current ripple of five level modulation over two level modulation as a function of duty ratio. The average ratio of the peak to peak ripple for a five level system to a two level system is 0.09. This means that a five level system switching at 50kHz is, in terms of peak ripple current, as good as a two level system switching at 556kHz. This represents a substantial improvement in output quality and the achievable control bandwidth. The improvement of a five level modulation system over a three level system is also displayed in Figure 2.7. In this case the average improvement is one third. A five level modulation simulation was run using "TUTSIM",[18], to determine the output voltage and current spectrum for a 10kHz input signal.

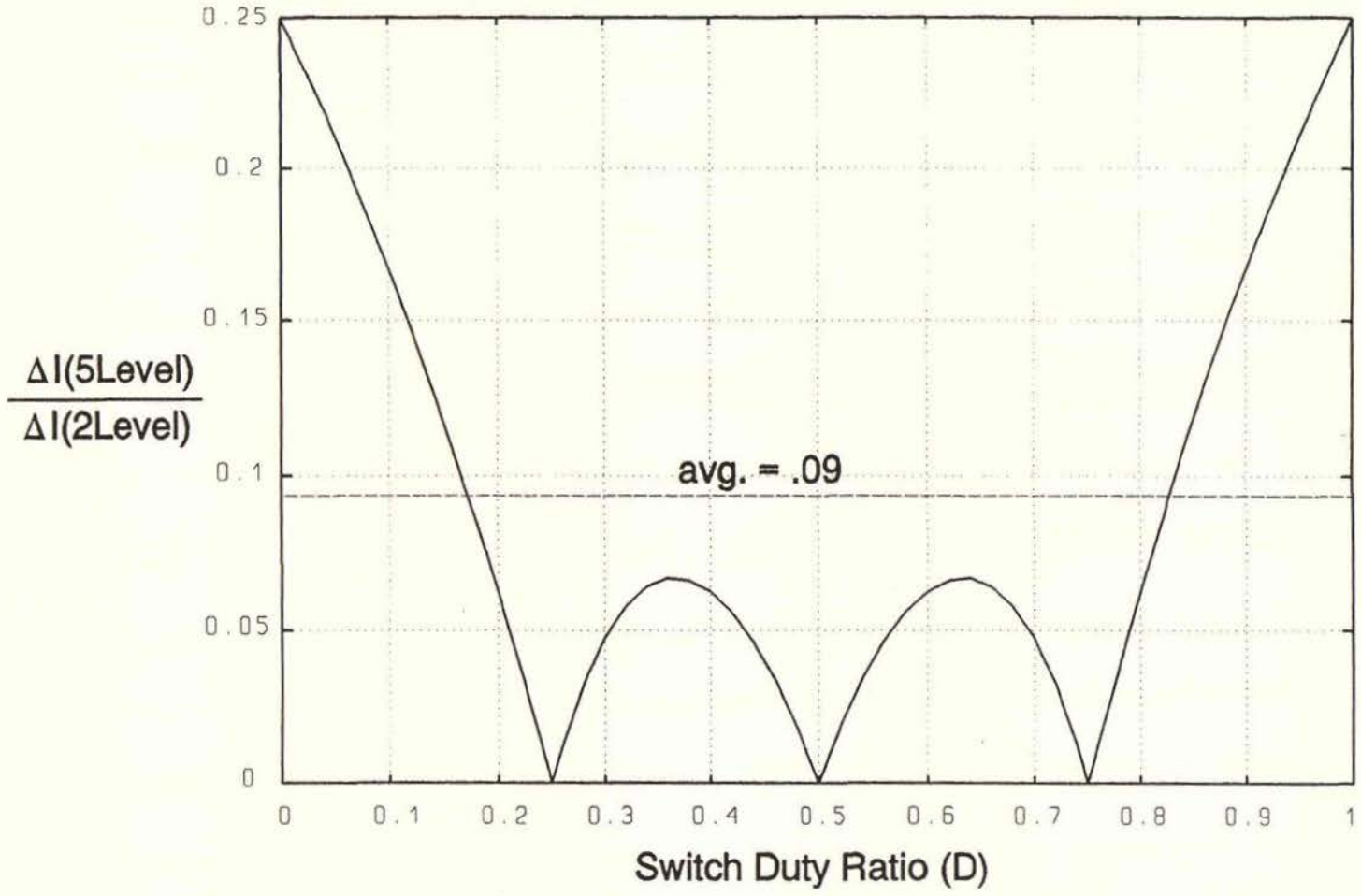


Figure 2.6 Current Ripple Improvement of 5 Level Over 2 Level Modulation as a Function of Duty Ratio

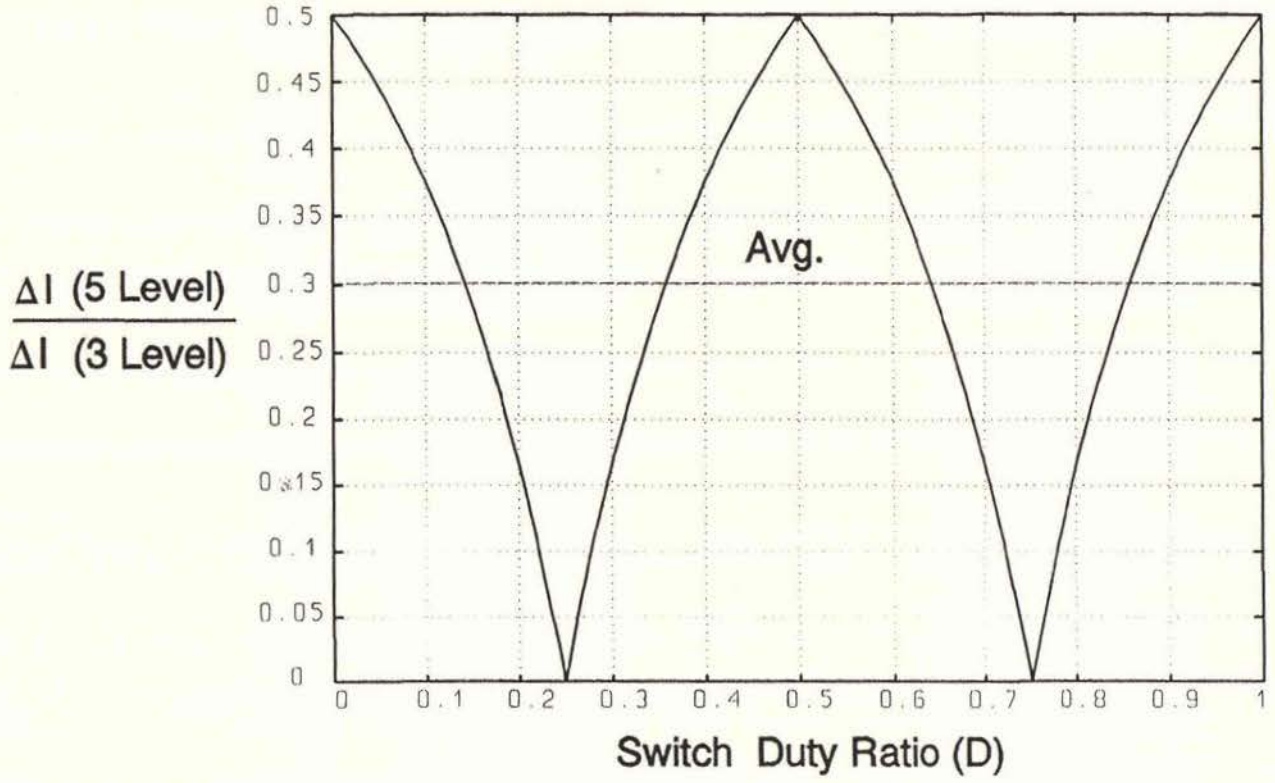


Figure 2.7 Current Ripple Improvement of 5 Level Over 3 Level Modulation as a Function of Duty Ratio

The Tutsim model is shown in Figure 2.8. A common 50kHz symmetrical ramp signal is delayed by 5μS,10μS and 15μS to obtain the four phase set. Each ramp is compared with the modulating signal to produce the four phase PWM. These are applied to relays which switch between +E and –E (+/– 280 volts in this case). These are summed to produce the five level load voltage. The load has been set to 2Ω resistance in series with 200μH inductance. The simulated load voltage and current for a 10kHz modulating signal is shown in Figure 2.9. The voltage spectrum shown in Figure 2.10 is of interest since it shows that the spectral components are side bands spaced at increments of the modulating frequency around a suppressed carrier at the switch frequency multiplied by four. In this case the first side band is at 200 $\pm$ 10kHz. Note that there is no component at the switch frequency of 50kHz. Perfect cancellation is to be expected since this is an ideal simulation, however in a real system perfect cancellation cannot be obtained. Nevertheless the 50kHz component can be kept relatively low by careful design. The current spectrum is shown in Figure 2.11. The high frequency spectral components produced by the five level scheme are found to be heavily attenuated by the load with the highest being at 150kHz with an amplitude of only a fraction of an amp. for a 30A_{rms} output.The control bandwidth is normally limited by the peak to peak ripple current. The converter plus controller is normally considered to be a linear system in so far as the control analysis is concerned. This assumption however breaks down once the ripple level at the input to the pulse width modulators becomes excessive. Normally bandwidths are restricted to one tenth of the effective switching frequency. This would mean a bandwidth of 20kHz should be easily obtained with a five level converter switching at 50kHz. This topic will be more thoroughly explored in Chapter Five.

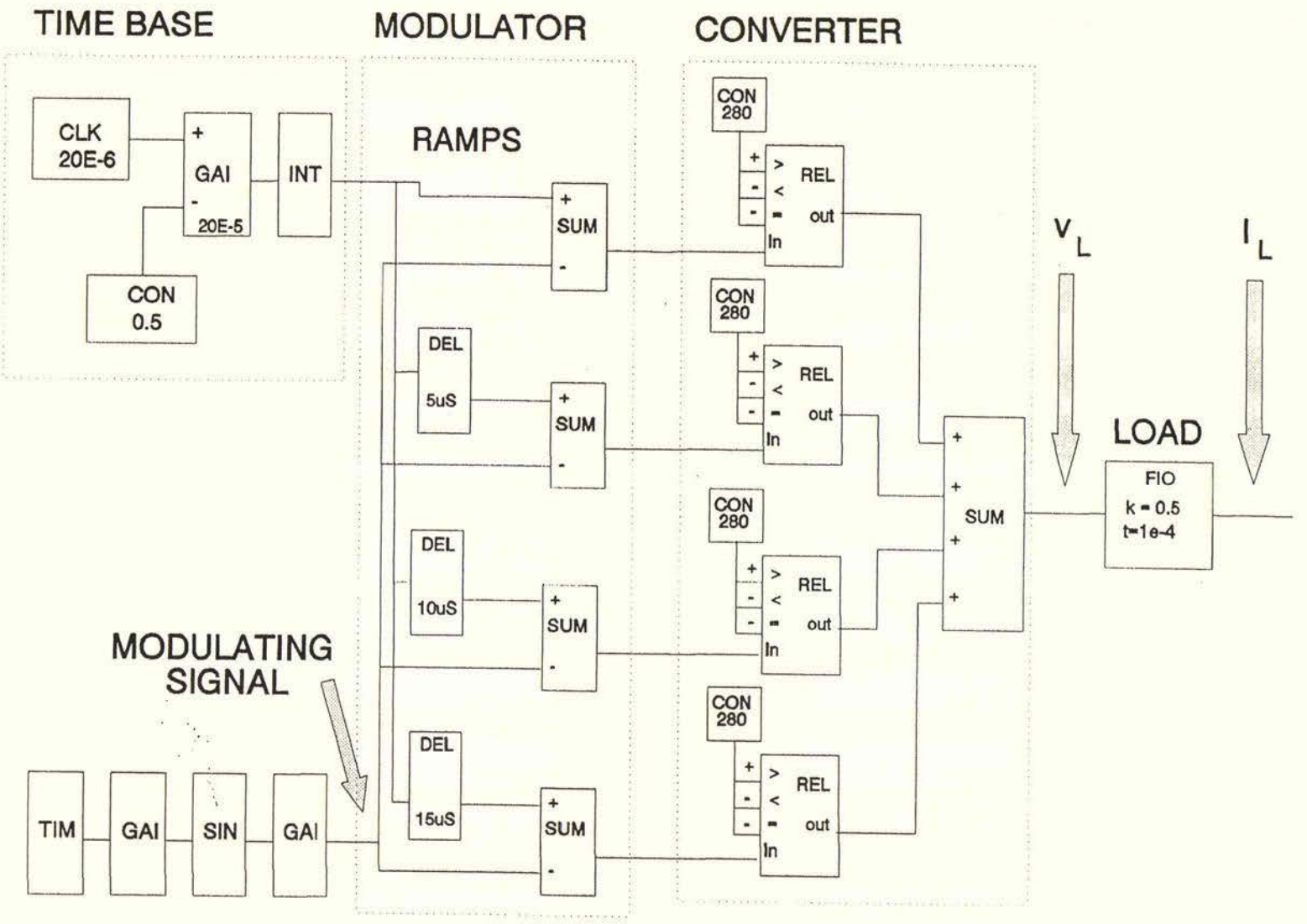


Figure 2.8 Five Level Modulation Simulation "TUTSIM" Model

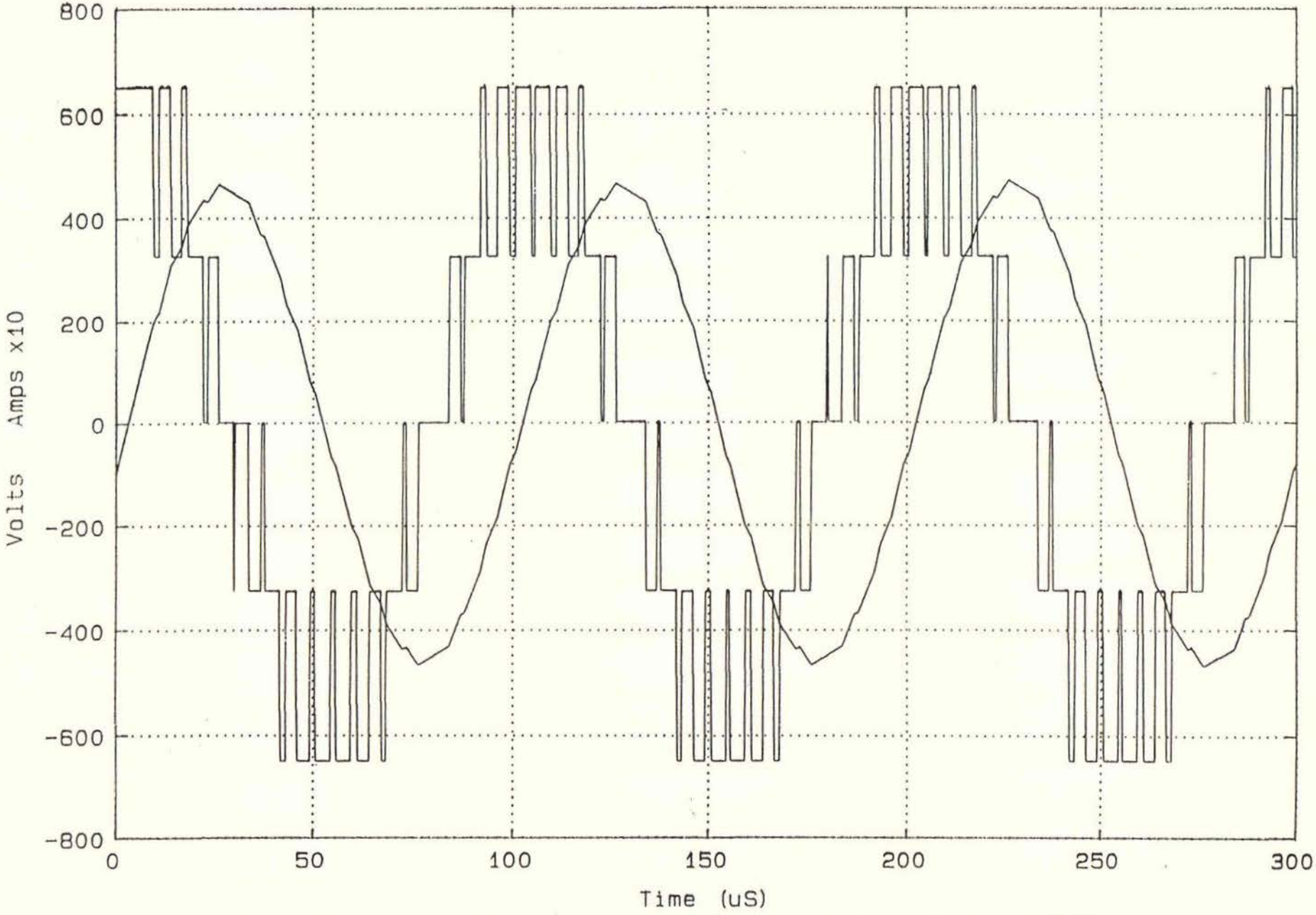


Figure 2.9 Five Level Modulation Simulation Results (Load Voltage and Current)

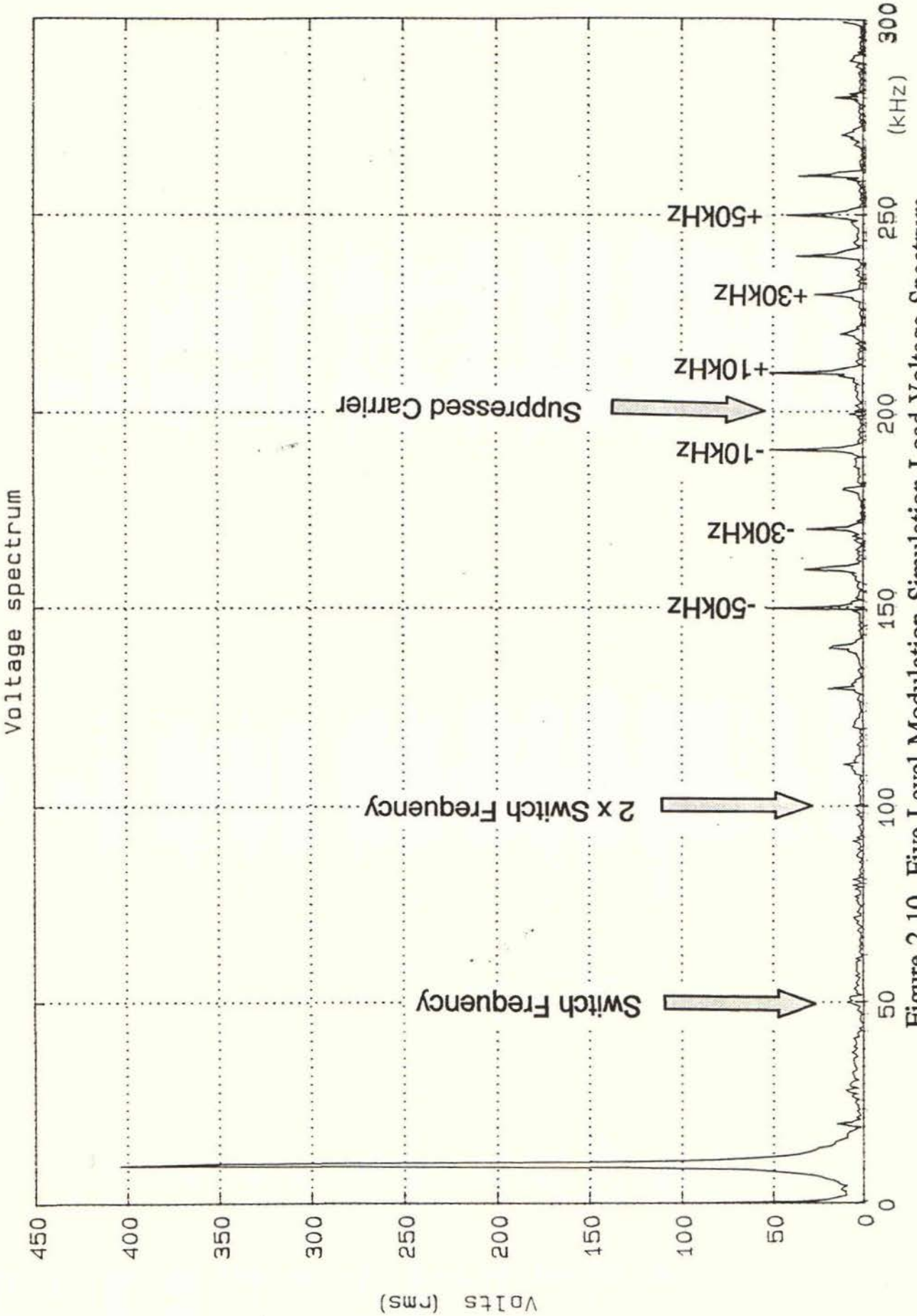


Figure 2.10 Five Level Modulation Simulation Load Voltage Spectrum

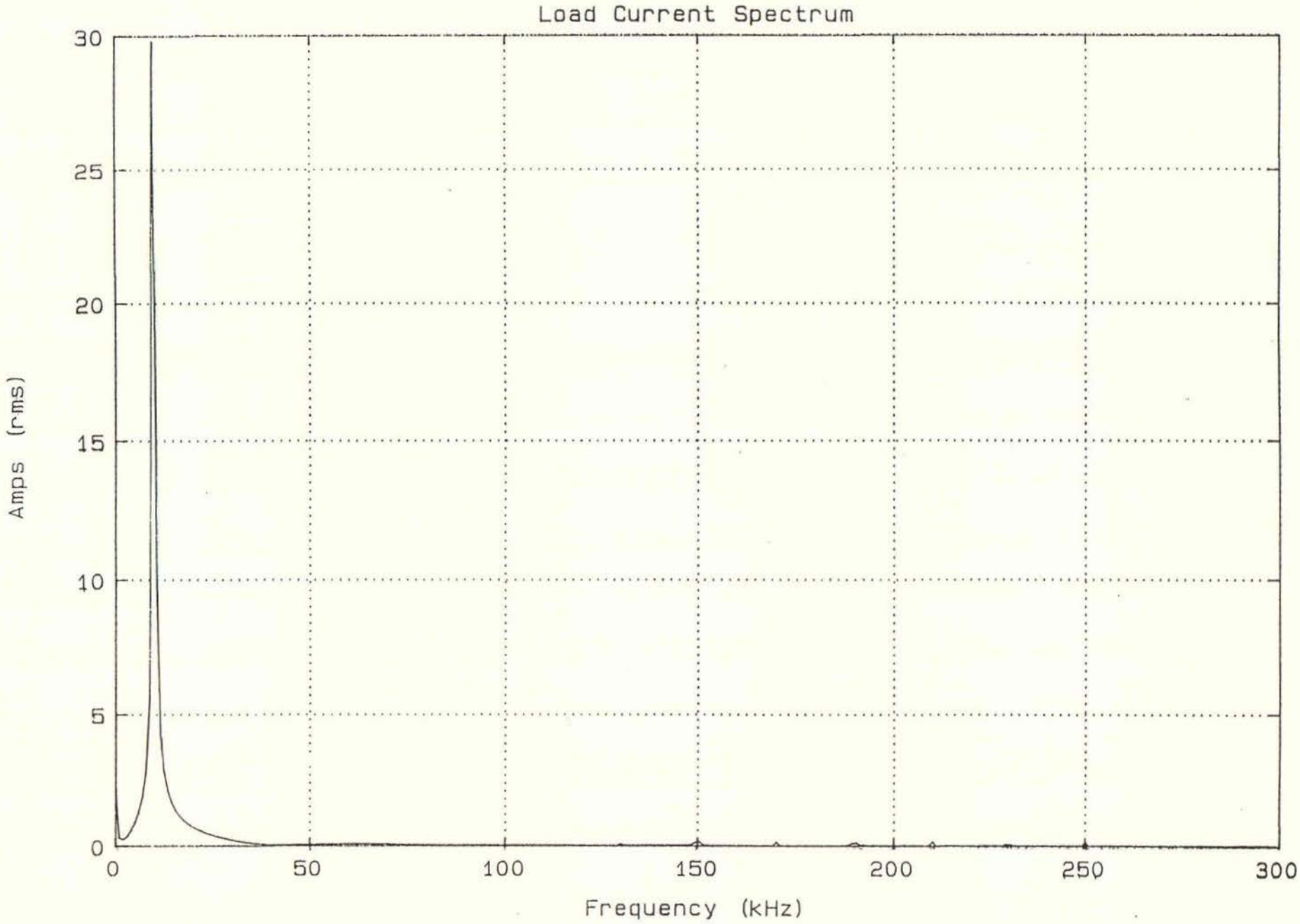


Figure 2.11 Five Level Modulation Simulation Load Current Spectrum

2.3 The New Five Level Converter Topology

As previously indicated five level modulation has normally been achieved by the neutral point clamped or the series connected bridge topology. In both cases two extra phase legs and hence four switches are added to produce the two extra levels. For the application this represented an unacceptable increase in the power circuit complexity and so a different approach was needed. An alternative solution is to replace the bridge converter by four buck converters. If the buck converters operate in the continuous conduction mode they produce a two level output waveform. These can be controlled to produce the four phase waveforms as shown in part(c) of Figure 2.5. A five level modulation scheme can therefore be achieved if the outputs of the four buck converters can be combined. Figure 2.12 shows how the combining was achieved. The two buck converters from one phase leg are coupled by a center tapped auto transformer and the load is connected between phase legs. The phase leg output voltages will be given by:

$$V_a(t) = \frac{v_{ap}(t) + v_{an}(t)}{2} \qquad 2.3\text{–}1$$

$$V_b(t) = \frac{v_{bp}(t) + v_{bn}(t)}{2} \qquad 2.3\text{–}2$$

The buck converter voltages all have identical pulsewidth modulated waveshapes but are phase displaced. With $V_{ap}(t)$ as a reference and a buck converter switching period of T, the following equations can be written:

$$V_{an}(t) = V_{ap}(t\text{–}T/4) \qquad 2.3\text{–}3$$

$$V_{bn}(t) = -V_{ap}(t\text{–}T/2) \qquad 2.3\text{–}4$$

$$V_{bp}(t) = -V_{ap}(t\text{–}3T/4) \qquad 2.3\text{–}5$$

And the output voltage is:

$$V_{out}(t) = V_a(t) - V_b(t) \qquad 2.3\text{–}6$$

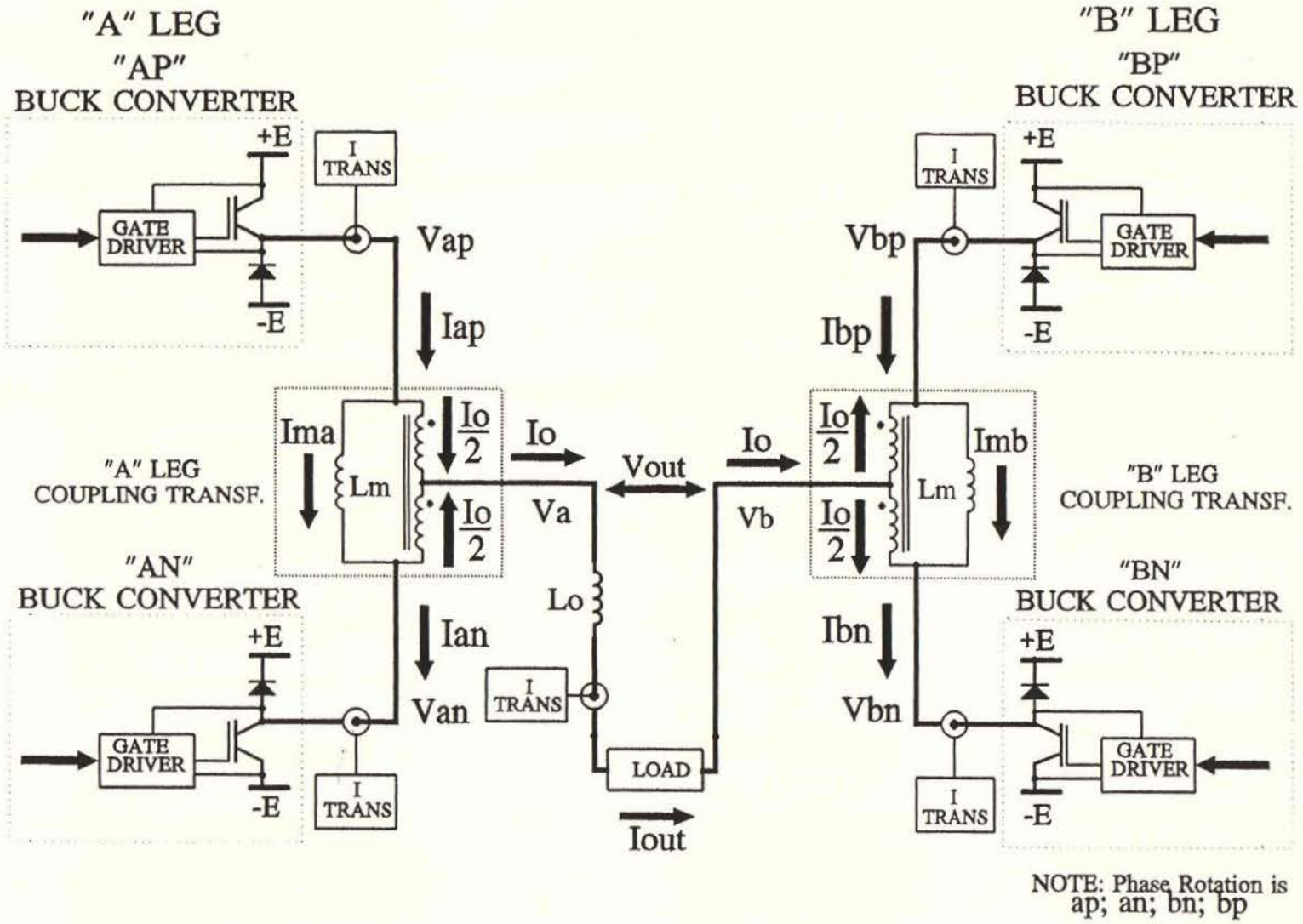


Figure 2.12 New Five Level Inverter Topology

Therefore combining equations:

$$V_{out}(t)=\frac{V_{ap}(t)+V_{ap}(t-T/4)(V_{ap}-T/2)+V_{ap}(t-3T/4)}{2} \qquad 2.3\text{–}7$$

The output will therefore be five level providing all the buck converters remain in conduction. Because the positive buck converters "AP" and "BP" can only source current and the negative buck converters "AN" and "BN" can only sink current a bias current must be maintained flowing down each leg at all times so that all converters remain in conduction. This bias current can be created by forcing a volt–second difference between the top and the bottom converters which causes a magnetizing current I_{ma} to be established in L_m. The discussion of the bias current will be limited to that concerning the "A" leg, the operation of the "B" leg being identical. This volt–second difference is easily produced by forcing a deviation in pulsewidths at the modulator stage of the controller. The bias current is given by the following: (note: all the following equations refer to average currents)

$$I_{bias} = \frac{I_{ap}(t) + I_{an}(t) - abs[I_{ap}(t) - I_{an}(t)]}{2} \qquad 2.3\text{–}8$$

The above expression is simply the minimum out of I_{ap} and I_{an}. The two converter currents from Figure 2.12 are related to the leg magnetizing current I_{ma} and the output current I_o by the following relationships:

$$I_{ap}(t) = I_{ma}(t) + \frac{I_o(t)}{2} \qquad 2.3\text{–}9$$

$$I_{an}(t) = I_{ma}(t) - \frac{I_o(t)}{2} \qquad 2.3\text{–}10$$

Therefore from equation 2.3–8:

$$I_{bias}(t) = I_{ma}(t) - \frac{abs[I_o(t)]}{2} \qquad 2.3\text{–}11$$

And I_{ma} can be controlled by the differential volt seconds across L_m with the following relationship applying:

$$I_{ma}(t) = \frac{1}{L_m} \int \Delta V(t)\, dt \qquad 2.3\text{–}12$$

A simple proportional negative feedback control loop can be used to set the bias current to a desired level. However it can be seen from equation 2.3–11 that the output current acts as a disturbing influence in this loop and so it is found that it is not practical nor desirable to design a controller which can hold the bias current constant, this is discussed in more detail in Chapter Five.

An incidental but very significant benefit of this topology is the elimination of the "leg shoot through fault" possibility of the normal bridge inverter. In high voltage systems this can cause the complete destruction of the inverter components. For this inverter the through current(bias current) is a controlled variable.

2.4 Coupling Transformer Selection

The selection of the coupling transformer is effected by the following factors:

(a) Buck converter maximum peak to peak ripple current

(b) Performance of the bias current control loop

The performance of the bias current control loop is the most complex factor to analyse. During dynamic changes in output current the bias current control loop will act to keep the bias current constant as already explained. In doing this it can be shown that a 50kHz spectral component will be introduced into the output voltage.

To show that this is true consider that the output current is increasing at a fixed rate, m, so that:

$$I_o = mt \qquad 2.4\text{–}1$$

Now it will be assumed that the control loop has the ability to maintain the bias current constant at I_{set}. This means that:

$$I_m = I_{set} + \frac{m}{2} t \qquad 2.4\text{–}2$$

To obtain I_m a voltage ΔV must be impressed across L_m which will be given by:

$$\Delta V = L_m \frac{dI_m}{dt} = L_m \frac{m}{2} \qquad 2.4\text{–}3$$

This means a constant differential voltage must be maintained across L_m to keep I_{bias} constant when the output current is rising at a constant rate. Because the phase rotation of the converter must be ap;an;bn;bp to obtain the five level output the converters contribute one pulse in the same order to the output each 20uS as illustrated in Figure 2.13. To create the differential voltage between the "AP" and "AN" converters the "AP" pulse will be wider than the "AN" pulse and likewise the "BP" pulse will be wider than the "BN" pulse. Because of the phase rotation the result is two long pulses followed by two short pulses. This pattern repeats itself every 20μS and therefore has a 50kHz fundamental component. The difference between the two waveforms clearly illustrates this. The 50kHz component can be shown to be proportional to L_m and m. This 50kHz component is undesirable since it degrades the output waveshape as well as giving potential problems in the main current control loop. The exact calculation of the 50 kHz component requires complex analysis beyond the scope of this project.

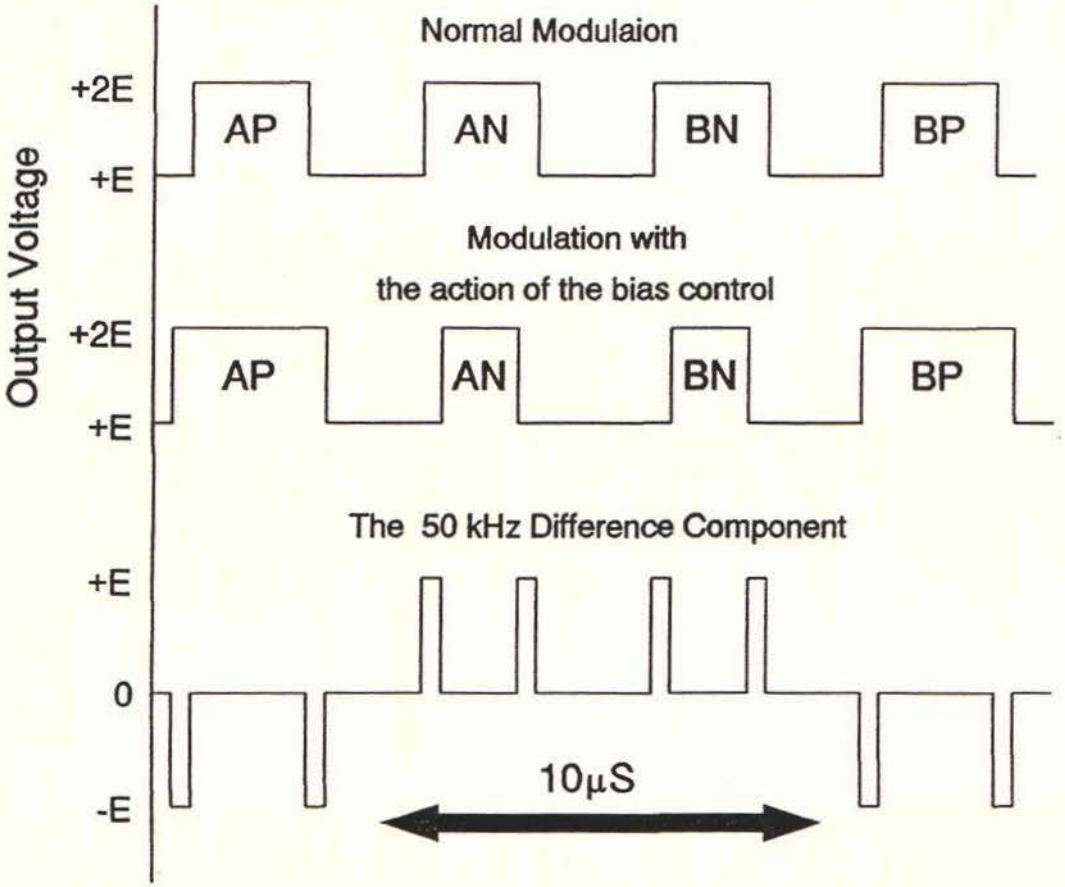


Figure 2.13 The Effect of Bias Current Control on the Modulation Integrity

The approach in this design has been to not make the bias current control loop respond to fast rates of change in output. That is its bandwidth is limited which avoids the problem described above. However this results in the necessity of setting the bias current slightly higher. This leaves the buck converter peak to peak ripple current as the major factor involved in the selection of L_m. The low power model was constructed with $L_m = 400\mu H$. The "TUTSIM" simulation and the low power model both gave quite acceptable results using this value. The simulation showed that L_m could be reduced to $200\mu H$ before the performance degraded. It was found by simulation that for inductances below $200\mu H$ the whole system became prone to chaotic modes of behavior. With only a small magnetizing inductance small switching descrepencies can cause large changes in the output current. This can lead to complex non–linear interactions between the two control loops which is thought to lead to the disturbances that occurred. Although it was intended to make $L_m = 400\mu H$ and all the low power and simulation testing was based on this value, because of the restrictions of core sizes and availability the actual implemented value will be $325\mu H$. This is constructed from six SIEMENS UU 93/152/30; Seferrit N27 cores with a 7.5mm gap between cores. The winding consists of 28 turns of $25mm^2$ litz conductor with a center tap.

The peak to peak ripple current in L_m, which is also that carried by the converters since the output ripple is considered negligible, can be found by realising that the maximum time for which the bus voltage is applied across it is $5\mu S$. The ripple current will therefore be given by:

$$\Delta I = \frac{2E\ \Delta t}{L_m} \qquad 2.4\text{–}4$$

$$= \frac{2 \times 336 \times 5}{325} = 10.3 \text{ A p–p}$$

This ripple is added to the bias current in addition to the output peak current. This effects how low the bias current can be set. In this respect a peak current of 5.15 A represents an acceptable amount.

2.5 Buck Converter Cell Topology

A simplified schematic of the chosen Buck converter cell is shown in Figure 2.14. The primary factor involved in the selection of the Buck converter cell topology is the necessity to keep the switching losses in the IGBT and freewheel diodes to an acceptable level. To reduce the switching loss snubbers are employed. There is a preference in high power converters for lossless snubbing systems to be implemented. The extra complexity of lossless snubbing is justified since the lost power would otherwise be so high that it becomes difficult to dissipate with an acceptable temperature rise. There have been many lossless snubbing systems proposed in the literature,[10–14]. The basic principle is always to reduce the IGBT switch on and switch off loss as well as the freewheel diode reverse recovery loss. The reverse recovery loss is controlled by the peak reverse current. This is reduced by limiting the current diversion, (di/dt), rate from the freewheel diodes (D_f) to the IGBT. Because of the addition of L_f the IGBT turn on loss is also kept low since the rate of rise of collector current is slow relative to the devices inherent rise time. Limitation of di/dt is achieved by the addition of the inductor L_f in series D_f. This diode reverse recovery current also adds to the peak current which the IGBT is required to carry. From this point of view it is also desirable that it be reduced. However the inclusion of L_f means that the IGBT turn off the load current can only be transferred to the freewheel diodes at a limited rate. This rate is determined by how high an IGBT collector emitter voltage overshoot can be tolerated at turn off.

The IGBT turn off loss is limited by providing an alternate path for the load current with a controlled rate of increase of collector emitter voltage to a peak level which is well within the devices capability. A capacitor is normally used to control the rate of rise of collector emitter voltage. If this capacitor is made sufficiently large it can also be made to completely divert the load current into L_f without V_{ce} becoming excessive. This however results in a relatively long diversion time and large snubber capacitors which makes this approach impractical for high operating frequencies.

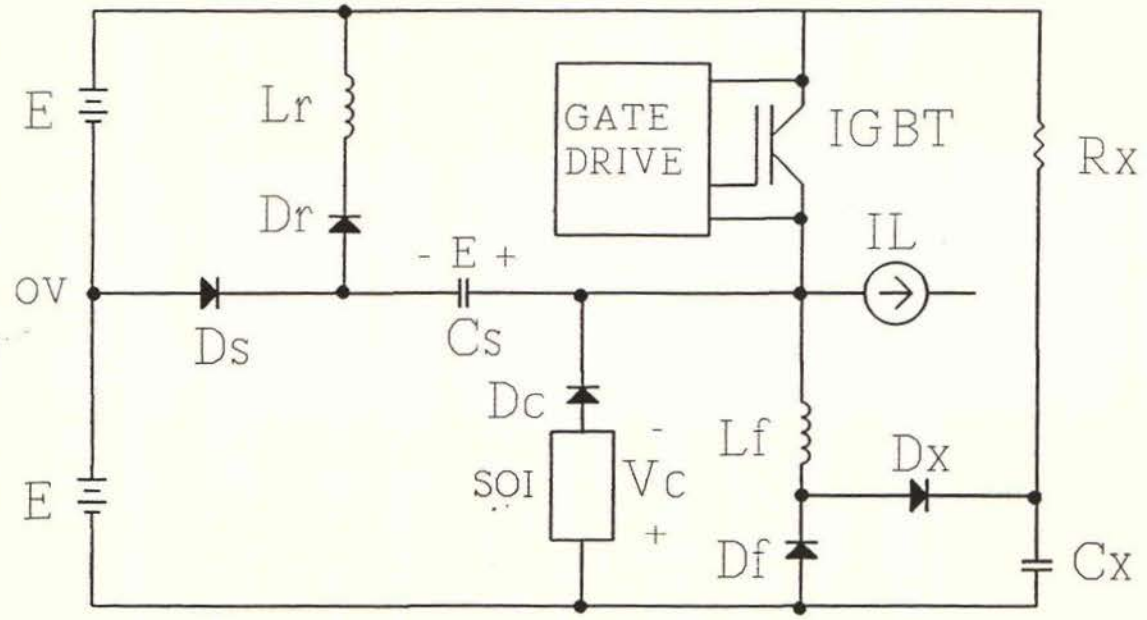


Figure 2.14 Simplified Positive Buck Converter Cell

A better approach is to utilise the capacitor to just limit the rate of rise of voltage such that the turn off energy is at an acceptable level and use a lossless clamp to limit the maximum collector emitter voltage.

The lossless snubbing/clamping system finally chosen is a combination of two techniques as shown in Figure 2.14. A resonant resetting capacitive dv/dt IGBT snubber was implmented which requires access to a d.c. supply center point, which is normal for high voltage buses. This topology was the least complex out of those reviewed, [11]. The lossless clamping system uses a self oscillating inverter (SOI) to feed the energy associated with the magnetization of L_f back to the supply, [13]. The clamp voltage V_c controls the IGBT overshoot and hence the current diversion rate. The clamp system D_c and V_c guarantees that the IGBT collector emitter voltage is restrained. The SOI is tied to the supply bus, this means the clamp voltage is determined by the bus voltage and the clamp energy associated with the magnetization of L_f is conserved. It is possible to use only the clamp and omit the the snubber but the switching loss will be considerable. To illustrate this point the loss will be calculated. Energy would be dissipated during the IGBT current fall time of 200nS. For E = 336V, a clamp voltage of 156V and a load current of 100A the power dissipation for a switch frequency of 50kHz would be:

$$P_s = (2E + V_c)\frac{I_L}{2} t_f f_s \qquad 2.5\text{–}1$$

$$= 828 \times \frac{100}{2} \times 0.2 \times 0.05 = 414 \text{ watts}$$

As will be shown in Chapter Four this is considerably more than the conduction loss (178 watts worst case) and is unacceptably high.

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The unclamped peak voltage is:

$$V_p = 2E + I_L \sqrt{\frac{L_f}{C_s}} \qquad 2.5\text{–}2$$

The cosine decay time is:

$$t_3 - t_2 = \frac{\pi}{2} \frac{1}{\sqrt{L_f C_s}} \qquad 2.5\text{–}3$$

The case where the voltage reaches its peak only occurs at low load currents. It is assumed in Figure 2.15 that the load current is high and the clamp voltage is reached with the current in D_s being diverted to to the clamp. This current then decays linearly over t_3 to t_4. The diode D_f takes up current over this period due to the clamp voltage diverting current to L_f. The diversion to L_f is lossless with energy being stored in C_s and also transferred back to the supply via the active clamp. At the IGBT turn–on two processes occur. The first process is the diversion of the load current from D_f to the IGBT at a rate determined by:

$$\frac{dI_f(t)}{dt} = \frac{2E}{L_f} \qquad 2.5\text{–}4$$

The value of L_f is selected to limit the reverse recovery loss in D_f. At t_6 diode D_f recovers. The IGBT turn on loss is low as its collector voltage falls before any significant collector is established. The second process is the resonant resetting of capacitor C_s. At t_5 a resonant current begins to flow in L_r, D_r, C_s and the IGBT. The current is:

$$I_r(t) = (V_c - E) \sqrt{\frac{C_s}{L_r}} \sin \frac{t}{\sqrt{C_s L_r}} \qquad 2.5\text{–}5$$

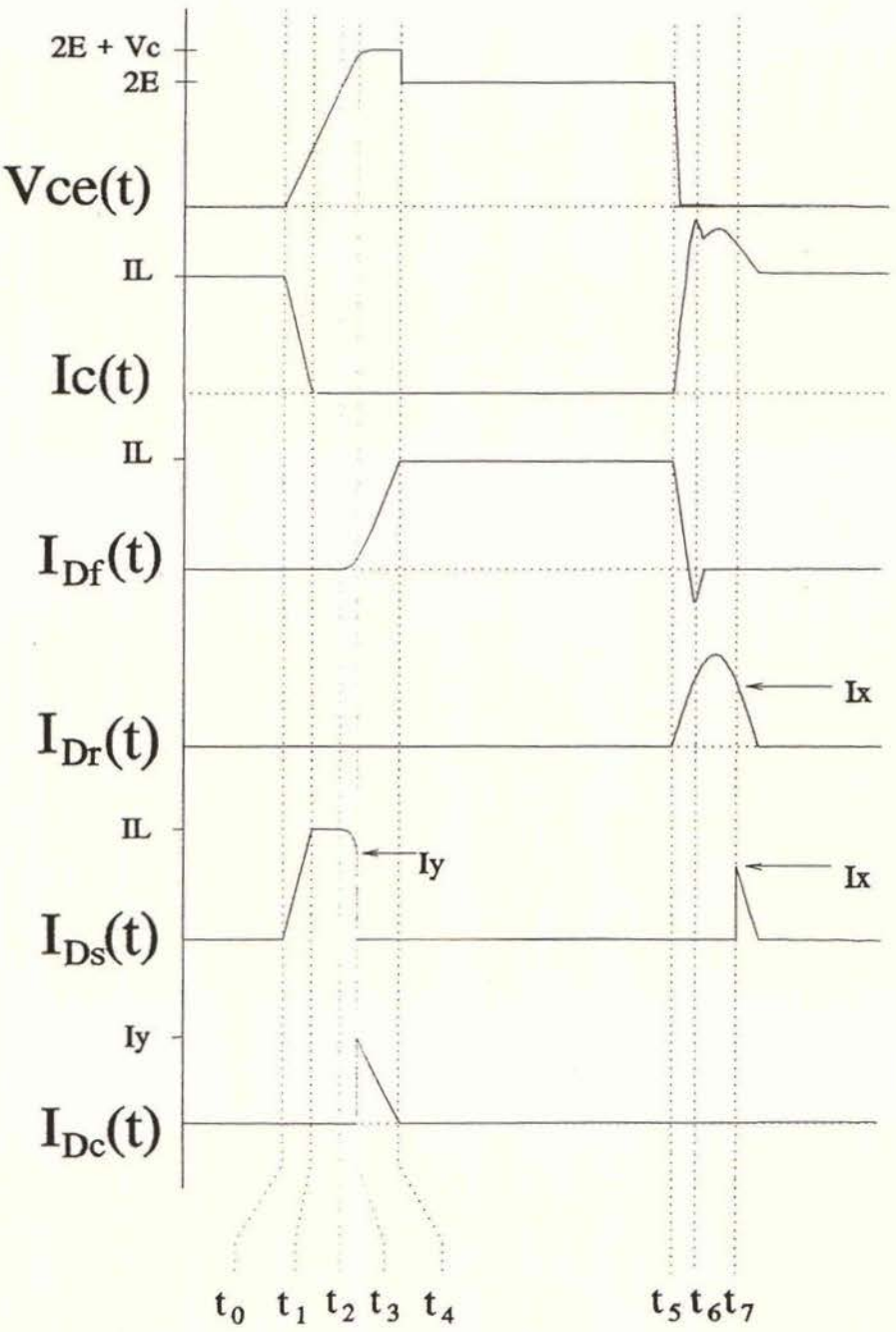


Figure 2.15 Positve Buck Converter Cell Waveforms

This current persists until C_s is reset to E. Current then transfers to D_s,D_r and L_r. The inductor decays linearly to zero at the following rate:

$$\frac{dI_r(t)}{dt} = \frac{E}{L_r} \qquad 2.5\text{–}6$$

During this period the capacitor overcharge energy due to the clamping action during the IGBT turn–off is returned to the supply.

3. POWER DEVICE MODELING

An important part of any high power converter design is the determination of the power device voltage stress, current stress and power dissipation. These are used in an iterative process to:

(a) select the power devices
(b) determine suitable snubbing
(c) determine the cooling requirement

The development of accurate device models is fundamental to calculation of the power semiconductor stress levels. In this chapter the modeling of the power diodes and the IGBT will be considered.

The selected diodes had reverse recovery data limited to one operating point. This necessitated the development of a procedure for the calculation of the reverse recovery performance from limited data. A large proportion of the chapter is devoted to semiconductor diode charge control theory and the subsequent development of this procedure. Because the SPICE circuit simulation package has been used for design verification its diode reverse recovery modelling technique is examined in detail, [44].

Another diode characteristic which is of importance is forward recovery. The mechanism of forward recovery and its implications in this converter are also discussed.

3.1 Power Diode Physics

Before the modeling is discussed the physics of the semiconductor diode will be reviewed.

Figure 3–1 shows important features of a n^+– p junction diode in the reverse and forward biased conditions. The following symbols are used:

n_{no}–n^+ region equilibrium electron(majority carrier)concentration

n_n – n^+ region electron (majority carrier) concentration

p_{no}– n^+ region equilibrium hole (minority carrier) concentration

p_n – n^+ region hole (minority carrier) concentration

p_{po}– p region equilibrium hole (majority carrier) concentration

p_p – p region hole (majority carrier) concentration

n_{po}– p region equilibrium electron(minority carrier)concentration

n_p – p region electron (minority carrier) concentration

The n^+ region is heavily doped as compared with the p region as displayed by the reverse biased charge concentration diagrams, in practice n_{no} can be two or three orders of magnitude greater than p_{po}. The charge concentration is presented on a logarithmic scale. Under zero bias conditions because of the charge concentration gradients holes will diffuse from the p region to the n^+ region and electrons will diffuse from the n^+ region to the p region. The diffusion current density is directly proportional to the charge concentration gradient with respect to distance, x.

$$J_{\text{diff}} = qD_p \frac{dp}{dx} + qD_n \frac{dn}{dx} \qquad 3.1\text{–}1$$

J_{diff} – Total diffusion current density

q – Electronic charge

D_p, D_n – Diffusion coefficients

p, n – Charge concentrations

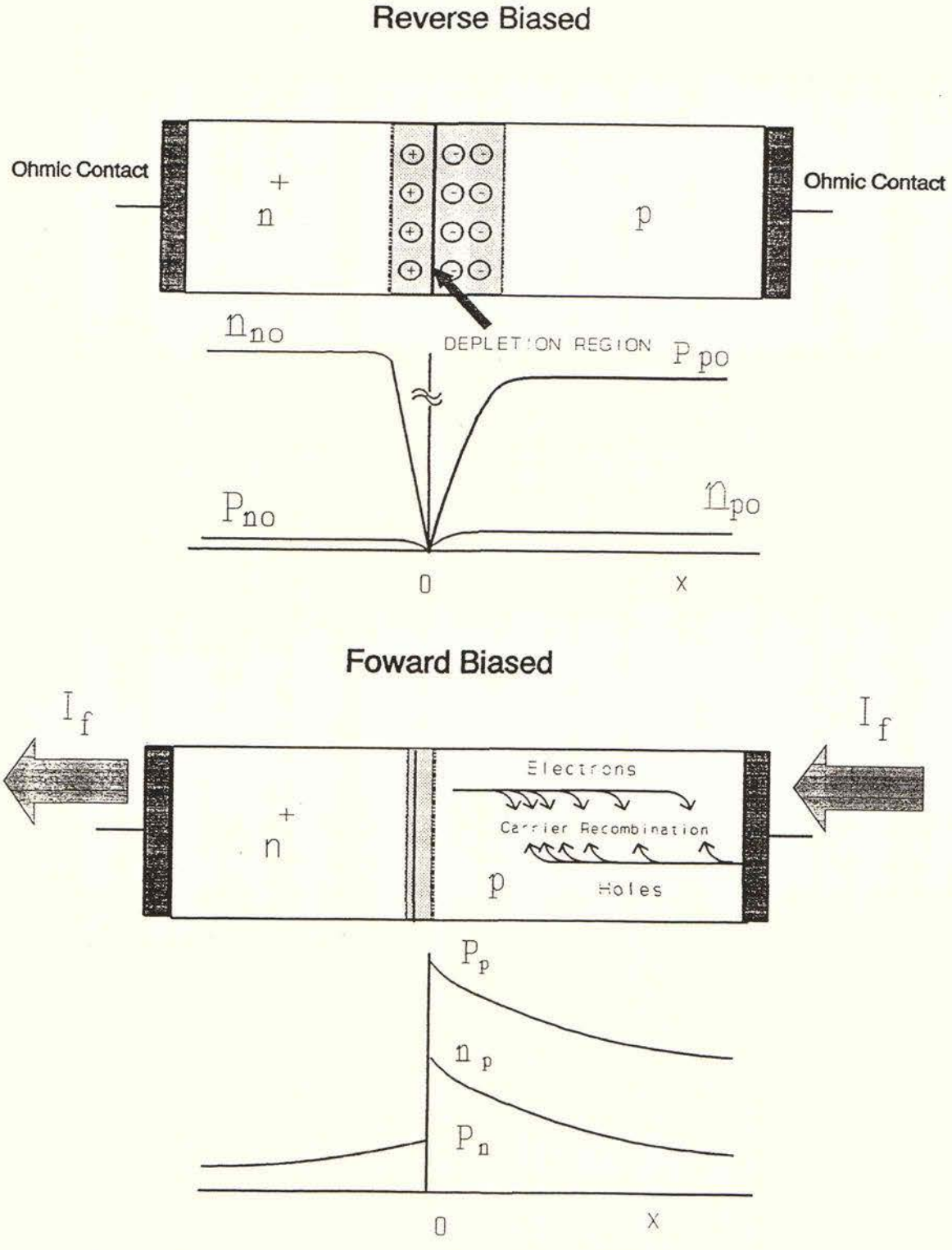


FIGURE 3-1 Reverse and Forward Bias Carrier Densities

In both cases these diffusing carriers will combine with majority carriers in the opposite region. The result is a depletion of mobile carriers in the junction area the junction area resulting in an electric field between the remaining accepter atoms in the p region and donor atoms in the n^+ region. This electric field causes a drift of charges in an opposing direction to the diffusion movement.

$$J_{drift} = q\,(\mu_p p + \mu_n n)\,E \qquad 3.1\text{–}2$$

J_{drift} – Drift current density

E – Electric field strength

μ_p, μ_n – Carrier mobility constants

A balance is reached between the drift flow (current) and the diffusion flow (current) and no net charge movement occurs. A contact potential (ϕ_0) is created across the depletion region (also known as the space charge or transition region), this can be calculated from consideration of the conditions required for charge flow balance, [23]. Application of an external reverse bias extracts majority carriers from the n^+ and p regions at the space charge boundaries expanding its width. The space charge region behaves like a capacitor with an increasing plate separation. The reverse biased diode is normally modeled by a non–linear capacitance:

$$C_{dep}(V_d) = \frac{C(0)}{\left[\,1 - \frac{V_d}{\phi_0}\,\right]^m} \qquad 3.1\text{–}3$$

$C_{dep}(V_d)$ – Depletion Capacitance

$C(0)$ – Zero Bias Capacitance ($V_d = 0$)

V_d – Diode Voltage

ϕ_0 – Contact Potential(approx. 0.5 V for power diodes)

m – Grading Coefficient

The grading coefficient depends abruptness of the junction. An abrupt junction has an $m = 1/2$ whereas a linearly graded junction has $m = 1/3$. High voltage diodes naturally tend to be fabricated with a graded junction. For diodes with $V_{rrm} >$ 500V m should be 1/3 [20–22, 28–29] manufacturers often do not quote the diode capacitance in data sheets. In the case where it is given it is often not measured at zero bias, though C(0) can easily be calculated using the above equation. When it is not given a simple rule of thumb can be used, [22–22];

$$C(0) = 12\ I_{av}(\text{rated})\ \text{pF} \qquad 3.1\text{–}4$$

This is a reasonable estimate for Fast and Ultra Fast Diodes in the $I_{av} < 100A$; $V_{rrm} <$1000V range. This is based on examination of data for many diodes. Under steady state reverse bias conditions a reverse current flows due to minority carrier flow. Because the minority carrier densities are low in the reverse biased condition this current is low except when the reverse voltage approaches the breakdown level. Reverse breakdown occurs when the electric field reaches a level at which minority carriers gain sufficient energy during the drift process to excite additional minority carriers to the conduction energy band. These in turn can excite further carriers. This is known as avalanche multiplication and the result being a sharp rise in reverse current for only small increases in voltage. If this is not limited destruction of the diode results. Some power semiconductors are designed to avalanche to a certain extent and therefore act to absorb transient turnoff energy in power electronic circuits, such a device is the Philips BYX30 fast rectifier diode, [22].

When forward bias is applied the depletion region shrinks allowing electrons from the n^+ region to spill (injected) into the p region.

In the analysis that follows it is assumed that all conduction originates from electrons transiting to the p region, this is valid because equilibrium electron concentration in the n^+ region is far higher than the equilibrium hole concentration in the p region. Once in the p region electrons become minority carriers. The minority carrier density at the transition area boundary will increase which in turn causes a concentration gradient into the p region. A minority carrier diffusion current into the p region results. Because the minority carrier concentration is now above the equilibrium level there is a natural tendency to return to equilibrium, this occurs by what is known as recombination. That is minority carriers recombine with majority carriers. The recombination rate is proportional to, the excess minority carrier concentration above the equilibrium level:

$$R_n = \frac{n_{pe}}{\tau_d} \qquad 3.1\text{–}5$$

R_n – Minority carrier concentration recombination rate

n_{pe} – Excess electron concentration in the p–region

τ_d – Excess minority carrier lifetime

The minority carrier life time represents the average time between recombinations, [23]. The excess minority carrier concentration will build up throughout the p region until a balance between injected minority carrier flow and the recombination flow is established. The minority carrier concentration from the transition boundary to the ohmic contact can be solved for using this balance condition. Where the p region, which in this case is termed the base of the diode, is long compared with the average distance travelled by a minority carrier before recombination the profile of the concentration is exponential as shown in Figure 3–1.

This can be easily understood by realising that minority carrier conduction is occurring via diffusion which is proportional to the concentration gradient. At any point this current is balanced by the recombination current which is proportional to the concentration. Therefore the concentration gradient must reduce with the concentration level which implies an exponential relationship. If the base of the diode is short compared with the minority carrier travel before recombination (short based diode) then most carriers do not recombine before reaching the ohmic contact. The minority carrier lifetime now becomes the transit time through the base region. The short based diode is assumed in the SPICE model and the minority carrier lifetime has been called the Transit Time (T_t). The carrier concentration is assumed to linearly decrease towards the ohmic contact, [23]. Real diodes will be something between the two cases, but this detailed knowledge is not necessary for our purposes. The minority carrier injection is normally classified into three levels, low level, medium level and high level. This relates to the minority carrier concentration. Low level injection is characterised by the minority carrier concentration being small compared with the majority carrier concentration. There is a strong tendency to maintain space charge neutrality in the p region which is governed by the following:

$$N_a + n_p = p_p \qquad 3.1\text{–}6$$

N_a – Accepter atom concentration

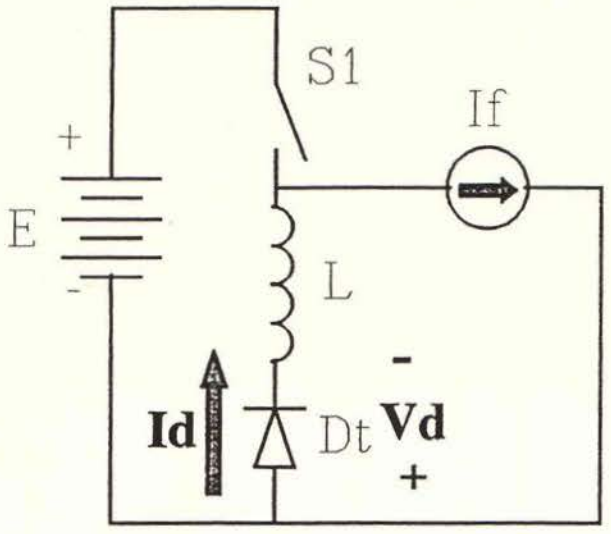
Since $n_p << N_a$ for low level injection the effect of increases in n_p on p_p are neglected. Of cause what actually happens is there is a tendency for the increased minority carrier profile to be matched by an increased majority carrier profile. This is driven by an electric field in the p region directed towards the n^+ region. A drift of holes occurs towards the transition region to balance the charge from the injected electrons. Some equilibrium field and majority carrier concentration is reached.

The electric field gives rise to an voltage drop which adds with the contact potential to produce the total diode forward drop. For low level injection these effects are very small and are neglected. However as the forward current and hence the injection level increases, the majority carrier concentration increases significantly. Tied to this is an increase in the electric field and hence forward voltage drop. High level injection is characterised by a minority carrier concentration approaching that of the majority carriers and the majority carrier concentration significantly increasing above the equilibrium value, ie excess holes in the p region. Power diodes operate at high injection levels and hence exhibit significant forward voltage drop in addition to the contact potential. They are generally modeled as an ideal diode in series with a resistance. However this resistance is not the bulk resistance of the semiconductor which is many times higher. In the high level injection condition the large number of excess holes in the p region act to increase the conductivity. This is termed conductivity modulation, [29].

3.2 Power Diode Turn Off Characteristics

The important feature of the switch off process is the reverse recovery period. During the commutation process the forward current is reduced to zero followed by a short period for which a reverse current flows. The function of the reverse current is to re–establish charge equilibrium conditions within the semiconductor. No reverse voltage can be supported until this occurs. Until this time reverse current is therefore determined by external circuit elements. Figure 3.2(a) shows a Buck Converter. With switch S_1 open assume a steady state current of I_f flows in the inductor and diode. The inductance, L, limits the diode $\frac{dI_d}{dt}$ during commutation. With closure of S_1 voltage E is applied across L causing I_d to decay at a rate of:

$$\frac{dI_d}{dt} = \frac{E}{L} \qquad 3.2\text{–}7$$



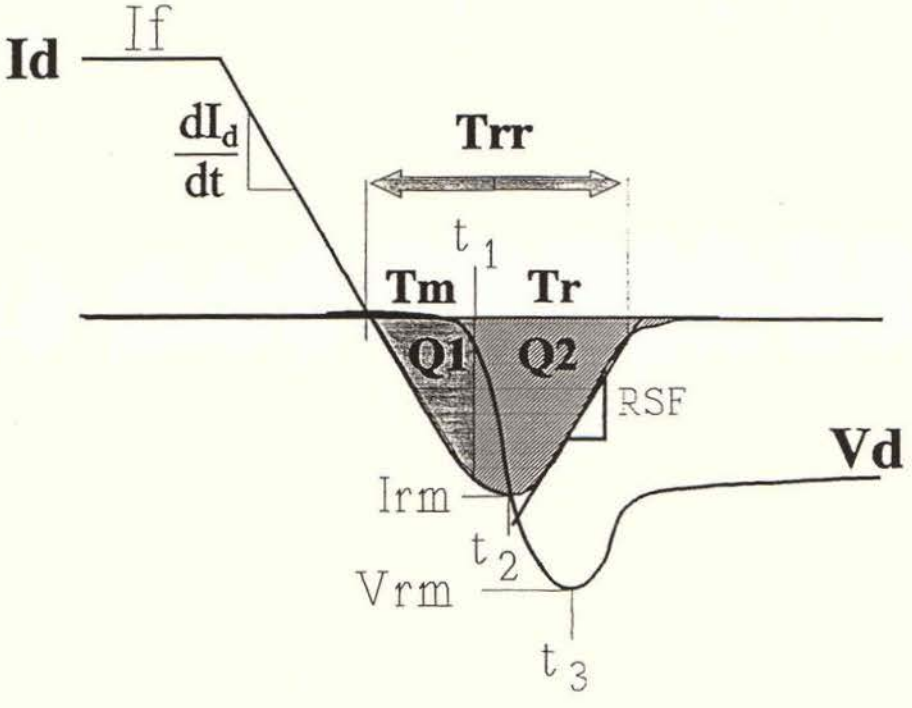


Figure 3-2 Power Diode Reverse Recovery Transient

The diode current reaches zero and then rises in the reverse direction. At time t_1 the diode begins to support reverse voltage and the $\frac{dI_d}{dt}$ begins to decline. Shortly after this at t_2 the reverse current reaches a peak and begins to decline. At this point the diode supports the supply voltage E. As the reverse current decays the diode reverse voltage rises above the supply voltage and peaks at t_3. This period is known as "snap off" and the peak reverse voltage is determined by the maximum rate of decay of current. The maximum reverse current and snap off characteristics are functions of both the diode and the external circuit elements. External snubbing networks, for example, influence the snap off period.

The reverse recovery behavior of the P–N junction diode can be modeled using charge control theory, [27]. The charge control relationship will now be discussed.

If steady state conditions are assumed and all minority carriers are recombining then:

$$I_d = \int R_n \, .d\nu \qquad 3.2\text{–}1$$

$$Q_d = \int n_{pe} \, .d\nu \qquad 3.2\text{–}2$$

I_d – Diode forward current

Q_d – Stored excess minority charge in n region

ν – Volume of semiconductor material

From equations 3.1–5, 3.2–1 and 3.2–2 it follows that:

$$I_d = \frac{Q_d}{\tau_d} \text{ or } Q_d = I_d . \tau_d \qquad 3.2\text{–}3$$

This is a significant result showing that the excess stored charge is proportional to the forward current. Under high levels of injection and/or short based diodes the assumption that all current flowing due to recombination is not valid. This though does not effect the general concept. It does however effect the value τ_d. The lifetime is a function of current but can be assumed to be constant to simplify the analysis without excessive inaccuracy, [24]. The dynamic relationship between Q_d and I_d can be deduced by considering I_d changing from I_{d1} to I_{d2} in time δt. Then the total charge movement through the diode is:

$$\delta Q = \left[\frac{I_{d1} + I_{d2}}{2}\right] \delta t + \delta Q_d \qquad 3.2\text{–}4$$

Now since:

$$I_{d1} = \frac{Q_{d1}}{\tau_d}$$

$$I_{d2} = \frac{Q_{d2}}{\tau_d}$$

Substituting into equation 3.2–4

$$\delta Q = \left[\frac{Q_{d1} + Q_{d2}}{2\tau_d}\right] \delta t + \delta Q_d$$

As δt becomes small:

$$Q_{d1} = Q_{d1} = Q_d$$

$$dQ = \frac{Q_d}{\tau_d} dt + dQ_d$$

Differentiating:

$$\frac{dQ}{dt} = \frac{Q_d}{\tau_d} + \frac{dQ_d}{dt} \qquad 3.2\text{–}5$$

$$I_d = \frac{Q_d}{\tau_d} + \frac{dQ_d}{dt} \qquad 3.2\text{–}6$$

This is known as the fundamental charge control equation for the p–n junction, [28]. However charge flow due to expansion or retraction of the depletion region has not been considered in this equation. This is equivalent to charging and discharging the depletion capacitance. This effect can be neglected so long as the diode is forward biased but during commutation when the reverse voltage increases the charge control equation must be modified, [24]:

$$I_d = \frac{Q_d}{\tau_d} + \frac{dQ_d}{dt} - \frac{d[C_{dep}(V_d)\ V_d]}{dt} \qquad 3.2\text{–}7$$

Notice since $C_{dep}(V_d)$ is a function of V_d, it is included in the differential. This capacitive displacement current influences the behavior of the diode during the "snap off" period. Equation 3.2–6 can be used to model the diode to the point where reverse voltage begins to be supported.

The SPICE large signal modeling technique in reference to the diode turn off characteristics will now be discussed. Equations relating the reverse recovery performance in relation to circuit parameters and the minority carrier lifetime will be derived. However research has shown that the modeling technique used in SPICE does not represent the true process. Never the less it is important to establish the relationships so that they can be applied to simulation parameter setting. At the end of the section the true reverse recovery mechanism is discussed.

The relevant equations are also derived. These second set of equations are found to be similar in structure to those that apply to the SPICE diode model. In both cases the equations are implicit, requiring either a lookup table or a graphical means to solution, both are presented.

The large signal model used by SPICE is shown in Figure 3.3, [23]. A voltage dependent current source (I_d) is connected in parallel with a voltage dependent capacitor (C_d). The capacitor charge at low V_d is modeled as follows, [23]:

$$Q_d = \tau_d I_d + C_d(0)\int_0^{V_d}\left[1 - \frac{V_d}{\phi_0}\right] dV_d \qquad 3.2\text{–}8$$

For a diode I_d is related to V_d as follows, [23]:

$$I_d = \eta I_o e^{\left[\frac{V_d}{\eta \kappa_t} - 1\right]} \qquad 3.3\text{–}9$$

I_0 – Reverse saturation current

η – Constant dependent on the injection level

κ_t – Thermal voltage ($\approx$ 26 mV @ 300^0 K)

For high forward current (normal for power diodes) the first term of equation 3.2–8 dominates:

$$Q_d = \tau_d I_d \qquad 3.2\text{–}10$$

Consider a reduction in forward current from I_{a1} to I_{a2}. Assuming equilibrium conditions exist at I_{q1} then $I_d = I_{a1}$; V_d and Q_d would be determined by I_d via equations 3.2–8 and 3.2–9.

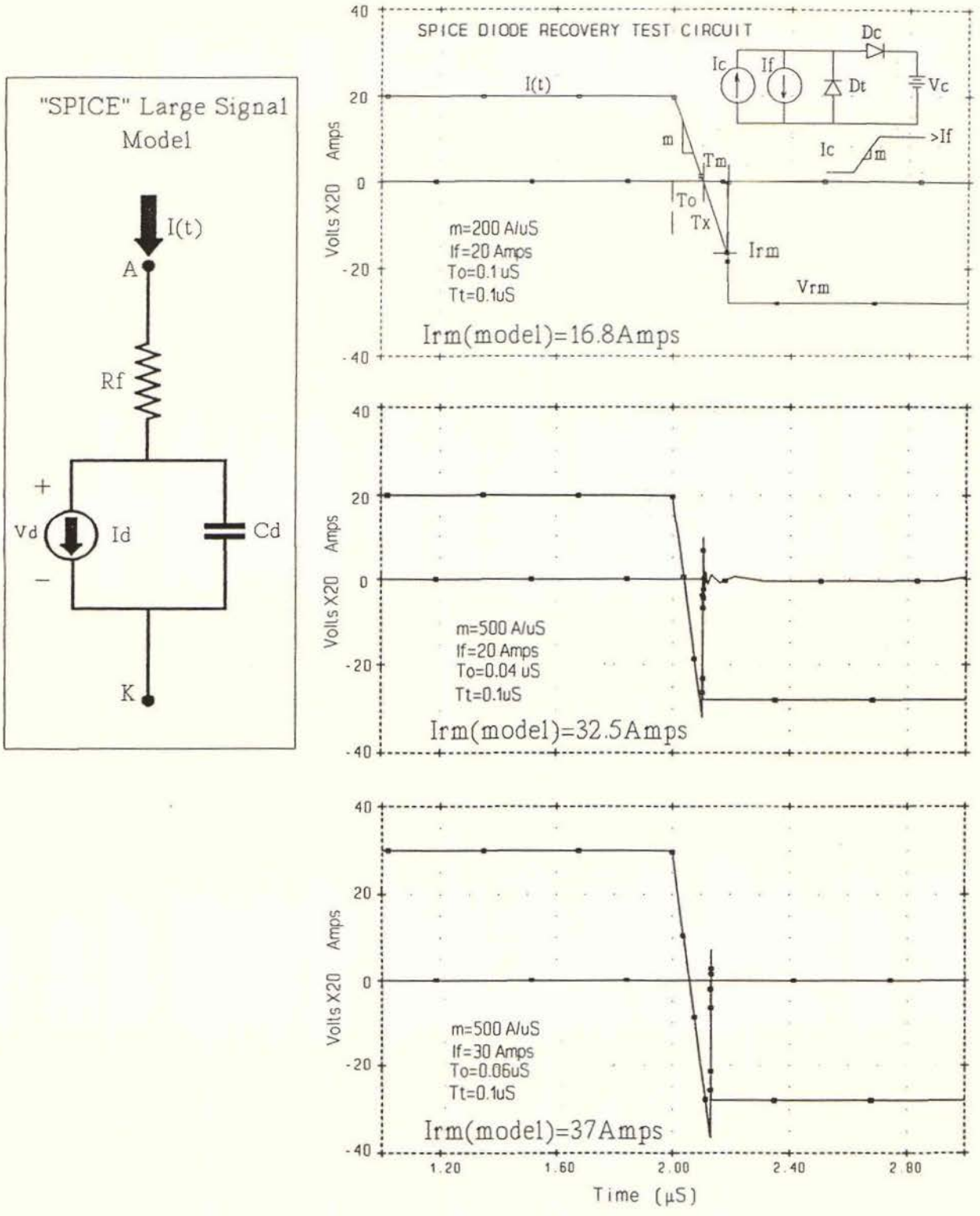


Figure 3.3 Spice Simulation of Reverse Recovery

The excess stored charge at a forward current of I_{a1} would be given by:

$$Q_{d1} = \tau_d I_{a1} \qquad 3.2\text{–}11$$

An instantaneous reduction in I_a would cause no initial change in Q_d and hence V_d and I_d are initially unchanged. As time proceeds a current $(I_d - I_{a2})$ flows to discharge C_d until I_d is again equal to I_a. Stored excess charges recombine until the forward current is again just supported. During the commutation process no reverse voltage across C_d is supported until Q_d is reduced to zero. After this the reverse voltage builds up rapidly as dictated by equations 3.2–8 and 3.2–9. If the commutation dI_d/dt is low compared with the rate of change of the recombination current, dR_n/dt. The lag in removal of stored charge is small and the diode will recover without significant reverse sweepout current. However if the dI_d/dt is much higher there will be a large amount of stored charge at the time when the diode current is reduced to zero.

This stored charge can support a reverse current (therefore no reverse voltage can be supported) which combines with the recombination process to reduce Q_d to zero. The reverse current builds up at the rate determined by the external inductance and commutating voltage until Q_d is reduced to zero. At this time reverse voltage is supported. However due to the charging of the depletion capacitance up to the commutating voltage the current peaks at a slightly higher reverse current then this. The switch S1 of Figure 3.2 has to carry the reverse current, which is one undesirable effect of reverse recovery. It should also be pointed out that incorrectly designed R–C snubbers will tend to augment the diode depletion capacitance and increase the peak current seen by the switch. Using equation 3–10 and $I_d(0)=I_f$ and a commutating $dI_d/dt = m$ the time required to reduce the excess stored charge to zero can be solved for as follows. The initial excess stored charge from equation 3.2–3 is:

$$Q_d(0) = I_f \tau_d \qquad 3.2\text{–}12$$

The current during the interval is forced to be:

$$I_d(t) = -mt + I_f \qquad 3.2\text{–}13$$

I_f – Steady state forward current before commutation

m – Rate of decay of current $\left[\frac{dI_d}{dt}\right]$

From equations 3.2–6 and 3.–13:

$$-mt + I_f = \frac{Q_d(t)}{\tau_d} + \frac{dQ_d(t)}{dt} \qquad 3.2\text{–}14$$

Solving this linear first order differential equation yields, [47]:

$$Q_d(t) = ke^{\left[\frac{-t}{\tau_d}\right]} + -m\tau_d\, t + m\tau_d^2 + I_f\tau_d \qquad 3.2\text{–}15$$

k – integration constant

Using equation 3.2–12, k can be determined:

$$k = -m\tau_d^2 \qquad 3.2\text{–}16$$

Therefore by substitution into equation 3.2–15:

$$Q_d(t) = -m\tau_d^2 e^{\left[\frac{-t}{\tau_d}\right]} + -m\tau_d\, t + m\tau_d^2 + I_f\tau_d \qquad 3.2\text{–}17$$

Solving for $Q_d(t) = 0$ and replacing t by T_x (Reverse blocking time) results in:

$$\frac{I_f}{m} = T_x - \tau_d\left[1 + e^{\left[\frac{-T_x}{\tau_d}\right]}\right] \qquad 3.2\text{–}18$$

This equation cannot be directly solved for T_x, therefore an indirect method for determining T_x is proposed. The following symbology will be used:

$$T_0 = \frac{I_f}{m} \qquad 3.2\text{–}19$$

$$T_x = \frac{I_f + I_{rm}}{m} \qquad 3.2\text{–}20$$

$$T_m = \frac{I_{rm}}{m} \qquad 3.2\text{–}21$$

$$T_x = T_0 + T_m \qquad 3.2\text{–}22$$

T_0 – Forward Current Decay Time

T_x – Reverse Blocking Time

T_m– Reverse Current Rise Time

I_{rm} – Peak reverse current during recovery

These are described in Figure 3.4. Therefore substituting equations 3.2–19 and replacing τ_d by T_t (the SPICE Transit time parameter) equation 3.2–18 can be written as:

$$\frac{T_0}{T_t} = \frac{T_x}{T_t} - \left[1 - e^{\left[\frac{-T_x}{T_t}\right]}\right] \qquad 3.2\text{–}23$$

And by substitution of 3.2–22 into 3.2–23:

$$\frac{T_m}{T_x} = \frac{T_t}{T_x}\left[1 - e^{\left[\frac{-T_x}{T_t}\right]}\right] \qquad 3.2\text{–}24$$

Equation 3.2–24 can be used to determine an approximate value for the Transit Time from manufacturer's data. The equation 3.2–23 can then be used to predict the reverse recovery characteristics for other operating conditions. The ratio T_m/T_x of equation 3.2–24 can be found using manufacturer's data:

$$\frac{T_m}{T_x} = \frac{I_{rm}}{I_f + I_{rm}} \qquad 3.2\text{–}25$$

Equation 3.2–24 can be solved by the use of the nomogram in Figure 3.4 The nomogram simply displays the relationship on log–log scales allowing T_t/T_x to be found. This could be done equally well using a a look up table. The reverse blocking time T_x is also available from the data sheet:

$$T_x = \frac{I_f + I_{rm}}{m} \qquad 3.2\text{–}26$$

In some data sheets the Recovered Charge will be given. In this case it is important to determine if Q_1,Q_1 and Q_2 or Q_1+ Q_2 of figure 3.4 are given:

Q_1 – the lag charge denoted Q_s

Q_2 – the residual charge denoted Q_f

Q_1+ Q_2 – the reverse recovery charge denoted Q_{rr}

If Q_1 is given the following can be applied to find I_{rm}:

$$I_{rm} = \sqrt{2\ Q_1\ m} \qquad 3.2\text{–}27$$

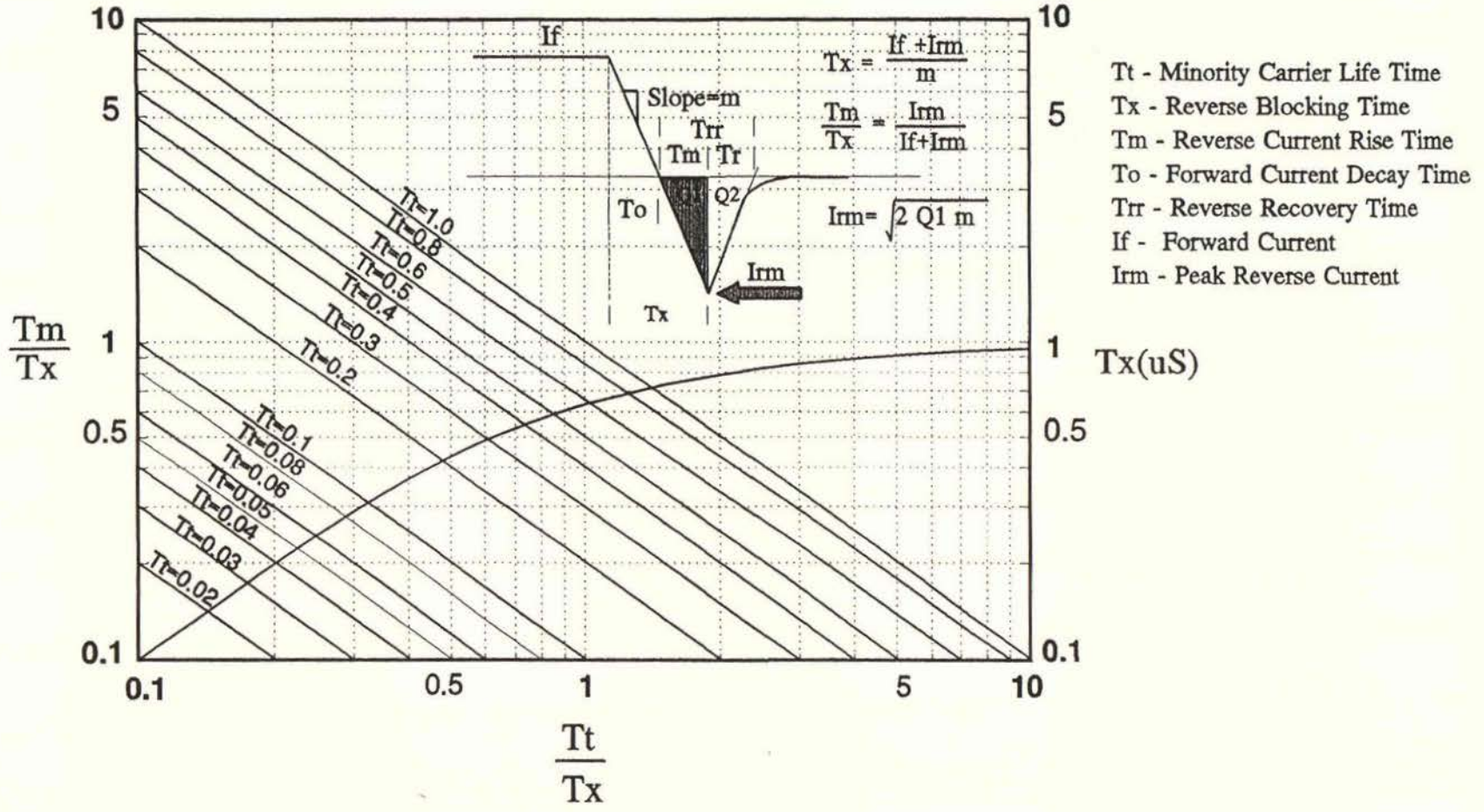


Figure 3.4 Minority Carrier Life Time According to SPICE using Manufacturers Data

If Q_{rr} is assumed to be split evenly between Q_1 and Q_2 (which is the case for most soft recovery diodes), [34]:

$$I_{rm} = \sqrt{Q_{rr}\ m} \qquad 3.2\text{–}28$$

Some data sheets may give Q_{rr} and the Reverse Snap off Factor (RSF) as illustrated in Figure 3–1, [25]:

$$RSF = \frac{T_m}{T_r} = \frac{Q_2}{Q_1} \qquad 3.2\text{–}29$$

$$Q_1 = \frac{Q_{rr}}{1 + RSF} \qquad 3.2\text{–}30$$

Having found T_t/T_x from the nomogram and T_x from 3.2–26 the minority carrier lifetime determined. As an aid T_x has been plotted against T_t/T_x for constant values of T_t so that that the result can be obtained visually. A nomogram, shown in Figure 3.5, has also been formulated for equation 3.2–23, this can be used to estimate T_x and therefore I_{rm} for any forward current and commutating dI/dt. The procedure is to calculate the forward current decay time (T_o):

$$T_0 = \frac{I_f}{m} \qquad 3.2\text{–}31$$

Using the ratio T_o/T_t the ratio T_x/T_t is found and hence I_{rm} is determined:

$$I_{rm} = m\ T_x - I_f \qquad 3.2\text{–}32$$

The above analysis is based on the SPICE model of Figure 3.2. Three simulation runs were done using the circuit shown with a test diode (D_t) with a Transit Time of 0.1μS to verify the model.

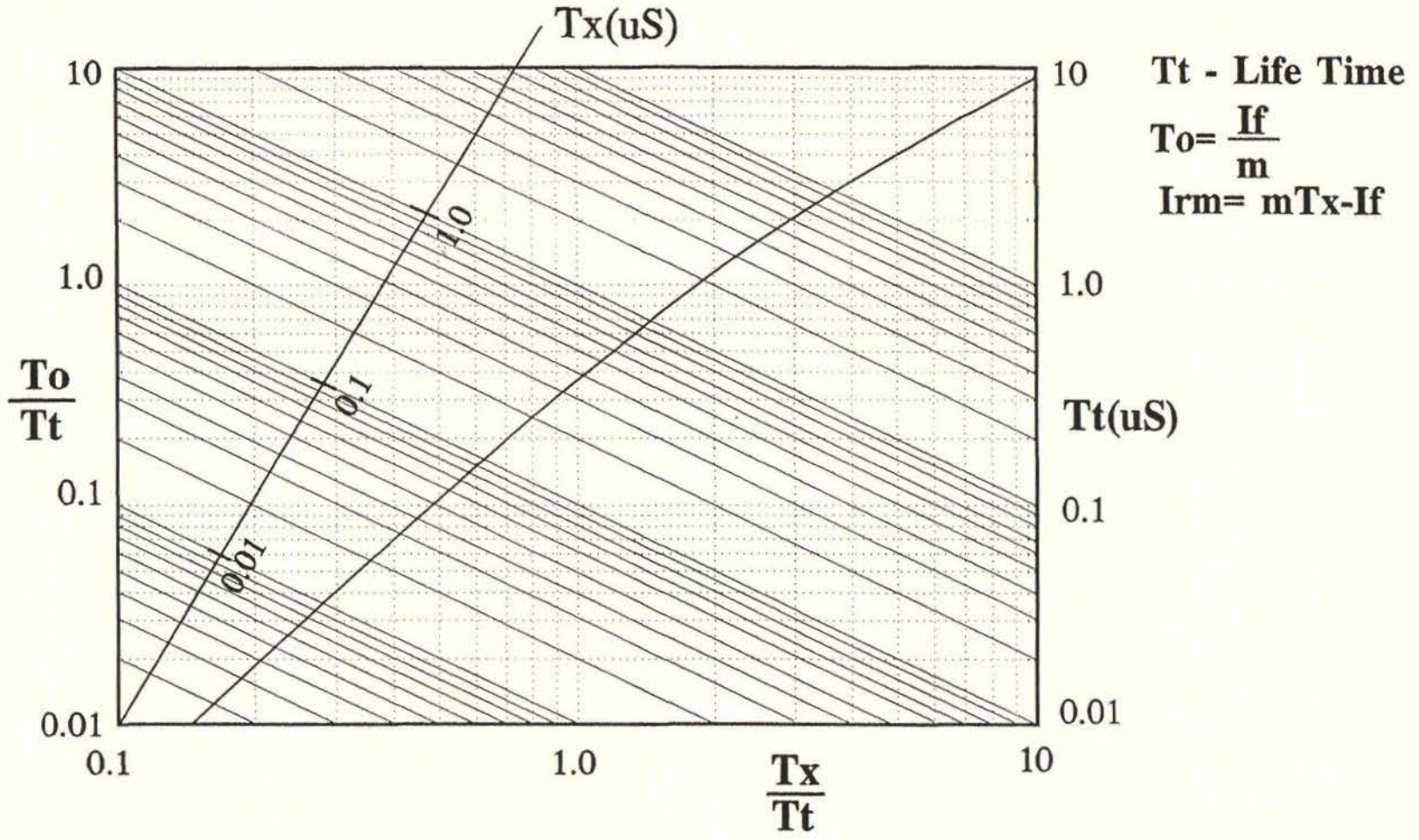


Figure 3.5 Determination of Irm According to SPICE

The zero bias capacitance was set to zero to eliminate the effects of the depletion capacitance charge current. As indicated the peak reverse currents were consistent with the model. The SPICE model however does not represent the true reverse recovery mechanism. The SPICE model assumes that the reverse current can continue to increase until the total stored charge is removed. In reality the reverse current can only rise at a steady rate while it is being supported by a sufficiently high minority carrier concentration near the transition region boundary. At some time the concentration is insufficient and the rate of rise of reverse current reduces. At the same time the reverse voltage begins to rise. The actual peak reverse current attained will depend on the depletion capacitance characteristics and external components. The important point is that not all the stored charge is removed at the time of peak reverse current. This effect is amplified at high commutation dI/dt as Figure 3–6 illustrates. The p region excess minority carrier concentration at steady state and at several instants during commutation for high and low dI/dt recoveries are shown. Minority carrier conduction is dominated by diffusion and for the p region from equation 3.1–1:

$$J_{\mathrm{diff}} = q\, D_{\mathrm{n}} \frac{\mathrm{d}n_{\mathrm{p}}}{\mathrm{d}x} \qquad 3.2\text{–}33$$

The diffusion current is directed from areas of high to areas of low charge concentration. Because the conduction is only via minority carrier diffusion at the edge of the transition area (x=0) it follows that the concentration gradient there is determined by the diode current. Hence after period T_0 when the current has decayed to zero the gradient at x=0 will also be zero as indicated in Figure 3.6. After this time the current reverses and hence the slope reverses. At the end of period T_m, neglecting depletion capacitance effects, the maximum reverse current is attained which corresponds to the maximum reverse gradient and the concentration reaching zero at the transition region boundary. The charge Q_1 (lag Charge) is removed during T_m and Q_2 (Residual Charge) remains,to be removed during T_r.

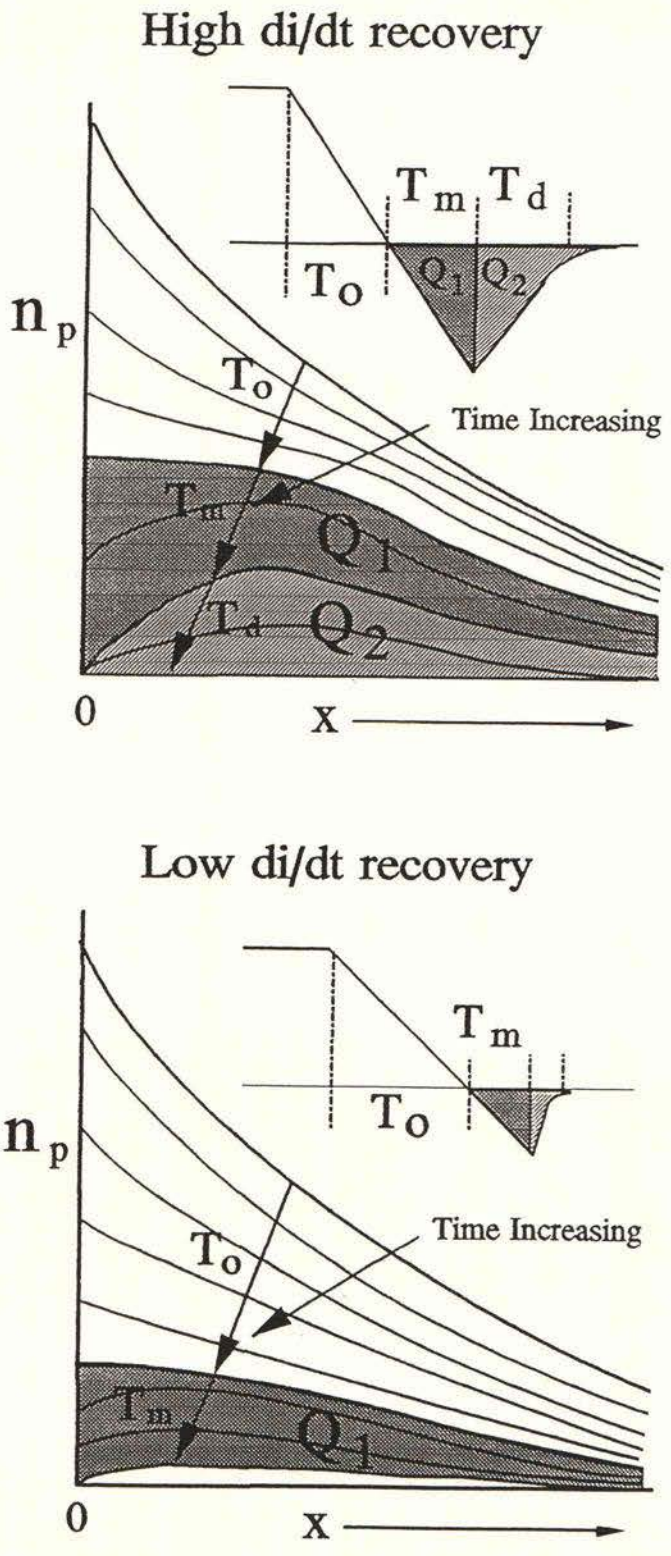


Figure 3.6 Excess Minority Carrier Concentration During Reverse Recovery

The switching loss can be attributed to the removal of Q_2. When a high commutation dI/dt is applied the minority carriers are quickly swept back across the transition region causing a depletion nearby, but in the middle regions carriers are removed by recombination and flow by diffusion which can be a much slower process. It is this time lag that causes the residual charge Q_2. It should also be noted that some of the initial stored charge is removed during T_0 due to recombination. In the case of the low dI/dt recovery more charge is removed during T_0 and T_m due simply to the increased time available for recombination to occur. If the dI/dt is low enough the diode would be able to almost attain its equilibrium state throughout the forward current decay and the reverse recovery would be virtually non–existent Use of higher dI/dt results in increased reverse current and increased residual charge (Q_2).

Relationships allowing the calculation of I_{rm} from limited manufacturers data taking into account the existence of the residual charge will now be derived. The value of I_{rm} is determined by the constraint that the reverse current must be sustained by adequate minority charge. During the commutation the reverse current is increasing while the excess minority charge is being reduced. The excess minority charge is determined by the charge control equation. The diode is in the forward biased state. The associated time constant will be denoted the forward biased minority carrier lifetime, τ_f. A point is reached where further increase in reverse current is not possible and snap off commences. At snap off reverse bias is established and current decays to zero. The diode now enters the reverse biased state. The excess charge during snap off is constrained to be proportional to the reverse current, [28]. The proportionality constant is the reverse biased minority carrier lifetime. This implies that:

$$Q_d(T_x) = I_{rm}\,\tau_r \qquad 3.2\text{–}34$$

τ_r – Reverse biased minority carrier lifetime

The ratio of the forward lifetime to the reverse lifetime, τ_f/τ_r, is a characteristic of the diode. To solve for T_x under the condition specified in equation 3.2–34 equation 3.2–17 will be used with τ_d being replaced by τ_f:

$$I_{rm}\tau_r = -m\tau_f{}^2 e^{\left[\frac{-T_x}{\tau_f}\right]} + -m\tau_f T_x + m\tau_f{}^2 + I_f\tau_f \qquad 3.2\text{–}35$$

Which can be reduced to:

$$\frac{I_f}{m}\frac{\tau_r}{\tau_f} = -\tau_f e^{\left[\frac{-T_x}{\tau_f}\right]} + -T_x + \tau_f + \frac{I_f}{m}$$

Let $\alpha = \frac{\tau_f}{\tau_r}$ and using 3.2–19 and 3.2–21

$$\frac{T_m}{\alpha} = -\tau_f e^{\left[\frac{-T_x}{\tau_f}\right]} + -T_x + \tau_f + T_0$$

Using equation 3.2–22 and replacing τ_f by T_t to be consistent with the original analysis the following equations can be written:

$$\frac{T_0}{T_t} = \frac{T_x}{T_t} - \frac{\alpha}{1+\alpha}\left[1 - e^{\left[\frac{-T_x}{T_t}\right]}\right] \qquad 3.2\text{–}36$$

$$\frac{T_m}{T_x} = \frac{\alpha}{1+\alpha}\frac{T_t}{T_x}\left[1 - e^{\left[\frac{-T_x}{T_t}\right]}\right] \qquad 3.2\text{–}37$$

The equations are only different from 3.2–23 and 3.2–24 by the factor $\frac{\alpha}{1+\alpha}$. It is known for power diodes that α is about 4, [24]. Therefore:

$$\frac{T_0}{T_t} = \frac{T_x}{T_t} - 0.8\left[1 - e^{\left[\frac{-T_x}{T_t}\right]}\right] \qquad 3.2\text{–}38$$

$$\frac{T_m}{T_x} = 0.8\,\frac{T_t}{T_x}\left[1 - e^{\left[\frac{-T_x}{T_t}\right]}\right] \qquad 3.2\text{–}39$$

Nomograms for these modified equations have also been constructed and are displayed in Figures 3.7 and 3.8. These can be used in exactly the same manner as previously. The relationships have also been displayed in tabular form in Table 3.1.

Figure 3.9 shows a comparison of the I_{rm} versus dI/dt relationship for a commercial Ultra Fast Recovery Diode, BYT30 PI–1000, [20] and that predicted by equation 3.2–38 using equation 3.2–39 to estimate the T_t parameter from data at the point marked "A". The modified model is shown to be very accurate for this diode. Diodes of various sizes from other manufacturers for which there has been sufficient data have also been tried. The model proved to be accurate for predicting I_{rm} for varying dI/dt and forward current.

The relationship between T_x/T_t and T_o/T_t displayed in Figure 3.8 on a log–log scale is approximately linear. This means that the the following approximate equation can be written:

$$\frac{T_o}{T_t} = C\left[\frac{T_x}{T_t}\right]^n \qquad 3.2\text{–}40$$

n – slope of the log–log relationship

C – constant

This allows an approximate function relating I_{rm} to m, I_f and T_t to be derived. This relationship is found to be useful in the design process and is used in Chapter Four.

Substituting equations 3.2–19 and 3.2–20 gives:

$$I_{rm} = C^{-\frac{1}{n}} T_t^{(1-\frac{1}{n})} m^{(1-\frac{1}{n})} I_f^{\frac{1}{n}} - I_f \qquad 3.2\text{–}41$$

The value of n is found from evaluation of the slope in Figure 3.8 to be 1.36. Also $T_o/T_t = 0.49$ at $T_x/T_t = 1$ which means $C = 0.49$.

The minority carrier lifetime for power diodes is known to increase with temperature. It is therefore necessary to consider the influence of junction temperature in the calculation of I_{rm}. In practice it has been found that the maximum reverse recovery current increases almost linearly with temperature over the range of 25^oC to 125^oC and is known to double for a 100^oC increase in junction temperature, [35]. Using this information the following equation can be written:

$$I_{rm}(T_{j2}) = I_{rm}(T_{j1}) \left[1 + \frac{T_{j2} - T_{j1}}{100}\right] \qquad 3.2\text{–}42$$

The transit time for the DSE60–10A diodes can now be determined using table 3.1 and manufacturer's data: $I_{rm} = 32$ Amps @ $I_f = 60$ Amps; $m = 480$ Amps/μS; $T_j = 100^oC$.

The relationship will be evaluated at $T_j = 125^oC$ hence equation 3.2–42 will be used to find I_{rm} for this temperature:

$$I_{rm}(T_{j2}) = I_{rm}(T_{j1}) \left[1 + \frac{T_{j2} - T_{j1}}{100}\right]$$

$$I_{rm}(125) = 32 \times \left[1 + \frac{125 - 100}{100}\right] = 40 \text{ Amps}$$

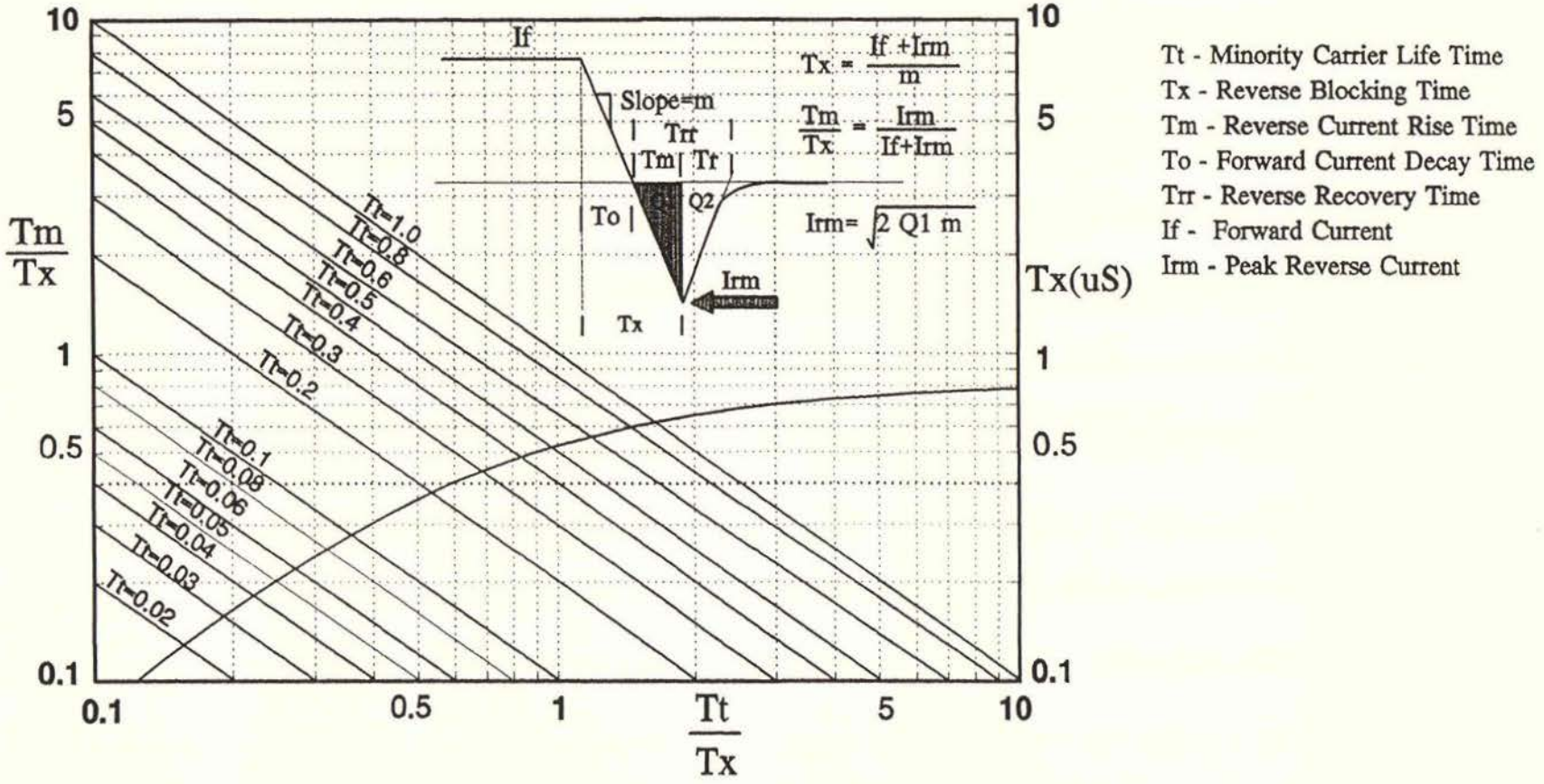


Figure 3.7. Minority Carrier Life Time According to Modified Model using Manufacturer's Data

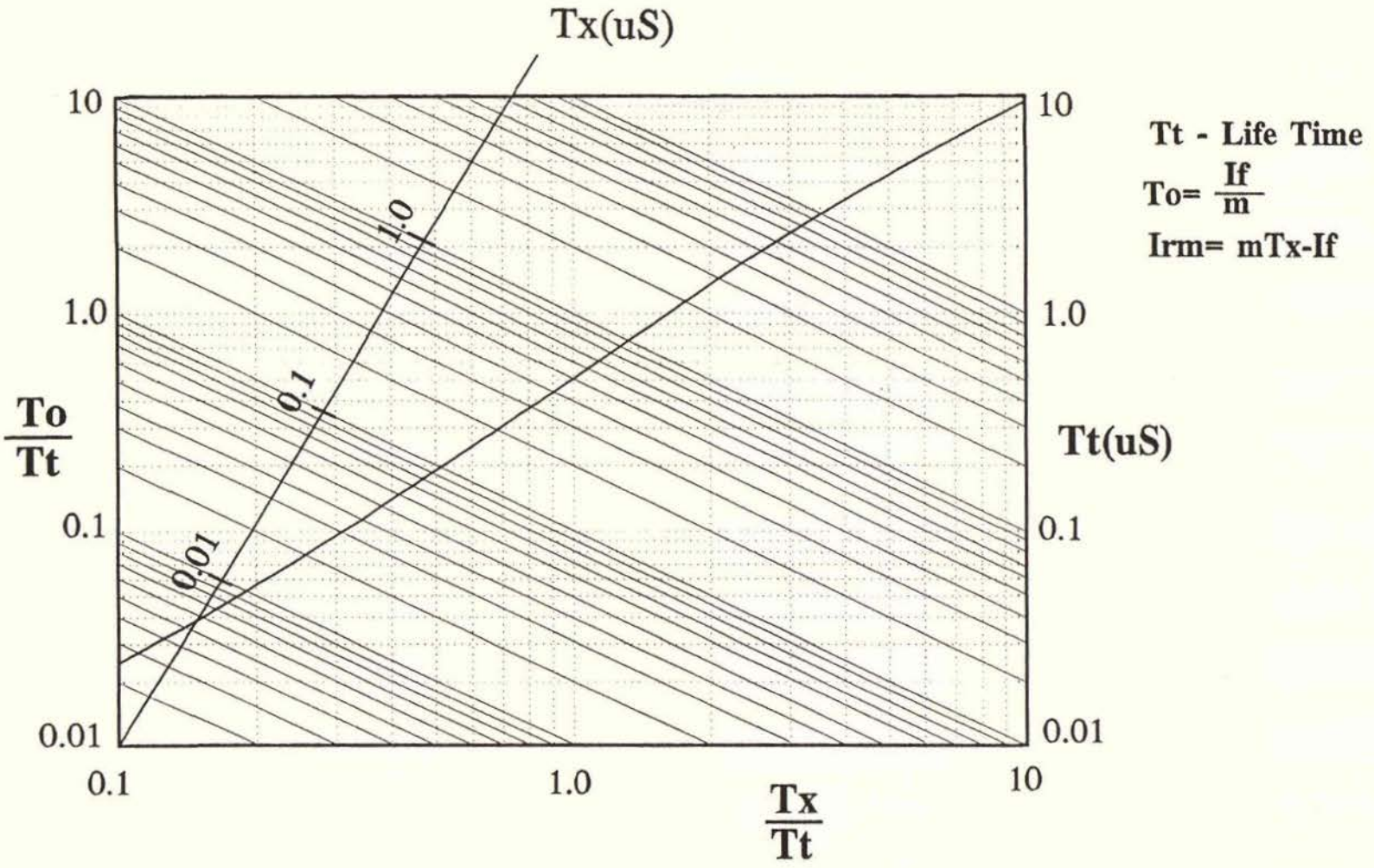


Figure 3.8 Determination of Irm Using Modified Model

$\frac{T_x}{T_t}$	$\frac{T_m}{T_x}$	$\frac{T_o}{T_t}$	$\frac{T_x}{T_t}$	$\frac{T_m}{T_x}$	$\frac{T_o}{T_t}$
0.10	0.76	0.02	1.00	0.51	0.49
0.12	0.75	0.03	1.20	0.47	0.64
0.14	0.75	0.04	1.40	0.43	0.80
0.16	0.74	0.04	1.60	0.40	0.96
0.18	0.73	0.05	1.80	0.37	1.13
0.20	0.73	0.05	2.00	0.35	1.31
0.22	0.72	0.06	2.60	0.28	1.86
0.28	0.70	0.08	2.80	0.27	2.05
0.30	0.69	0.09	3.00	0.25	2.24
0.32	0.68	0.10	3.20	0.24	2.43
0.34	0.68	0.11	3.40	0.23	2.63
0.36	0.67	0.12	3.60	0.22	2.82
0.38	0.67	0.13	3.80	0.21	3.02
0.40	0.66	0.14	4.00	0.20	3.21
0.42	0.65	0.15	4.20	0.19	3.41
0.44	0.65	0.16	4.40	0.18	3.61
0.46	0.64	0.17	4.60	0.17	3.81
0.48	0.64	0.18	4.80	0.17	4.01
0.50	0.63	0.19	5.00	0.16	4.21
0.52	0.62	0.20	5.20	0.15	4.40
0.54	0.62	0.21	5.40	0.15	4.60
0.56	0.61	0.22	5.60	0.14	4.80
0.58	0.61	0.23	5.80	0.14	5.00
0.60	0.60	0.24	6.00	0.13	5.20
0.62	0.60	0.25	6.20	0.13	5.40
0.64	0.59	0.26	6.40	0.12	5.60
0.66	0.59	0.27	6.60	0.12	5.80
0.68	0.58	0.29	6.80	0.12	6.00
0.70	0.58	0.30	7.00	0.11	6.20
0.72	0.57	0.31	7.20	0.11	6.40
0.74	0.57	0.32	7.40	0.11	6.60
0.76	0.56	0.33	7.60	0.11	6.80
0.78	0.56	0.35	7.80	0.10	7.00
0.80	0.55	0.36	8.00	0.10	7.20
0.82	0.55	0.37	8.20	0.10	7.40
0.84	0.54	0.39	8.40	0.10	7.60
0.86	0.54	0.40	8.60	0.09	7.80
0.88	0.53	0.41	8.80	0.09	8.00
0.90	0.53	0.43	9.00	0.09	8.20
0.92	0.52	0.44	9.20	0.09	8.40
0.94	0.52	0.45	9.40	0.09	8.60
0.96	0.51	0.47	9.60	0.08	8.80
0.98	0.51	0.48	9.80	0.08	9.00
1.00	0.51	0.49	10.00	0.08	9.20

TABLE 3.1 POWER DIODE REVERSE RECOVERY LOOKUP TABLE

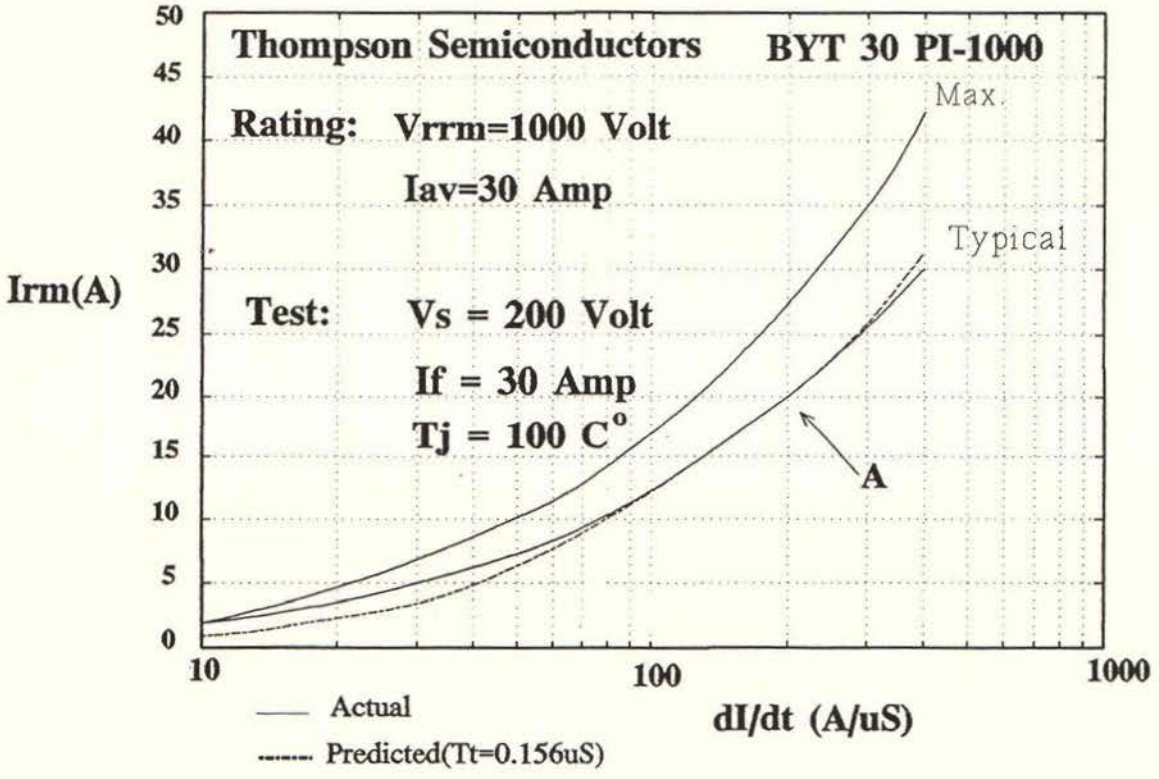


Figure 3.9 Commercial Diode Versus Model Comparison

From equation 3.2–25 T_m/T_x is calculated:

$$\frac{T_m}{T_x} = \frac{I_{rm}}{I_f + I_{rm}} = \frac{40}{60 + 40} = 0.4$$

From Table 3.1 T_x/T_t for $T_m/T_x = 0.4$ is found to be 1.6. The value of T_t using equation 3.2–20 will be given by:

$$T_t = \frac{T_t}{T_x} \frac{I_f + I_{rm}}{m}$$

$$T_t = 0.625 \times \frac{60 + 40}{480} = 0.13\ \mu S$$

Substituting T_t, C and n into equation 3.2–41 yields:

$$I_{rm} = C^{-\frac{1}{n}} T_t^{(1-\frac{1}{n})}\, m^{(1-\frac{1}{n})}\, I_f^{\frac{1}{n}} - I_f$$

$$I_{rm} = 1.69 \times 0.583 \times m^{0.265} I_f^{0.735} - I_f$$

$$I_{rm} = 0.985\, m^{0.265} I_f^{0.735} - I_f$$

$$I_{rm} \approx m^{0.265} I_f^{0.735} - I_f \quad @\ T_j = 125^0C \qquad 3.2–43$$

This relationship gives valid results when T_x/T_t is in the range of 0.3 to 3. This relationship will be used in Chapter Four. The object of finding the peak reverse current and the recovered charge is to evaluate the peak current stress on other devices and the reverse recovery power loss for the diode.

The reverse recovery loss will now be considered. The power dissipation during the reverse recovery period will be given by:

$$P_{rr} = f_s \int_0^{T_{rr}} V_d(t)\, I_d(t)\ dt \qquad 3.2\text{–}44$$

P_{rr}– Reverse recovery power loss

T_{rr} – Reverse recovery Time ($T_m + T_d$)

f_s – Switching frequency

In this case both V_d and I_d are functions of time.

$$I_d = \frac{dQ_d}{dt}$$

Therefore:

$$P_{rr} = f_s \int_0^{Q_2} V_d\, dQ_d \qquad 3.2\text{–}45$$

The diode voltage is seen as a function of the stored charge. During period T_m the diode voltage is very low and can be neglected. During period T_d the reverse voltage rises and will reach a voltage level denoted V_{rm}. The voltage rise characteristic is determined by external circuit components and the diodes own properties. It is normal to assume that the voltage rises linearly during T_d from zero to V_{rm} so the average voltage at which charge is removed is $V_{rm}/2$. Therefore Equation 3.2–45 can be reduced to:

$$P_{rr} = f_s \frac{E}{2} Q_2 \qquad 3.2\text{–}46$$

Generally for soft recovery diodes Q_2 is approximately the same as Q_1 and so some manufacturers recommend, [20]:

$$P_{rr} = \frac{f_s \ E \ Q_{rr}}{4} \qquad 3.2\text{–}47$$

However in for this design it will be assumed that the reverse voltage rises instantaneously to the value of E and hence:

$$P_{rr} = \frac{f_s \ E \ Q_{rr}}{2} \qquad 3.2\text{–}48$$

In practice the rising reverse voltage characteristic is a function of the external snubbing networks. The diode snubbing philosophy has been to provide small RC snubbers with the peak voltage being clamped to the steady state value. The reverse voltage is therefore likely to rise relatively quickly. Assuming instantaneous rise in diode reverse voltage therefore better models the actual circumstances. Equation 3.2–48 will yield a slightly conservative result whereas equation 3.2–47 would be an under estimate.

3.3 Power Diode Turn On Characteristics

In power electronic circuits the diode forward current is generally forced and the voltage developed across the diode is a function of its internal processes. Normally the current during turn on increases at a rate determined by the turn off characteristics of another semiconductor device. This could be another diode undergoing snap off or a controlled device being turned off. During the application of forward current to a non–conducting diode the peak forward voltage developed can be far in excess of that for the conducting state. The peak voltage increases with an increasing rate of rise of forward current.

A typical forward recovery transient is shown in Figure 3.10. Just before the application of forward current the depletion region exists due to reverse voltage as illustrated in Figure 3.2. Due to the asymmetrical doping the depletion region in the lightly doped p section will be much wider then that in the n^+ section. Once forward current commences electrons from the n^+ region are almost immediately injected into the p region. The minority carrier density quickly grows and recombination with majority carriers commences. The already depleted majority carrier concentration is further reduced creating greater negative space charge near the junction. Minority carriers also flow by diffusion due to the concentration gradient which is being established. At the p region ohmic contact, holes are being injected at an equally high rate and because the minority carrier concentration in this area, at this time is low, recombination is also low. An electric field is established across the p region driving majority carriers towards the junction and minority carriers towards the ohmic contact. Charge carriers also move by diffusion as concentration gradients are established. The typical minority charge distribution progress with time during a forward current transient is shown in Figure 3.10. The carriers can only flow and reach a steady state distribution by diffusion and drift.

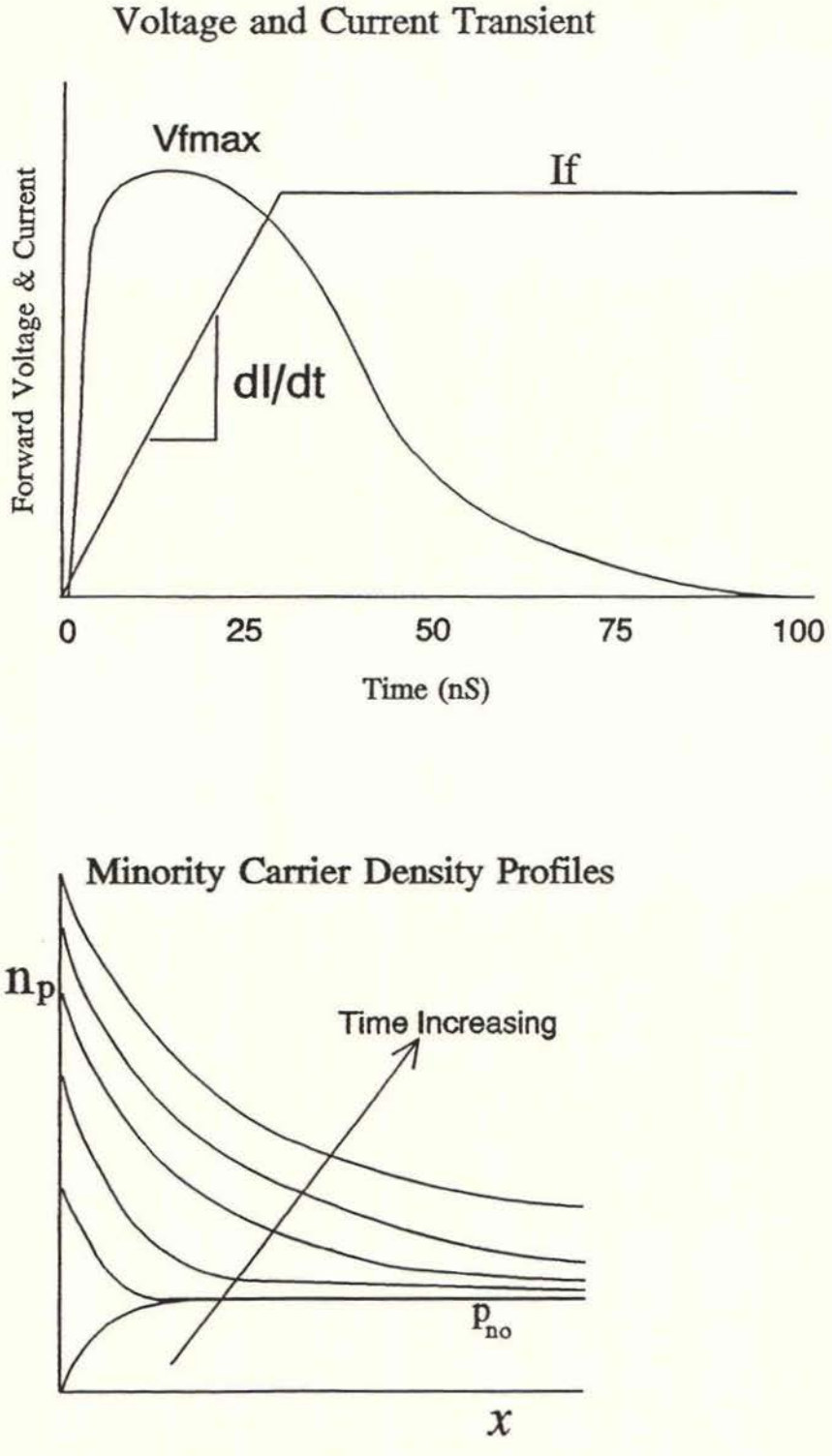


Figure 3.10 Typical Diode Forward Recovery Transient

If the rate of rise of forward current is low, the charge distribution can closely follow the rising current and diffusion processes dominate. Under these conditions the necessary electric field is low. At high rates of rise of forward current significant electric field levels are established making the drift component of charge flow dominate, [31].

To achieve the charge distribution necessary for steady state conduction, with conductivity modulation, a certain amount of charge has to be transported within the diode. The electric field is predominantly responsible for this at high rates of increase of forward current. According to equation 3.1–2 charge flow due drift is directly proportional to the electric field strength. It follows that a certain electric field, time product is necessary to establish the necessary charge distribution and hence conductivity modulation. This equates to a volt–second product across the diode. This makes the diode behave like an inductor during initial turn on if the rate of rise of current is high. The transient is often modeled using an R–L series circuit with R being a function of the forward current, [24]. The voltage generated can be substantial with peak forward voltages in the region of 150V being possible for some diodes with 30V being typical of most fast recovery diodes, [20–22,31].

From observation of equation 3.1–2 it is seen that the charge flow due to drift is proportional to electric field and charge concentration. Since the charge concentration on average is low throughout the p region in the early stages of the transient the electric field will reach high levels. Once the charge builds up the electric field reduces and the diode effectively becomes more conductive (conductivity modulated). A high rate of increase of current will tend to cause a high forward voltage to initially develop but the time for which this is sustained is short. A lower rate of rise of current which would cause less forward voltage to be developed but for a longer time. If the forward current reaches its final value while the internal charge structure is still in a transient state then its magnitude as well as rate of rise would affect the peak voltage.

Charge flow due to drift reaches a saturation level at electric field strengths around 10^4 V/cm. Beyond this the field begins to increase even more rapidly. However at field strengths of around 10^5 V/cm minority carriers gain sufficient energy to excite minority carriers from the lattice during collisions and avalanche multiplication occurs in the forward direction. The generation of additional charge assists the semiconductor into conductivity modulation, and the forward voltage does not significantly increase beyond this level, [31].

An important point that must be made is that very fast reverse recovery diodes tend to generate high forward voltage transients. This is an unfortunate characteristic since in high frequency high power converters good reverse and forward recovery performance are both desirable. The reason is that short minority carrier life times conflict with the establishment of conductivity modulation.

The DSE60–10A diode had excellent reverse recovery performance but exhibited reasonably poor forward recovery performance. Unfortunately the manufacturer neglected to include this information in the data sheet, [19]. The major consequences of high forward recovery voltages is the increased voltage stress applied to other circuit components.

The effect of diode forward recovery in the buck converter cell displayed in Figure 3–11 will be examined. First forward recovery in diode Ds will be discussed. Consider the the period where the IGBT is switched off. Load current I_L is transferred from the IGBT to the Snubber Diode D_s via the snubber capacitor C_s. The rate of diversion is normally assumed to be forced by the IGBT and in this case is approximately 300A/μS. Diode D_s is forced to conduct this current. The rate of rise of voltage across the IGBT is controlled by the snubber capacitor.

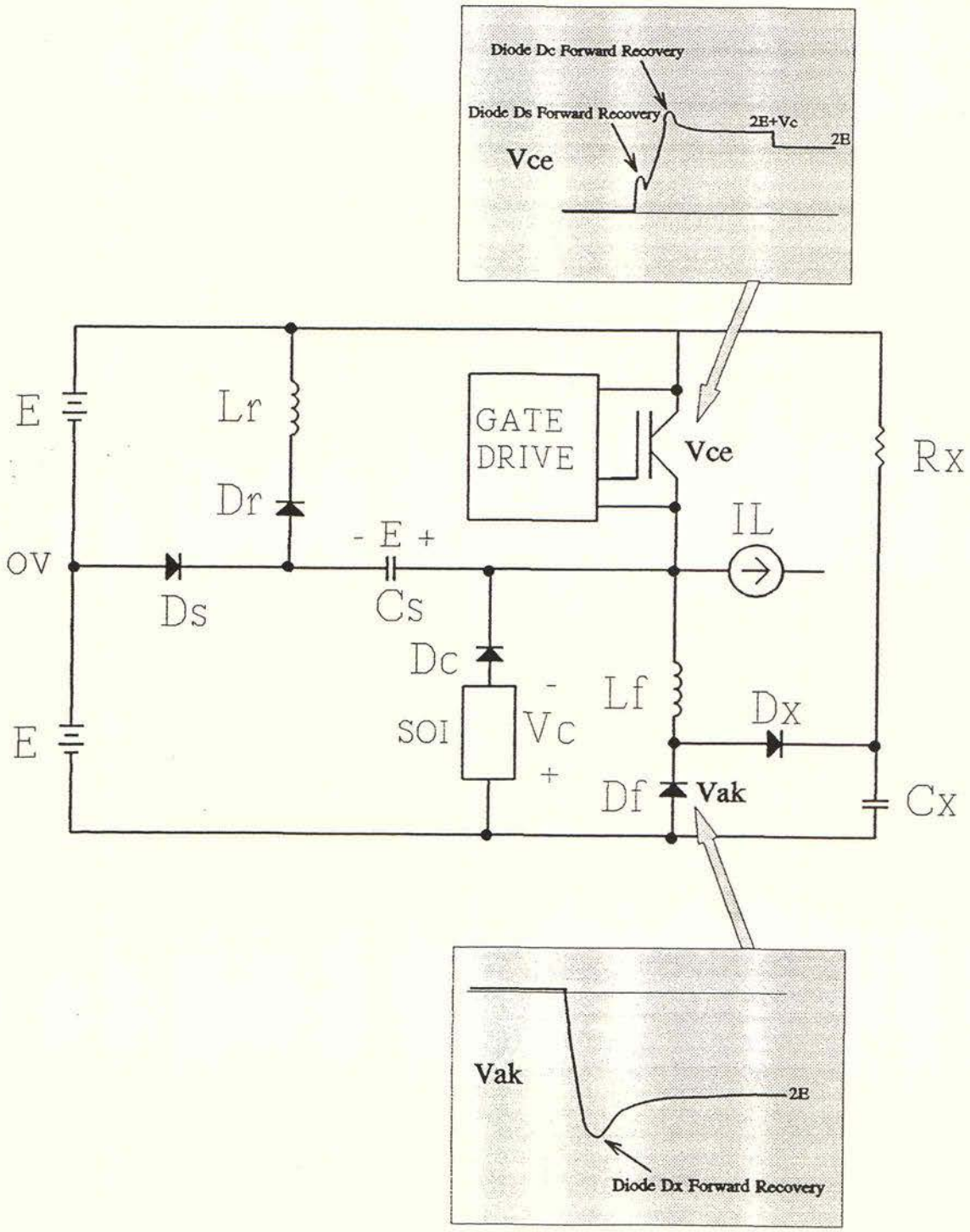


Figure 3.11 Circuit Effects of Diode Forward Recovery

However during the current transfer period the forward recovery voltage across D_s and the voltage developed across the wiring inductance causes a step in the initial IGBT voltage. Great effort was put into the construction and layout designs to reduce wiring inductance since even an inductance as low as $0.1\mu H$, which is equivalent to approximately 100mm of standard wire, would develop 30V across it. The inductance of the snubber circuit is estimated to be approximately $0.2\mu H$. The actual step voltage across the IGBT was found to be approximately 240V. The circuit inductance would account 60V of this and the diode forward recovery would account for the other 180V. The diode D_s is actually two DSE1 60–10A diodes in series so the peak forward voltage per diode at a dI_f/dt of 300 $A/\mu S$ would be approximately 90V. The direct consequences of the step voltage on the IGBT is increased turn off loss.

Secondly diode forward recovery is also experienced in the clamp diode D_c. In this case once the the voltage across the IGBT exceeds $(2E + V_c)$ current will be diverted from D_s to D_c. The diversion relationship is a function of the rising capacitor voltage and the circuit inductance and so is more complex than the first case and beyond the scope of the present discussion. Suffice it to say that the effective diversion rate is much lower than the first case and so the forward recovery is also much smaller.

The third section of the circuit where forward recovery has an effect is the reverse voltage overshoot on the freewheel diode D_f caused by the diode D_x. Consider the period when the IGBT switches on, the current in D_f decreases at a rate determined by the supply voltage (2E) and the commutating inductance L_f. Since L_f is $2\mu H$ and the nominal supply voltage is 560V the rate of decay of current is $280A/\mu S$. The maximum reverse recovery current flowing in D_f as will be shown in the next chapter is nominally 30A for a load current of 100A. This current, once D_f snaps off, is diverted into D_x and the energy stored in D_x is dissipated in R_x.

The snap off rate of D_f determines the rate of increase of current in D_x and so the peak forward voltage. The snap off rate is estimated to be 300A/μS. The peak forward voltage therefore should be around 90V as it was in the previous case. Actual measurements verified the forward recovery voltage.

Attempts were made to reduce the peak forward recovery voltage by placing two diodes in parallel. It was reasoned that dI/dt for diode would be halved and therefore the peak voltage should be reduced. The actual outcome was that there was little or no change. Further to this multiple parallel diodes were trialled, only after the current was shared over six diodes did any real reduction occur. It is thought that the reason for this is that the diodes avalanche in the forward direction down to a dI/dt of 60 A/μS. This is particularly poor, but is a result of the manufacturer having optimised the reverse recovery performance. Combined with the effects of the circuit inductance and the charging of C_x the total overshoot voltage on the diodes was 130V.

This explanation is presented in hindsight since no appreciation was had of severity of the forward recovery transient for these diodes until they were actually tested. Total peak reverse voltage across D_f was found to be 690V at the nominal bus voltage and a load of 75A. Although this was well below the maximum reverse rating, at the maximum load and bus voltage it could be expected that it would exceed 800V. Another influencing factor is the junction temperature. Although it is not well documented forward recovery voltage is known to increase with temperature, [36]. It was believed that there was insufficient margin in this design. The decision was made to modify D_f, which was originally six DSE1 60–10A diodes in parallel, to 12 diodes in a series parallel configuration to provide the additional margin. The disadvantage of this modification is increased conduction power loss.

3.4 Power Diode Forward Conduction Characteristics

Because power diodes almost universally are operating in the high level injection mode additional voltage apart from the junction potential is dropped across the diode. This is due to the electric field, required to transport majority carriers, building up to significant levels during high level injection. This voltage drop is close to being proportional to current and hence is modeled as simple series resistance (R_f). The total diode forward voltage is then given by:

$$V_f = V_{to} + I_f R_f \qquad 3.4\text{–}1$$

And therefore the conduction loss will be:

$$P_c = I_f V_{to} + I_f^2 R_f \qquad 3.4\text{–}2$$

For the DSEI 60–10A diode:

$$V_{to} = 1.4V \ @T_j{=}150^oC$$
$$R_f = 6m\Omega \ @T_j{=}150^oC$$

It is known that V_{to} decreases with temperature while R_f can either increase or decrease slightly with temperature depending on the diode structure. Unfortunately no data was given for the DSEI 60–10A to indicate the temperature dependence of V_{to} and R_f. Observation of data for similar diodes indicated that it would be safe to assume that R_f would be constant and in the worst case V_{to} would increase at $3mV/^oC$ as temperature is reduced, [20–22,37]. Therefore:

$$V_{to} = -3\times10^{-3} T_j + 1.85 \qquad 3.4\text{–}3$$

$$P_c = I_{favg}[-3\times10^{-3}T_j+1.85] + 6\times10^{-3}I_{frms}^2 \qquad 3.4\text{–}4$$

The forward voltage drop is quite high compared with normal power diodes. This is normal for high voltage diodes with low minority carrier lifetimes.

Light doping as well as longer base structures are required to obtain the reverse voltage rating. Both these tend to increase the minority carrier lifetime. To keep the minority carrier lifetime low, gold is often diffused into the silicon and produces a "trapping site" for minority carriers hence reducing there lifetime. However the reduction of minority carrier lifetime reduces the conductivity modulation effect and so contributes to increased forward drop, [28]. As already pointed out the Forward recovery characteristics also tend to suffer in high voltage low lifetime power diodes. The manufacture of high voltage high speed power diodes is a difficult task and in fact impossible using the normal p–n structure. The p–i–n is generally used in high voltage high speed diodes. The analysis of the p–i–n structure is more complex but the final results are similar. The material presented covering reverse recovery and forward recovery although based on a p–n structure is still quite valid, [24].

3.5 IGBT Characteristics

The insulated gate bipolar transistor is a recently developed power semiconductor device which shows great promise in the low and medium power range. The device selected for this converter is the TOSHIBA MG200Q1US1 IGBT which has a maximum continuous collector current of 200A and a maximum forward blocking voltage of 1200V, [8].

At first sight the device current rating would seem excessive for this application as the maximum continuous current is 100A. However in high frequency converters despite the use of snubbing systems switching loss becomes significant. This means the reduction of the conduction losses is necessary to keep the total losses and hence the cooling requirements to a practical level. The 200A rated IGBT gives the advantage of a lower forward voltage drop and hence lower conduction loss than a 100A device at the same load. The IGBT's internal structure as shown in Figure 3.12 can be modeled by a n–channel enhancement mosfet driving a pnp transistor, [8].

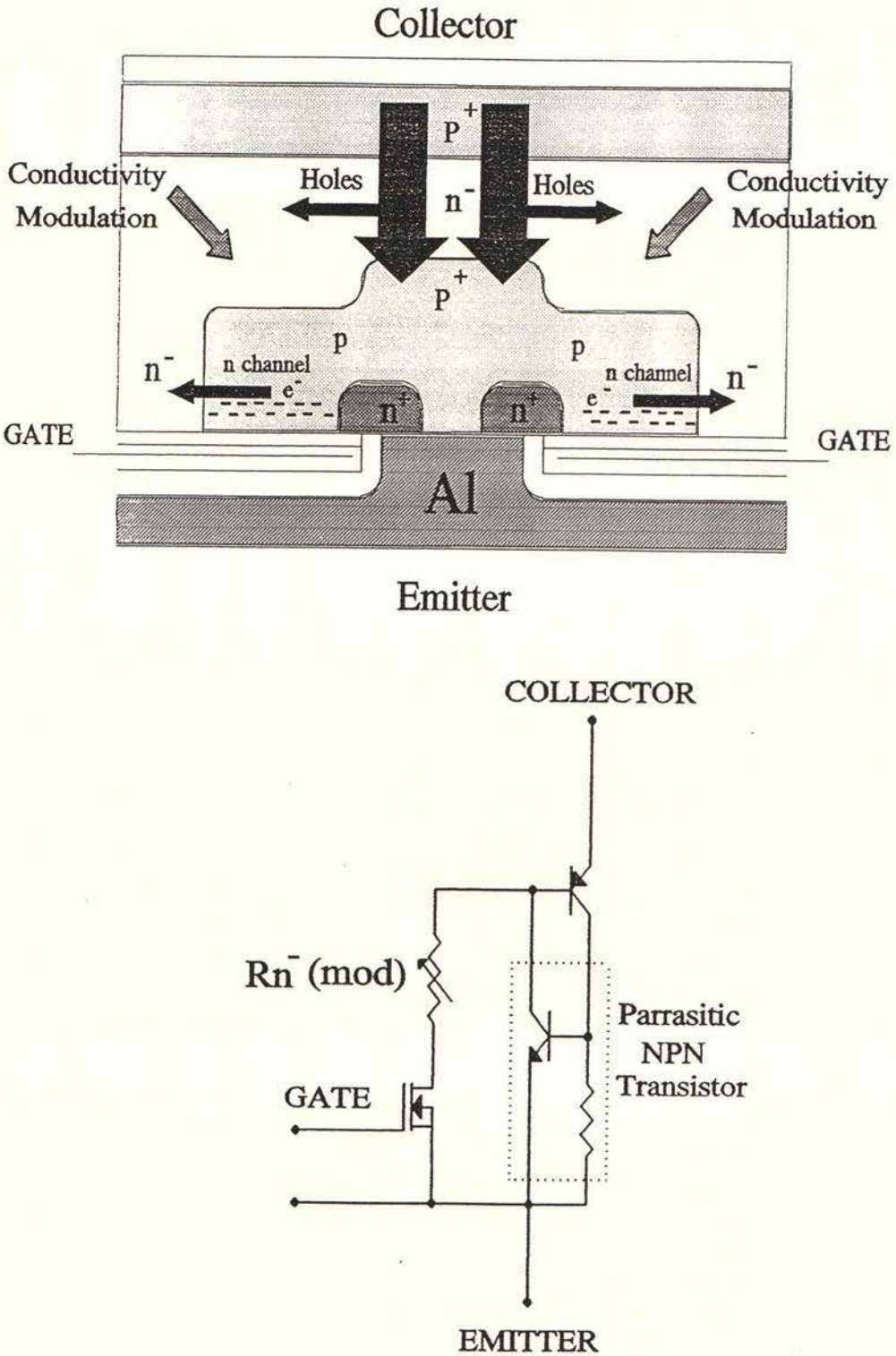


Figure 3.12 Insulated Gate Bi-Polar Transistor Operation

Application of a gate to emitter voltage causes an n–channel to be established between each n^+ layer and the n^- layer through the p layer. The top p^+ n^- junction is forward biased causing injection of holes into the n^- region which become minority carriers. A fraction of these will recombine with electrons in the n^- layer and hence contribute to the n–channel electron current. The greater fraction of the minority carriers are swept across the second p–n junction and on to the emitter. At high current densities the minority carrier density in the n^- layer reaches a level at which, in order to preserve charge neutrality, the majority carrier concentration becomes significantly increased, the result being increased conductivity, ie Conductivity Modulation, [8]. The drain resistance of the mosfet is effectively modulated by the collector current. The pnp transistor base drive current automatically adjusts in relation to the collector current with the collector emitter voltage drop being maintained low. This gives the IGBT a lower forward drop then an equivalent mosfet. In addition to this the minority carrier storage is controlled since the pnp transistor is never overdriven with its collector base junction becoming forward biased. Hence the storage time can be kept low. For this device the storage time is approximately 500nS, [8]. For an equivalently rated bipolar switching transistor the storage time would be around 10μS, which is unworkable in this application.

3.6 IGBT Conduction Power Loss

The on–state forward characteristics can be modeled by a fixed voltage source in series with a resistance. Therefore the forward voltage is given by:

$$V_f = V_{to} + R_f I_f \qquad 3.6\text{–}1$$

The parameters V_{to} and R_f are functions of the device case temperature. From [8]:

$$V_{to} = -6\times10^{-3}\, T_c + 2\ 25 \qquad 3.6\text{–}2$$

$$R_f = 9\times10^{-6}\, T_c + 4.3\times10^{-3} \qquad 3.6\text{–}3$$

T_c – Device case temperature in ^{0}C

From equations 3.6–1,3.6–2 and 3.6–3:

$$P_c=(-6\times10^{-3}T_c+2.25)I_{favg} + (9\times10^{-6}T_c+4.3\times10^{-3})I_{frms}^2 \qquad 3.6\text{–}4$$

3.7 IGBT Switching Power Loss

The IGBT turn on and turn off loss have been greatly reduced by the use of external snubbing and clamping networks. However the switching loss is still significant compared with the conduction loss and therefore must be considered. At turn on the diversion of load current from the freewheel diodes to the IGBT is determined by the voltage applied across L_f. Assuming the IGBT turned on instantly the diversion rate would be 280A/μS for a supply voltage of 560V. In reality the IGBT current rise time is 150nS, [8]. At a final collector current of 100A this would result in a maximum turn on dI/dt of 667A/μS. The required dI/dt of 280 A/μS is substantially below this. The IGBT turn on voltage will therefore collapse over 150nS. The current rise characteristic would then be determined by the collector emitter voltage decay. Assuming a linear fall in voltage from the supply voltage 2E to zero over 150nS the collector voltage would be given by:

$$V_{ce} = \frac{-2E}{t_r} t + 2E \qquad 3.7\text{–}1$$

t_r – Rise Time

The voltage across L_f will be given by:

$$V_{L_f} = \frac{2E}{t_r} t \qquad 3.7\text{–}2$$

The diverted current is therefore:

$$I_c = \frac{1}{L_f} \int \frac{2E}{t_r} t \, dt$$

$$I_c = \frac{1}{L_f}\,\frac{2E}{t_r}\,\frac{t^2}{2} \qquad 3.7\text{–}3$$

The turn–on power loss will be found from:

$$P_{s1} = f_s \int_0^{t_r} V_{ce}\, I_c\, dt$$

f_s – switch frequency

Substituting equations 3.7–1 and 3.7–3:

$$P_{s1} = f_s \int_0^{t_r} \left[\frac{-2E}{t_r}\, t + 2E\right] \left[\frac{1}{L_f}\,\frac{2E}{t_r}\,\frac{t^2}{2}\right] dt$$

$$P_{s1} = \frac{2E^2 f_s}{t_r^2\, L_f} \int_0^{t_r} (t_r\, t^2 - t^3)\, dt$$

$$P_{s1} = \frac{2E^2 f_s}{t_r^2\, L_f} \times \frac{t_r^4}{12}$$

$$P_{s1} = \frac{E^2 f_s t_r^2}{6L_f} \qquad 3.7\text{–}4$$

The analysis above assumes that the final collector current is not reached within the rise time (t_r). This is justified for the majority of the load range. For low loads equation 3.7–4 gives a conservative result.

There is another component of turn on loss that has not been considered in the above analysis. The collector emitter voltage decays to a low level within t_r but not to the final steady state value.

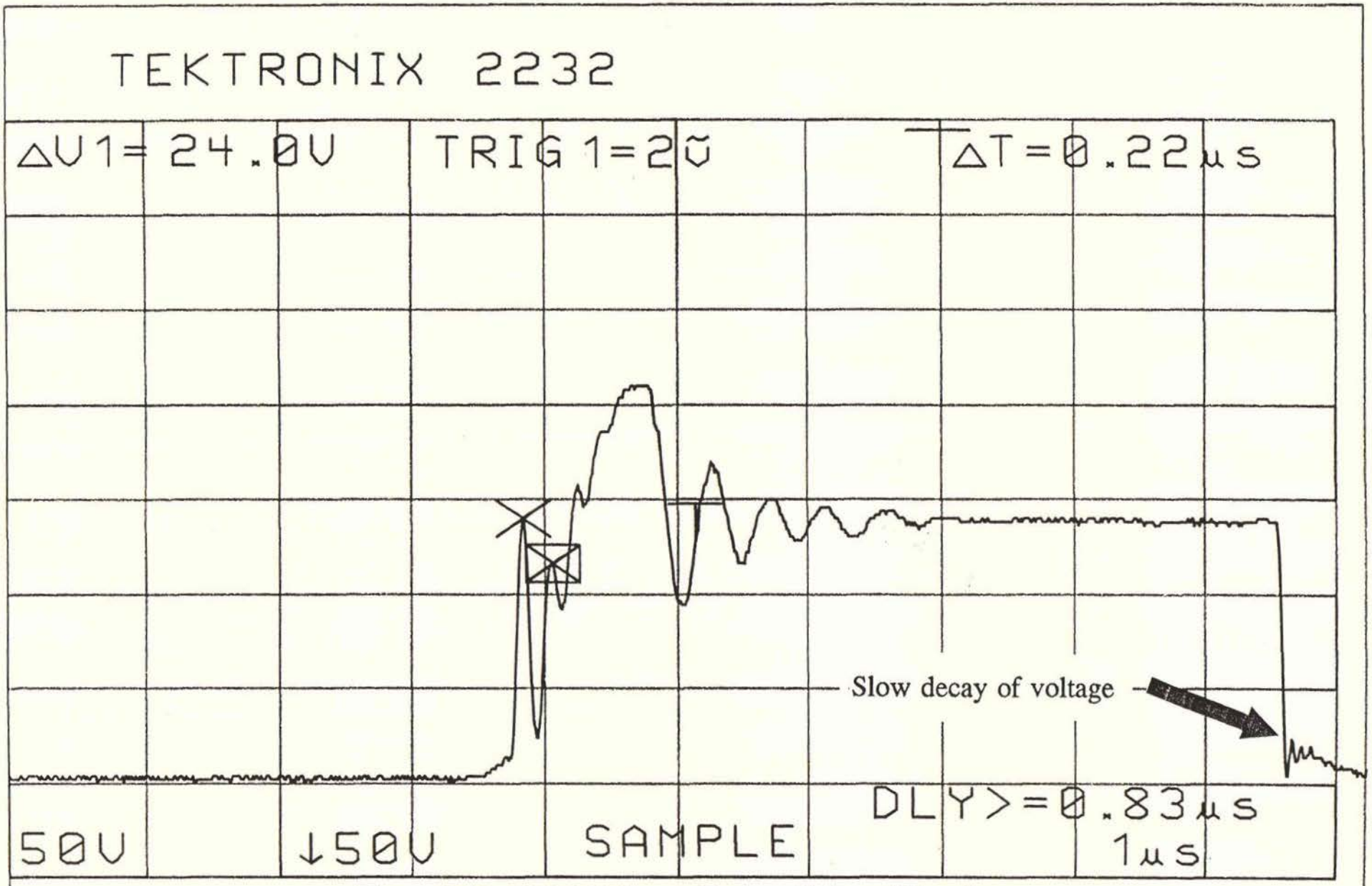


Figure 3.13 IGBT Collector Emitter Voltage Waveform

IL= 75A, Vbus=560V ; Scale-200V/div

It is thought that a period must elapse before full conductivity modulation is achieved. Figure 3–13 shows an actual oscillograph trace of V_{ce} for a load current of 75A. After the t_r period is complete the forward voltage tails off at a much slower rate from approximately 35V to the steady state value over 0.4μS. As will be seen in Chapter Four this represents a significant loss, however from the data presented in, [8] it is impossible to predict. An attempt to estimate it is carried out in Chapter Four.

The IGBT turn off is characterised by a short storage period during which time the minority carrier concentration declines. A point is reached where the full load current is no longer sustainable and the collector current begins to decline over a period t_f. From [8] it can be seen that the fall time is essentially constant at approximately 200nS over the range 40 to 200A. During the fall time load current is diverted to snubber capacitor C_s via diode D_s. The initial voltage across the capacitor has been reset to E such that the initial IGBT voltage is zero. If it is assumed that the IGBT current decays linearly to zero over t_f the snubber current will be given by:

$$I_{C_s} = \frac{I_L}{t_f} t \qquad 3.7\text{–}5$$

$$0 \leq t \leq t_f$$

Therefore:

$$v_{C_s}(t) = \frac{-1}{C_s} \int_0^t \frac{I_L}{t_f} t \, dt + E$$

$$V_{ce}(t) = E - V_{C_s}(t)$$

$$V_{ce}(t) = \frac{1}{C_s}\int \frac{I_L}{t_f}\, t\, dt$$

$$V_{ce}(t) = \frac{I_L t^2}{2\, t_f C_s} \qquad 3.7\text{–}6$$

The power dissipation due to the switch off transient will be given by:

$$P_{s3} = f_s \int_0^{t_f} V_{ce}\, I_c(t)\, dt$$

The collector current $I_c(t)$ is given by:

$$i_c(t) = \frac{-I_L}{t_f}\, t + I_L \qquad 3.7\text{–}7$$

From 3.6–57, 3.6–58 and 3.7–7:

$$P_{s3} = f_s \int_0^{t_f} \frac{I_L t^2}{2\, t_f C_s} \left[\frac{-I_L}{t_f}\, t + I_L \right] dt$$

$$P_{s3} = \frac{f_s I_L^2\ t_f^2}{24\ C_s} \qquad 3.7\text{–}8$$

However this analysis does not account for the effect of the forward recovery of diode D_s on the IGBT switch off loss as discussed in Section 3.3. Since no data is given for the forward recovery performance of the diodes, results from the test chopper will be used. Examination of the mechanism involved indicates that the volt–second area product to obtain full conduction is approximately constant for a given diode. Test results showed that for these diodes 3 VμS was required for conduction to occur.

The forward recovery period and maximum voltage is controlled by auxiliary RC snubbers across D_s and the IGBT, with the ($V\mu S$) remaining approximately constant. Increasing the snubber capacitance will reduce the peak voltage but extend the period of the recovery. Increased capacitance results in increased series resistor power loss. Hence there are practical limits to the size of the auxiliary snubbers. For the auxiliary snubbers used the forward recovery period was found to be in the order of 50nS. Within this period at a rate of decay of $280A/\mu S$ the collector current would have only reduced by 14A. As a conservative estimate it will be assumed that the diode forward recovery is impressed on the IGBT at the full load current. Therefore:

$$P_{s4} = \psi_d \, I_L \, f_s \qquad 3.7\text{–}9$$

ψ_d – Diode Forward Recovery Volt–Second product ($3V\mu S$)

The concepts and results developed above will be applied in Chapter Four to calculate the IGBT loss as part of the power circuit design.

4. POWER CIRCUIT DESIGN

In this chapter the the detailed design of the positive buck converter is presented. The design of the negative buck converter is identical except that the circuit is inverted. The design of power electronic converters, because of the complex interdependence of component values, is an involved task. Normally many iterations are conducted before the design is complete. Rather than presenting the design process as it was carried out, the selected component values are presented and their choice is verified. The relevant design equations are developed and the methodology is explained.

Two important components are the main snubber capacitor, C_s, and the dI/dt limiting inductor, L_f. These two components either directly or indirectly influence the design of much of the remaining converter. The first section of the chapter is devoted to a discussion of the selection of C_s and L_f.

The converter has been divided into functional modules. The design and stress levels are examined for all the major components in each module. In reference to Figure 4.1 These include:

(a) The snubber module including C_s,D_s and the capacitor resonant resetting circuit including D_r and L_r.

(b) The clamp module including D_c and the SOI.

(c) The freewheel diode module including D_f,L_f,D_x,C_x and R_x.

(d) The IGBT module.

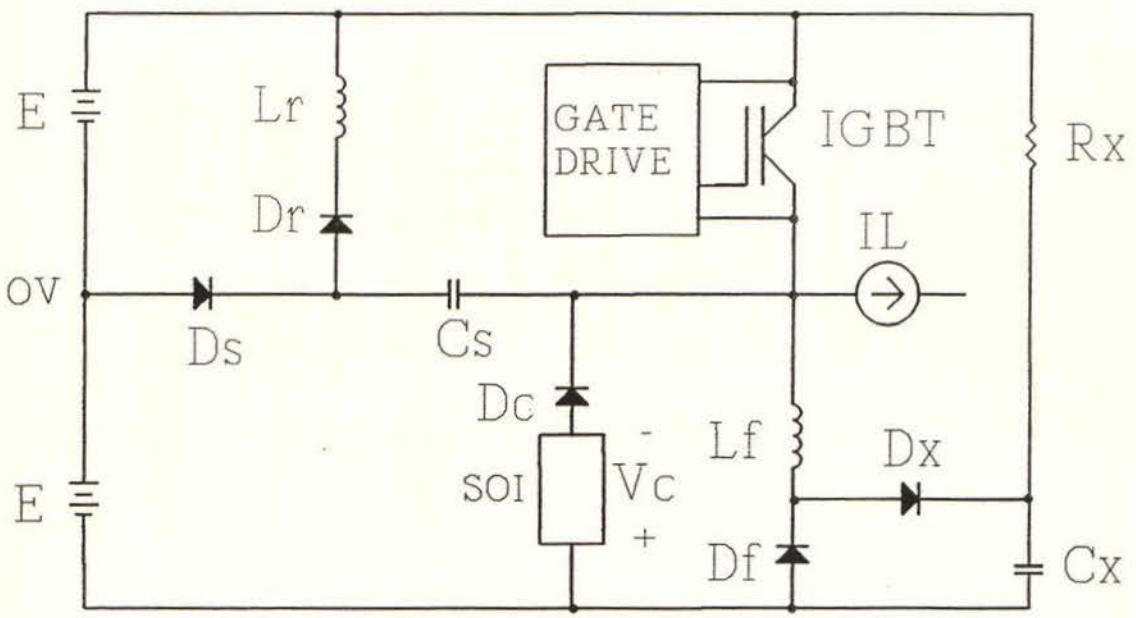


Figure 4.1 Simplified Positive Buck Converter Cell

As part of the clamp module a circuit description of the SOI is given and its operation is discussed. The IGBT module includes an operational description of the gate drive circuit.

The overall power loss is calculated for the rated output current of 100A at the nominal bus voltage of 560V for 50% duty cycle. This value is used to size the heatsinks and the forced cooling air requirement.

At the conclusion of the chapter results from the prototype buck converter are presented.

4.1 General Considerations

It is impractical to repeat the design process in its entirety in this chapter. Instead the final component selections will be presented and demonstrated to be appropriate according to the major criteria involved. The maximum voltage, current and thermal stresses, which ever is applicable will be calculated under the worst case operating condition for the particular component.

Since the major power dissipating components are mounted on a common heatsink the temperature of this heatsink is required to be known to be able to complete many of the calculations. This temperature will be assumed to be $80^{o}C$ and the total power dissipation at rated output and nominal operating conditions will be calculated and used to size the heatsink.

Following is a list of values of the major components and important parameters as implemented in the final design which will be used in the subsequent sections:

Assumed main heatsink temperature(T_h) = $80^{o}C$

Minimum IGBT on time (t_{mn}) = $2.5\mu S$

Minimum IGBT off time(t_{mf}) = 2.5μS

Supply voltage(E) = 280Vdc $\pm$ 20%

Clamping voltage(V_c) = $\frac{13}{28}$ × E

Freewheel diode commutating inductor(L_f) = 2.0μH

Freewheel diode clamping capacitor(C_x) = 0.9μF

Freewhweel diode clamping resistor(R_x) = 23.5Ω

IGBT snubber capacitor(C_s) = 0.05μF

Snubber resonant reversing inductor(L_r) = 8μH

Switching frequency (f_s) = 50kHz

Switching period(T) = 20μS

IGBT rise time (t_r) = 150nS

IGBT fall time (t_f) = 200nS

First the selection of L_f and C_s in relation to converter losses and the IGBT minimum on and minimum off time will be discussed. The values of C_s and L_f play a major role in the design of the entire converter.

4.2 Selection of the Snubber Capacitor and the Commutating Inductor

The selection of the snubber capacitor, C_s and the commutating inductor, L_f, are closely tied since both of them effect the operation of the converter when the IGBT turns off and on. When the IGBT turns off load current is diverted during its fall time (t_f) to the snubber capacitor C_s. This is illustrated as (t_1 to t_2) in Figures 4.2 and 4.3. The initial voltage across the IGBT, disregarding any diode forward recovery effects is zero and the rate of rise is controlled by the value of C_s. During the period t_2 to t_3 the voltage across C_s rises linearly to –E. Once the capacitor voltage rises above –E the diode D_f becomes forward biased and begins to pickup current. The current in the snubber capacitor reduces The interchange of current between C_s and the freewheel diodes occurs during the period t_3 to t_4.

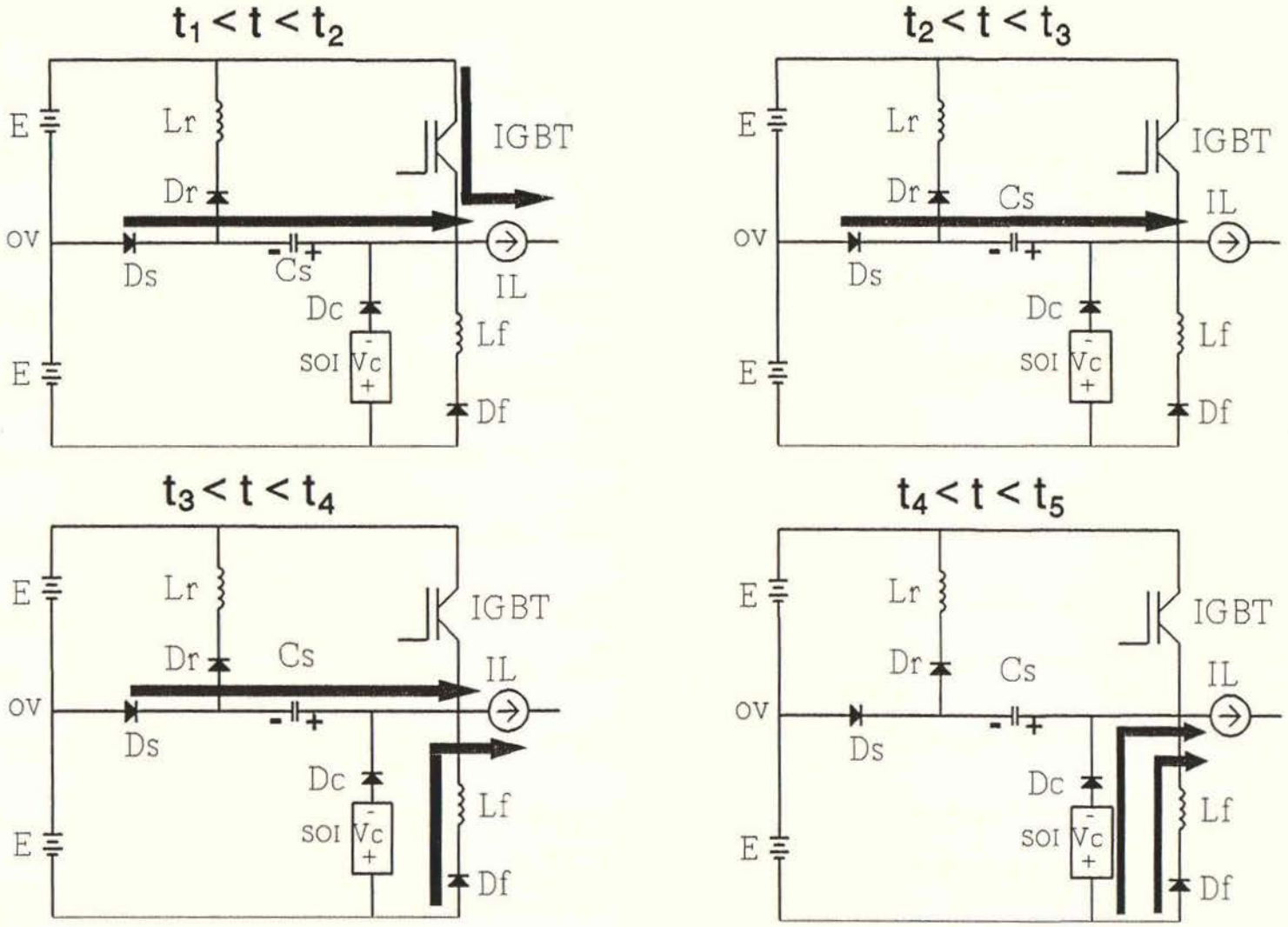


Figure 4.2 Snubber and Clamp Operational Sequence

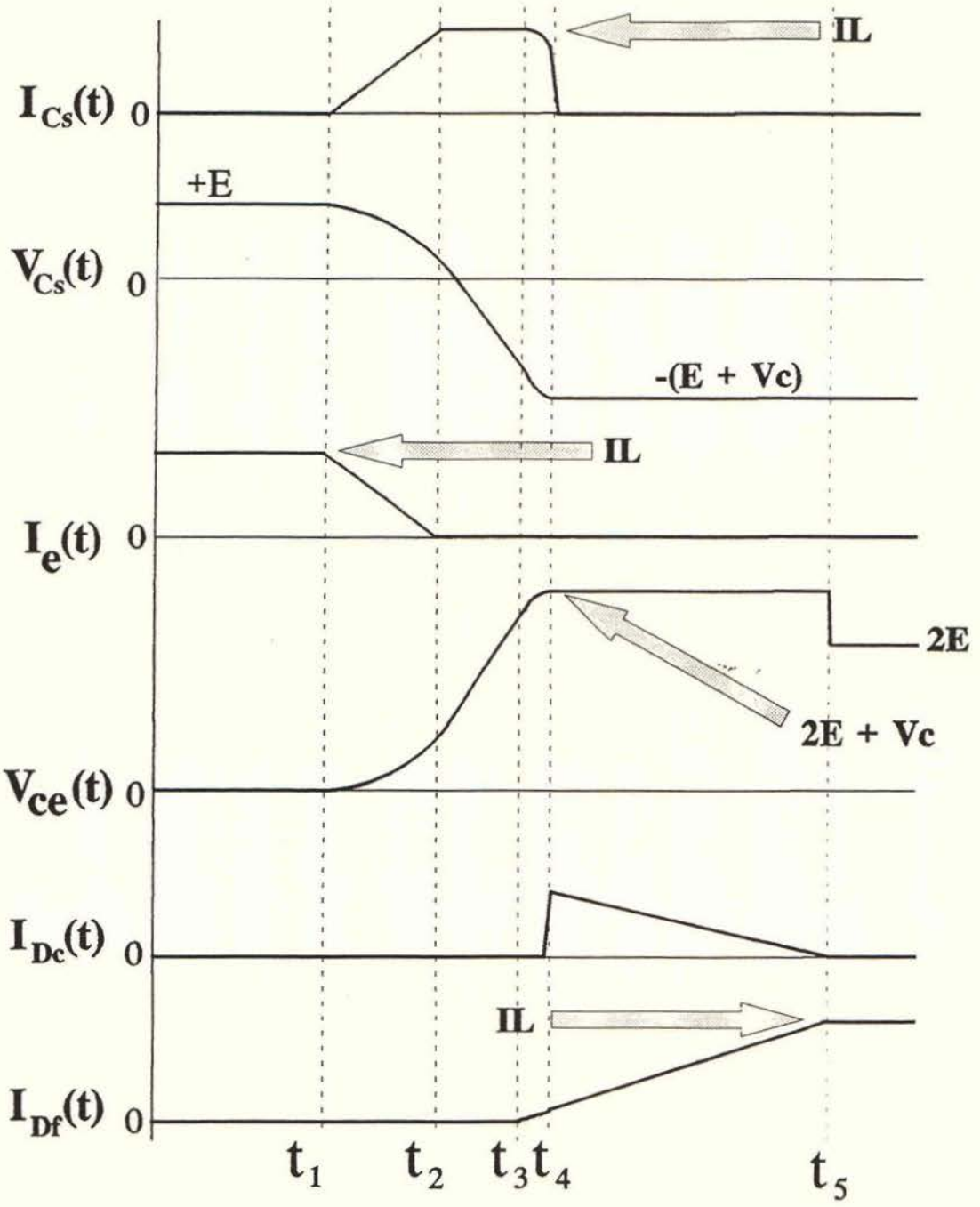


Figure 4.3 Snubber and Clamp Waveforms

Finally the capacitor voltage reaches $-(2E + V_c)$ and the diode D_c is forward biased so that the clamp voltage is applied across L_f. The current which was being carried by D_s is entirely transferred to D_c. During the period t_4 to t_5 the current in the clamp is diverted to the freewheel diodes the rate being determined by V_c/L_f. The total time t_1 to t_5 ,called t_d, represents the complete commutation time.

There are several factors which effect the selection of the values of L_f and C_s. These include the overall snubbing efficiency, the total commutation time and the rating of the recovery circuitry. The recovery circuitry in this case also includes the IGBT which must carry the resonant recovery current of C_s, increasing its peak current stress. This section discusses the selection of C_s an L_f in relation to loss minimisation and the total commutation time limitations. First the the overall snubbing loss will be considered. Increasing the values of L_f an C_s will reduce the switching loss in the freewheel diodes and the IGBT but increases the power that must be recovered and returned to the power supply. This power is recovered at an efficiency of less than 100%. The incremental reduction in switching loss reduces as the values of C_s and L_f increase. Therefore values of C_s and L_f can be selected that minimise the total loss.

In reference [15] a method was derived of selecting the values of L_f and C_s so that the overall power loss of the main switching device(IGBT) and the recovery system is a minimum. In this paper "Base snubber" values are found and all subsequent calculations are based on these. The term "Small Snubber" is applied to values below the base value and the term "Large Snubber" is applied to values above the base value. The base values are given by:

$$L_{fbase} = \frac{U_b \ t_f}{2I_L} \qquad 4.2\text{–}1$$

$$C_{sbase} = \frac{I_L \ t_f}{2 \ U_b} \qquad 4.2\text{–}2$$

U_b– supply voltage (2E)

Therefore using the values listed in section 4.1 and the nominal bus voltage and full load current:

$$L_{fbase} = \frac{560 \times 0.20}{2 \times 100} = 0.56 \ \mu H$$

$$C_{sbase} = \frac{100 \times 0.20}{2 \times 560} = 0.018 \ \mu F$$

Because the values chosen ($C_s = 0.05 \ \mu F$ and $L_f = 2 \ \mu H$) are greater than the base values, the snubbers are classified as large. This means that the snubber charging time is greater than the IGBT fall time. For a large snubber the optimum snubber size is given by:

$$X_{opt} = \frac{1}{\sqrt{3(1-\eta_r)}} \qquad 4.2\text{–}3$$

X_{opt} – Optimum multiple of the base value

η_r – Recovery system efficiency

From section 4.3 the snubber recovery efficiency in this converter is approximately 85%. Therefore X_{opt} will be:

$$X_{opt} = \frac{1}{\sqrt{3(1-0.85)}} = 1.5$$

This means that the optimum value for C_s will be $(1.5 \times 0.018) = 0.027\mu F$ and similarly for L_f it will be $(1.5 \times 0.56) = 0.84\mu H$. This analysis is true from a purely efficiency perspective. However there are other factors that need to be considered which make larger values for C_s and L_f a better choice. This analysis limits itself to the IGBT alone. While it is true that the function of the snubber capacitor is to control the turn off losses of the IGBT it is not true that the only function of L_f is to control the turn on losses. The peak reverse recovery current in the freewheel diodes and hence their switching loss is also dictated by the value of L_f. As will be seen in a later section it was necessary to make $L_f = 2\mu H$ to reduce this loss to an acceptable level.

An insufficiently large snubber capacitor causes excessive IGBT voltage overshoot. The overshoot being due to both parasitic inductance and the forward recovery of diode D_c. For this reason a value of $0.05\mu F$ was found to be more suitable. Another important factor is that increasing the values of C_s and L_f also extend the commutation time. It is desirable that for the major part of the operating load range that this time remains inside the minimum off time for the IGBT. If the IGBT switches on during the commutation period either the diode D_s or D_c will experience a reverse recovery dI/dt only limited by the rise time of the IGBT. Since this is of the order of 150nS this can be very severe and should be avoided where possible. As will subsequently be shown at the high end of the load range it is possible that the diode D_c will experience this if the inductor L_f is made too large or the minimum off time to small.

At the low end of the load range it will be the diode D_s which experiences the reverse recovery. This of cause can not be avoided, but the load current at which it occurs can be made sufficiently low by not selecting C_s too large or the minimum off time too short. By doing this the losses can be kept to an acceptable level. At the selected frequency of 50kHz the maximum value for t_{mf} and t_{mn} that could be tolerated was $2.5\mu S$. This restricts the output to $\pm$420V at the nominal bus voltage.

Although this limitation to a certain extent has been overcome by the control strategy used, 2.5μS still represents the maximum acceptable limit. Another parameter which has a bearing on the commutation time is the clamp voltage. The clamp voltage is proportional to the bus voltage. It is determined by the turns ratio of the SOI transformer. The maximum IGBT collector emitter voltage (V_{ce}) is determined by ($2E + V_c$) which at the upper limit of input voltage,($E = 336V$) will be 828V. In reality due to stray inductances and diode forward recovery effects this could be exceeded by up to 150V, under worst case conditions and therefore voltages approaching 1kV could be expected. This was considered to be the maximum voltage stress that could be tolerated for a 1200V device. In order to assess the selection of C_s and L_f in terms of the commutation time an expression for t_d will now be derived one stage at a time.

$t_1 \leq t \leq t_2$

During the period t_1 to t_2 the IGBT current is assumed to fall linearly from I_L to zero over t_f and hence the snubber capacitor current rises linearly over the same period. The capacitor voltage which is initially reset to +E will decrease with a quadratic function. This relationship from equation 3.7–6 is:

$$v_{C_s}(t) = E - \frac{I_L(t-t_1)^2}{2\,t_f C_s}$$

At time t_2, i.e. $(t-t_1) = t_f$:

$$v_{C_s}(t_f) = E - \frac{I_L\,t_f^2}{2t_f C_s} = E - \frac{I_L\,t_f}{2\ C_s} \qquad 4.2\text{–}4$$

$$t_2 - t_1 = t_f \qquad 4.2\text{–}5$$

$t_2 \leq t \leq t_3$

During the period t_2 to t_3 the capacitor current is constant and equal to I_L, the voltage decays linearly from an initial voltage determined by equation 4.2–4.

Therefore:

$$v_{C_s}(t) = E - \frac{I_L t_f}{2\ C_s} - \frac{I_L}{C_s}(t-t_2)$$

$$v_{C_s}(t) = E - \frac{I_L}{C_s}\left[\frac{\tau_f}{2}(t-t_2)\right] \qquad 4.2\text{–}6$$

At t_3 the capacitor voltage will have reached –E and therefore:

$$-E = E - \frac{I_L}{C_s}\left[\frac{t_f}{2} + (t_3-t_2)\right]$$

$$(t_3-t_2) = \frac{2E\ C_s}{I_L} - \frac{t_f}{2} \qquad 4.2\text{–}7$$

$t_3 \leq t \leq t_4$

During the period t_3 to t_4 the capacitor C_s and the Inductor L_f form a parallel L–C circuit which has a total current of I_L flowing in it. The voltage across the capacitor can be shown to be:

$$v_{C_s}(t) = -[E + I_L Z_s \mathrm{Sin}(\omega_s(t-t_3)] \qquad 4.2\text{–}8$$

Where: $Z_s = \sqrt{\frac{L_f}{C_s}}$

$$Z_s = 6.32\Omega \text{ (Using as built values)}$$

$$\omega_s = \frac{1}{\sqrt{L_f\ C_s}}$$

$$\omega_s = 3.16 \text{ Mr/s (Using as built values)}$$

The magnitude of the current in C_s will be reducing and will be given by:

$$i_{C_s}(t) = I_L \text{Cos}(\omega_s(t-t_3)) \qquad 4.2\text{–}9$$

The magnitude of the current in L_f will therefore be:

$$i_{L_f}(t) = I_L[1 - \text{Cos}(\omega_s(t-t_3)] \qquad 4.2\text{–}10$$

The time t_4 is governed by when the capacitor voltage reaches $-(E + V_c)$:

$$-(E + V_c) = -[E + I_L Z_s \text{Sin}(\omega_s(t_4-t_3)]$$

$$(t_4-t_3) = \frac{1}{\omega_s} \text{Sin}^{-1}\left[\frac{V_c}{Z_s I_L}\right] \qquad 4.2\text{–}11$$

If $Z_s I_L < V_c$ the capacitor voltage fails to reach $-(E+V_c)$ and therefore the current is diverted to L_f without a clamping period.

The current which has been diverted to L_f will be given by:

$$i_{L_f}(t_4) = I_L\left[1 - \text{Cos Sin}^{-1}\left[\frac{V_c}{Z_s I_L}\right]\right]$$

$$i_{L_f}(t_4) = I_L\left[1 - \sqrt{1 - \left[\frac{V_c}{Z_s I_L}\right]^2}\right] \qquad 4.2\text{–}12$$

And therefore:

$$i_{c_s}(t_4) = I_L\sqrt{1 - \left[\frac{V_c}{Z_s I_L}\right]^2} \qquad 4.2\text{–}13$$

And since the current in the snubber capacitor is transferred to the clamp just after t_4:

$$i_{D_c}(t_4) = I_L\sqrt{1 - \left[\frac{V_c}{Z_s I_L}\right]^2} \qquad 4.2\text{–}14$$

$t_4 \leq t \leq t_5$

During the period t_4 to t_5 current is diverted from the clamp to the freewheel diodes and hence L_f. The initial current in D_c is given by equation 4.2–14 and during t_4 it is reduced linearly to zero at a rate determined by the clamp voltage V_c:

$$i_{D_c}(t) = I_L\left[\sqrt{1 - \left[\frac{V_c}{Z_s I_L}\right]^2}\right] - \frac{V_c}{L_f}(t - t_4) \qquad 4.2\text{–}15$$

The time (t_5–t_4) will be given by $I_{L_f}(t) = 0$:

$$0 = I_L\left[\sqrt{1 - \left[\frac{V_c}{Z_s I_L}\right]^2}\right] - \frac{V_c}{L_f}(t_5 - t_4)$$

$$t_5 - t_4 = \frac{I_L \; L_f}{V_c}\left[\sqrt{1 - \left[\frac{V_c}{Z_s I_L}\right]^2}\right] \qquad 4.2\text{–}16$$

From equations 4.2–5,4.2–7,4.2–11 and 4.2–16 the total diversion time t_d will be given by:

$$t_d = \frac{t_f}{2} + \frac{2E \; C_s}{I_L} + \frac{1}{\omega_s}\mathrm{Sin}^{-1}\left[\frac{V_c}{Z_s I_L}\right] + \frac{I_L \; L_f}{V_c}\sqrt{1 - \left[\frac{V_c}{Z_s I_L}\right]^2} \qquad 4.2\text{–}17$$

This relationship can be used to determine the suitability of the selected values for C_s and L_f.

A plot of total diversion time against load current with C_s as a variable parameter (0.03μF,0.05μFand 0.07μF are used) is displayed in Figure 4.4. A horizontal line indicates the minimum off time for the IGBT of 2.5μS. At high load currents the capacitor value has little effect on the total diversion time since t_4–t_1 is small compared with t_5–t_4. Its main effect is at low currents where the load at which the minimum off time constraint is violated is effected by the value of C_s. Also below a load current of V_c/Z_s the capacitor voltage fails to reach $-(E + V_c)$ and the current is diverted into the freewheel diodes without a clamping period and so t_5–t_4=0 and t_4–$t_3 = \pi/(2 \times \omega)$. In fact it can be shown for the capacitor values considered and $L_f = 2\mu$H that there is no clamping period for load currents that correspond to $t_d \geq t_{mf} = 2.5\mu$S. This means that only the snubber diodes will be involved in a high reverse recovery.

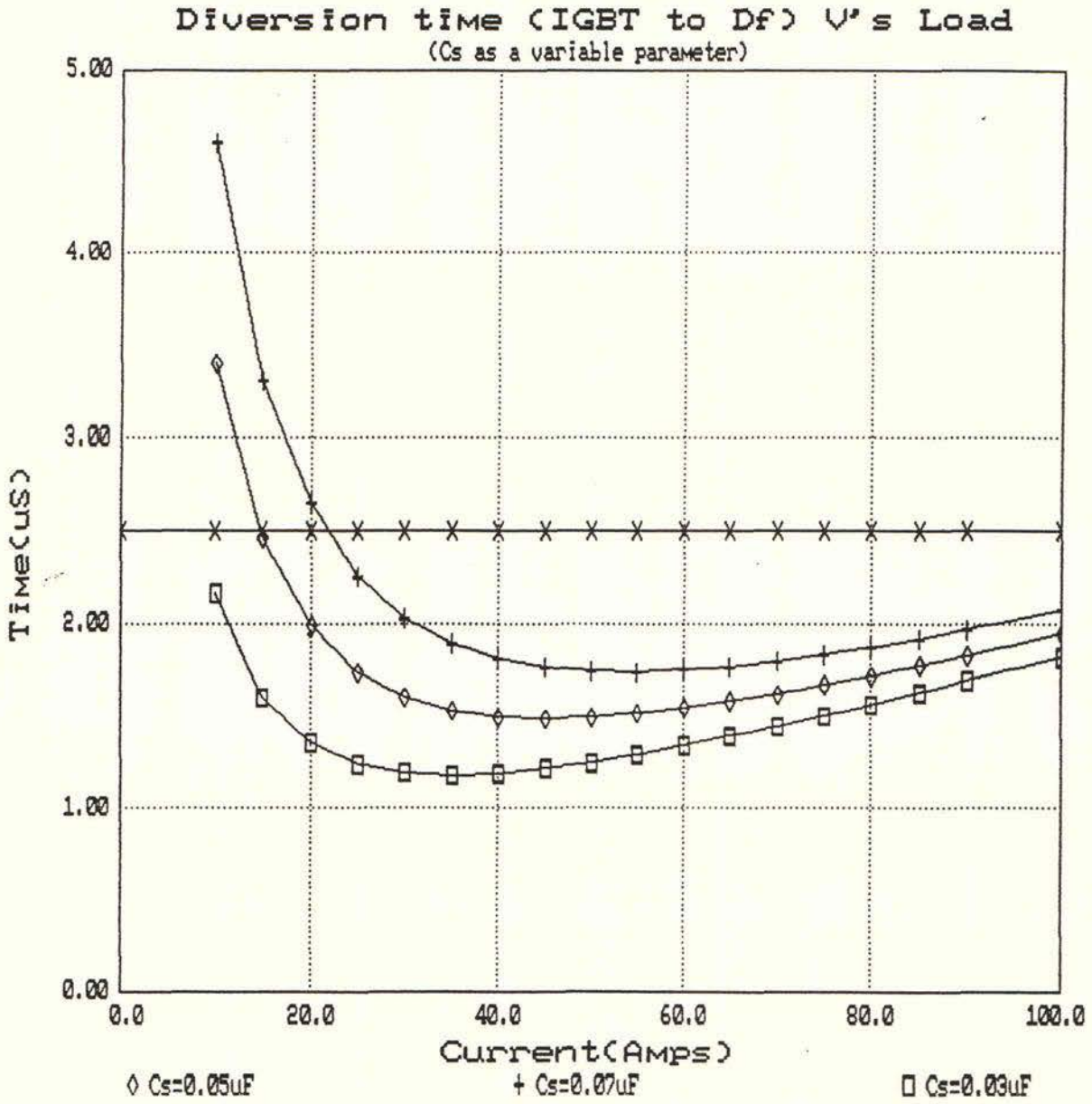


Figure 4.4 Effect of Cs on the Total IGBT to Df Diversion Time

The worst case occurs when diode D_s is carrying the total load current at t_3. This means that:

$$t_3 - t_1 = t_{mf}$$

$$\frac{t_f}{2} + \frac{2E\ C_s}{I_L} = t_{mf}$$

The diode D_s carries the full load current at this time so:

$$i_{C_s}(t_3) = i_L(t_3) = \frac{2E\ C_s}{\left[t_{mf} - \frac{t_f}{2}\right]} \qquad 4.2\text{–}18$$

The dI/dt is determined by the IGBT rise time as follows:

$$\frac{dI}{dt} = m = \frac{I_L}{t_r} \qquad 4.2\text{–}19$$

From Chapter Three an approximate expression relating I_{rm} to m and I_f for the DSE60–10A diodes was derived:

$$I_{rm} \approx m^{0.265}\, I_f^{0.735} - I_f \quad @T_j = 125^0C$$

Therefore from equation 4.2–16:

$$I_{rm} \approx \frac{I_L^{0.265}\, I_L^{0.735}}{t_r^{0.265}} - I_L$$

$$I_{rm} \approx I_L \left[\frac{1}{t_r^{0.265}} - 1 \right]$$

From Chapter Three the reverse recovery loss assuming instantaneous rise in reverse voltage:

$$P_s = f_s \, V_{rm} \, Q_2$$

Where:

$$Q_2 = Q_1 = \frac{I_{rm}^{\,2}}{2\,m}$$

Therefore:

$$P_s = f_s \, V_{rm} \, I_L^{\,2} \left[\frac{1}{t_r^{0.265}} - 1 \right]^2 \frac{t_r}{2I_L}$$

$$P_s = f_s \, V_{rm} \, \frac{t_r}{2} \left[\frac{1}{t_r^{0.265}} - 1 \right]^2 I_L \qquad 4.2\text{–}20$$

The reverse maximum voltage is guaranteed to be clamped to 450V by an active snubbing circuit as shown in Figure 4.7. Using the data from section 4.1 and substituting from equation 4.2–18 into 4.2–20:

$$P_s = 0.72 \, \frac{2E \; C_s}{\left[t_{mf} - \frac{t_f}{2} \right]}$$

$$P_s = 0.6E \; C_s$$

$$C_s - (\mu F)$$

At the maximum bus voltage (E=336V):

$$P_s \approx 200 \; C_s \qquad 4.2\text{–}21$$

$$C_s - (\mu F)$$

The conduction loss would be given by:

$$P_c = I_L \, t_{mf} \, f_s \, V_f$$

V_f – Diode average forward voltage

This neglects that the average current carried by D_s during the period t_1 to t_2 is less than I_L and therefore overestimates the loss. Substituting equation 4.2–15:

$$P_c = \frac{2E \; C_s}{\left[t_{mf} - \frac{t_f}{2}\right]} \, t_{mf} \, f_s \, V_f \qquad 4.2\text{–}22$$

The average forward voltage is 1.8V @$T_j = 125^oC$. Substituting the values from section 4.1 into 4.2–22 yields:

$$P_c = 55 \; C_s \qquad 4.2\text{–}23$$

C_s – (μF)

The total loss from equations 4.2–18 and 4.2–20 will therefore be:

$$P_t = 255 \; C_s \qquad 4.2\text{–}24$$

C_s – (μF)

The diode D_s consists of two series DSE60–10A diodes each insulated from the heatsink by silicon pads, therefore:

$$T_j = P_t \, [R_{th_{j\text{-}c}} + R_{th_{c\text{-}h}}] + T_h$$

$$T_j = P_t\,[0.75 + 0.75] + 80$$

$$T_j = 255\ C_s\,[0.75 + 0.75] + 80$$

$$T_j = 383\ C_s + 80 \qquad 4.2\text{–}25$$

$$C_s - (\mu F)$$

The diode D_s junction temperature for the three values of snubber capacitance is presented in Table 4.1.

$C_s(\mu F)$	$T_j(^oC)$
0.03	92
0.05	99
0.07	107

Table 4.1 Diode D_s worst case junction temperature for Cs equal to 0.03,0.05 and 0.07 μF

The choice of C_s as $0.05\mu F$ is quite a safe selection for this operating condition, actually a higher value of C_s could be used which would further reduce the switching loss for the IGBT. However, as previously mentioned the value of C_s effects the operation of the resonant reversal circuit and it can be shown that the value of $0.05\mu F$ on balance is a good selection. This will be explored in more detail in the next section.

The effect of changing the value of L_f on the total diversion time is shown in Figure 4.5. The value of L_f mainly effects the commutation time near the top of the load range and is most likely to cause a problem at the maximum current. At low load currents its effect is minor. It can be seen that the choice of $L_f = 2\mu H$ is appropriate since it allows the load current to surge to around 130A at the nominal bus voltage before there is a minimum off time violation.

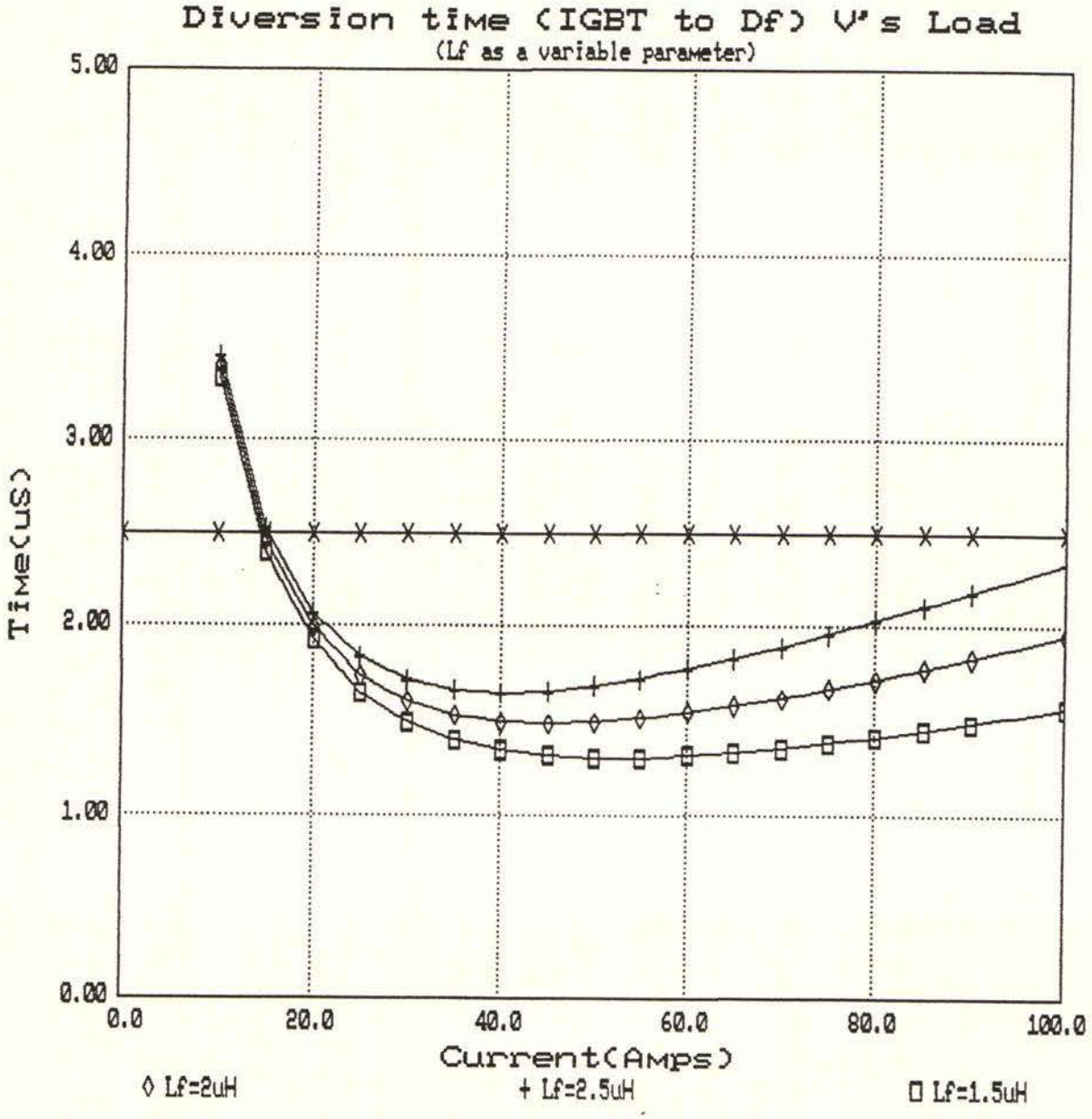


Figure 4.5 Effect of Lf on the Total IGBT to Df Diversion Time

Such an event will cause a very high reverse recovery current in the clamp diodes D_c. This case is substantially more severe then the last case since the diode could be carrying a large percentage of the full load current if L_f is selected too large. The philosophy in this instance was to select L_f such that in the worst case under continuous operating conditions the minimum off time would not be violated.

Figure 4.6 shows the diversion time as a function of load current for the "as built" values with the bus voltage as a parameter. At full load and minimum bus voltage the diversion time is longest but has sufficient margin from the 2.5μS limit if L_f is selected to be 2μH. However making L_f any larger would be unacceptable. Under surge conditions the limit will be violated. It is necessary to check that under surge conditions that the switching loss is not high. The requirement is that at the maximum surge current of 150A the junction temperature should not exceed 125^{0}C. The losses in diode D_c under surge conditions will now be checked. Since I_L is much greater than V_c/Z_s the diversion time is closely approximated to :

$$T_d = \frac{t_f}{2} + \frac{C_s}{I_L}[2E + V_c] + \frac{I_L L_f}{V_c} \qquad 4.2\text{–}26$$

And the initial current in D_c can be approximated to I_L. The current being carried by D_c during time t_4 will be given by:

$$i_{D_c}(t) = I_L - \frac{V_c}{L_f} t \qquad 4.2\text{–}27$$

Therefore at time t_{mf} the current in D_c will be given by:

$$i_{D_c}(t_{mf}) = I_L - \frac{V_c}{L_f}\{t_{mf} - [\frac{t_f}{2} + \frac{C_s}{I_L}(2E + V_c)]\}$$

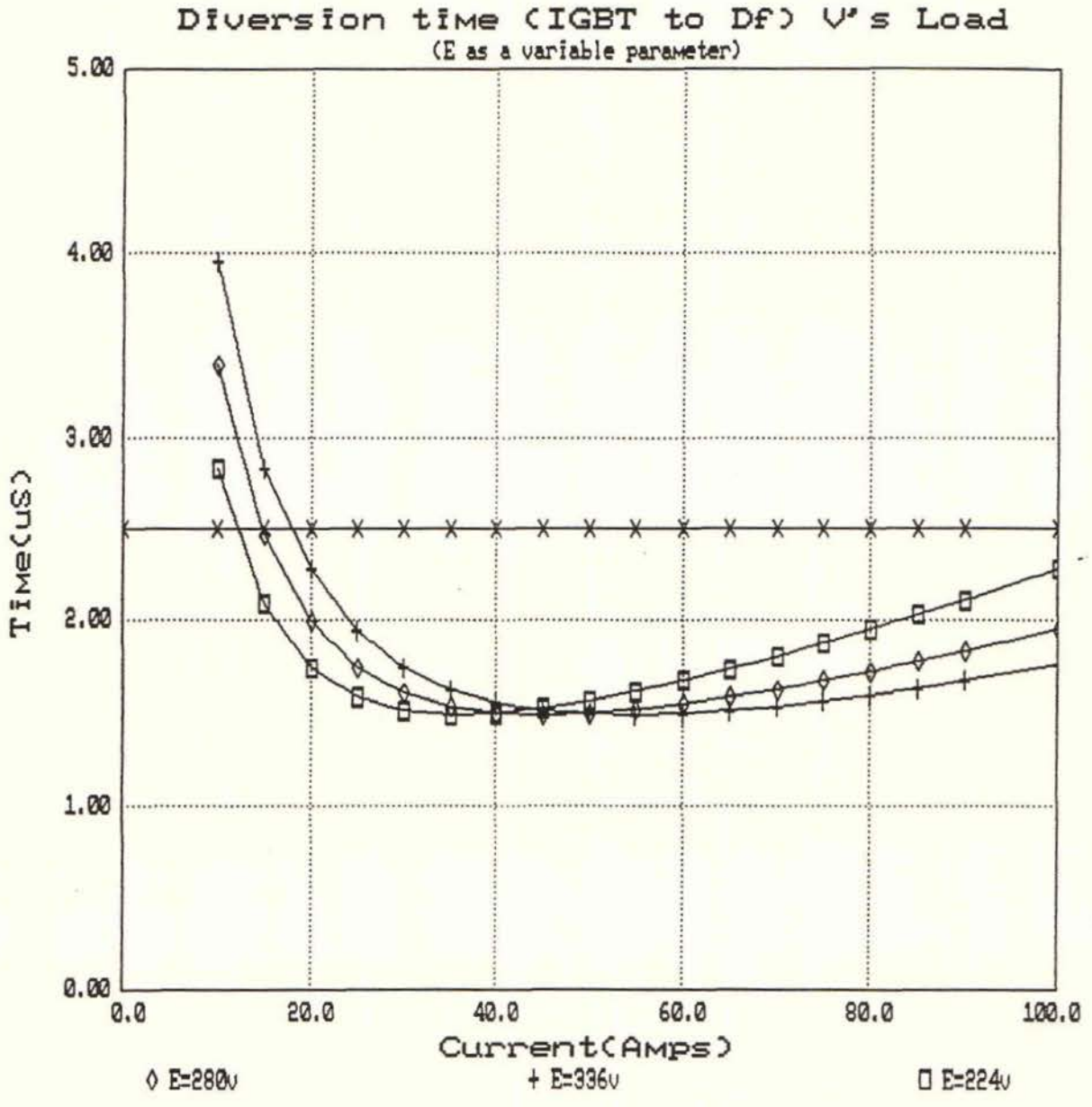


Figure 4.6 Effect of the Bus Voltage on the Total IGBT to Df Diversion TIme

The rate of decay of the forward current in D_c once the IGBT turns on will as before be:

$$\frac{di(t)}{dt} = m = \frac{i_{D_c}(t_{mf})}{t_r}$$

In this case because the calculation is more critical the exact value for I_{rm} will be calculated using table 3.1. the worst case conditions will be assumed:

$$V_c = 104V \text{ (i.e. minimum bus voltage)}$$

$$I_L = 150A(\text{surge current})$$

Also D_c is constructed from two parallel diodes. Therefore:

$$i_{D_c}(t_{mf}) = I_L - \frac{V_c}{L_f}\{t_{mf} - [\frac{t_f}{2} + \frac{C_s}{I_L}(2E + V_c)]\}$$

$$i_{D_c} = 150 - \frac{104}{2} \times [2.5 - (0.1 + 0.184)]$$

$$= 34.8A(17.4A \text{ per diode})$$

$$m = \frac{i_{D_c}(t_{mf})}{t_r}$$

$$= \frac{34.8}{0.15} = 232.0A/\mu S(116.0A/\mu S \text{ per diode})$$

$$T_o = \frac{I_f}{m} = \frac{34.8}{232.0} = 0.15\mu S$$

From Chapter Three:

$$T_t \text{ (diode transit time)} = 0.13\mu S \ @T_j = 125^oC$$

Therefore:

$$\frac{T_o}{T_t} = \frac{0.15}{0.13} = 1.15$$

From table 3.1:

$$\frac{T_x}{T_t} = 1.85$$

$$T_x = 1.85 \times T_t = 1.85 \times 0.13 = 0.24\mu S$$

$$I_{rm} = m\, T_x - I_f = 116.0 \times 0.24 - 17.4 = 10.4A \text{ per diode}$$

The switching loss will be given as before by:

$$P_s = f_s\, V_{rm}\, \frac{I_{rm}^2}{2m}$$

$$= 0.05 \times 450 \times \frac{10.4^2}{2 \times 116} = 10.5 \text{ watts}$$

The conduction loss will be determined by the average current flowing in D_c during the IGBT off time and the average forward drop in the diodes.

An average forward drop of 1.8V@$T_j = 125^oC$ will be assumed:

$$P_c = I_{avg}\, t_{mf}\, V_f\, f_s$$

$$I_{avg} = \frac{I_L + I_{D_c}(t_{mf})}{4}$$

$$= \frac{150 + 34.8}{4} = 46.2\text{A per diode}$$

$$P_c = 46.2 \times 2.5 \times 1.8 \times 0.05 = 10.4 \text{ watts}$$

The total loss will therefore be:

$$P_t = 10.5 + 10.4 = 20.9 \text{ watts}$$

The diodes are again isolated from the heatsink by silicone pads, so therefore:

$$T_j = P_t[R_{th_{j\text{-}c}} + R_{th_{c\text{-}h}}] + 80$$
$$= 20.9\times[0.75+0.75]+80= 111^oC$$

This is satisfactory, however it should be pointed out that had only a single set of series diodes been used the junction temperature would have been around 135^oC which was considered not to be sufficient margin.

The analysis above shows in so far as the minimum off time constraint and the IGBT snubbing efficiency is concerned the selection of C_s and L_f are appropriate. However further discussion of the selection of these in reference to other relevant aspects of the converter will be made in subsequent sections.

4.3 Snubber Module Design

In this section the design of the snubber module including D_{s1}/D_{s2},C_s,D_r and L_r will be examined based on the selection of 0.05 μF for the value of C_s. Shown in Figure 4.7 is a schematic diagram of the snubber module. First the design of the resonant resetting system will be discussed. The voltage across C_s must be reset from $-(E + V_c)$ to $+E$ within the IGBT minimum on time. If this does not occur the IGBT will be subjected to a step voltage at turn off resulting in increased switching losses. The resonant reversal process is illustrated in Figure 4.8 with waveforms being shown in Figure 4.9. During period t_1 to t_2 the inductor L_r and capacitor C_s form a series resonant circuit with an initial capacitor voltage of $-(E + V_c)$. This will resonantly reverse to $+E$ at which time there will be a current I_a flowing in L_r. The energy stored in L_r associated with I_a, E_a is equal to the additional energy stored in the C_s during the IGBT turn off.

That is:

$$E_a = \frac{1}{2}L_r I_a^2 = \frac{1}{2}C_s[V_c + E]^2 - \frac{1}{2}C_s E^2 \qquad 4.3\text{–}1$$

After t_2 the diode D_s is forward biased and the inductor current decreases linearly to zero at a rate determined by E/L_r, this occurs during the period t_2 to t_3. The energy E_a is returned to the supply. Disregarding the small device losses, the snubber is lossless.

In the following analysis the time period t_1 to t_2 will be denoted t_r, the period t_2 to t_3 will be denoted t_L and the period t_1 to t_3 will be denoted t_w. The total time t_w must be less than the IGBT minimum on time. During the interval t_1 to t_2 the inductor current is given by:

$$i_{L_r}(t) = \frac{E + V_c}{Z_r} \mathrm{Sin}(\omega_r t) \qquad 4.3\text{–}2$$

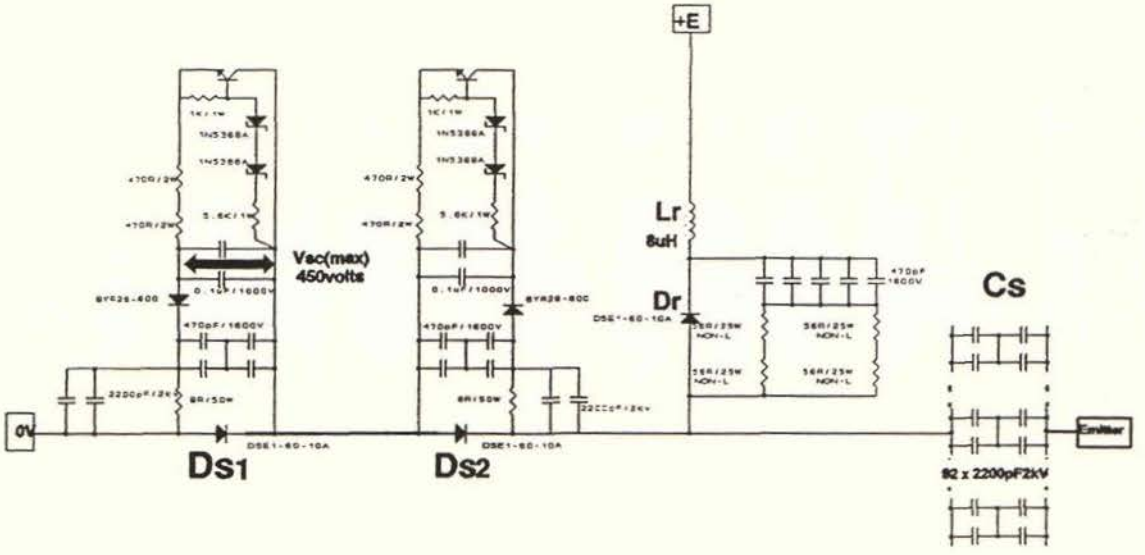
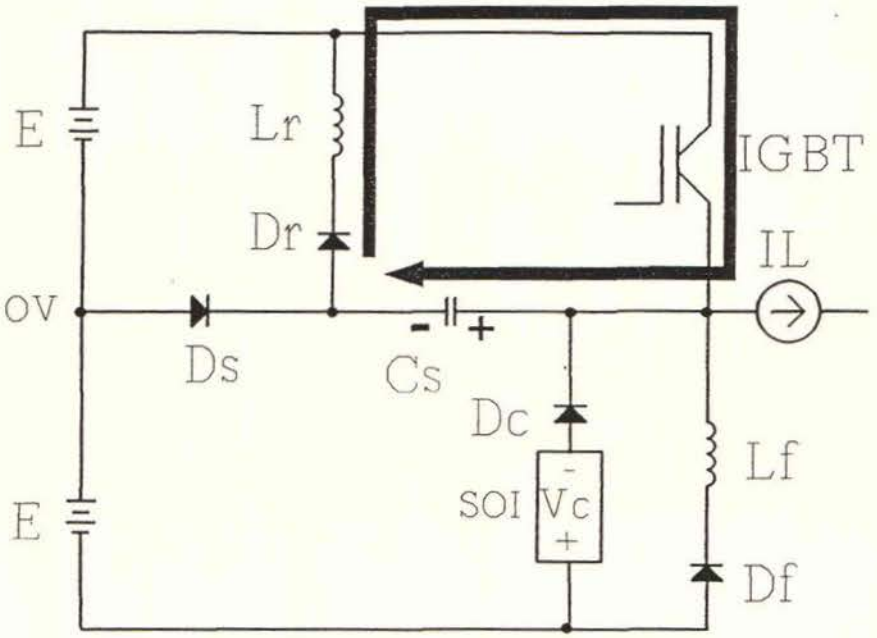


Figure 4.7 Snubber Module Schematic

$t_1 < t < t_2$



$t_2 < t < t_3$

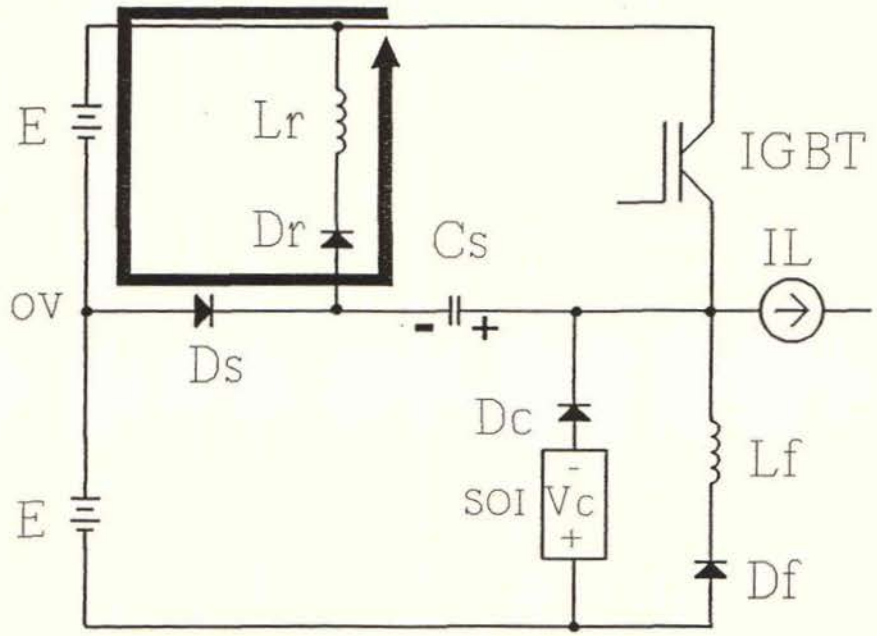


Figure 4.8 Snubber Resonant Reversal Operation

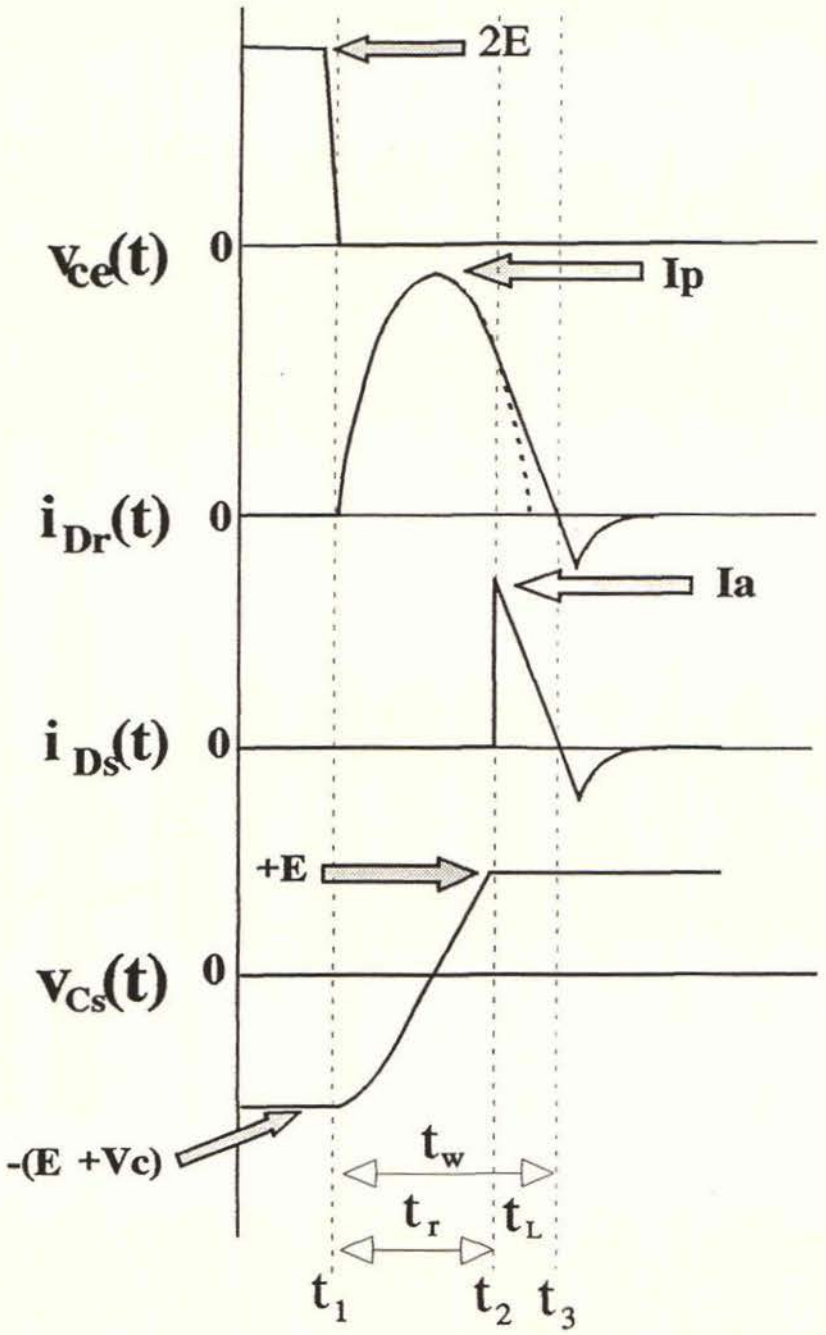


Figure 4.9 Snubber Resonant Reversal Waveforms

For $L_r = 8\mu H$ and $C_s = 0.05\mu F$:

$$Z_r = \sqrt{\frac{L_r}{C_s}} = \sqrt{\frac{8}{0.05}} = 12.65\Omega$$

$$\omega_r = \frac{1}{\sqrt{L_r C_s}} = \frac{1}{\sqrt{8 \times 0.05}} = 1.58 \text{ Mrad/s}$$

The peak current carried by the diode D_r at the highest bus voltage is:

$$I_p = \frac{E + V_c}{Z_r} = \frac{336 + 156}{12.65} = 38.9A$$

At this time it is worth making the point that I_p and the maximum reverse recovery current in D_f occur almost simultaneously This means the IGBT will have to carry a maximum current of $I_L + I_{rm} + I_p$ which will exceed 200A under surge conditions. This has a bearing on the choice of L_r and even C_s since these values effect the peak current. In this respect the values chosen yielded satisfactory results. The values chosen yield satisfactory results.

The capacitor voltage will be given by:

$$v_{C_s}(t) = -(E + V_c)\,\text{Cos}(\omega_r t) \qquad 4.3\text{–}3$$

The time t_r can be found from equation 4.3–3:

$$E = -(E + V_c)\,\text{Cos}(\omega_r t_r)$$

$$t_r = \frac{1}{\omega_r}\,\text{Cos}^{-1}\left[\frac{-E}{E + V_c}\right] \qquad 4.3\text{–}4$$

The current I_a being carried by L_r at t_2 from Equations 4.3–2 and 4.3–4 will be given by:

$$i_{L_r}(t_2) = I_a = \frac{E + V_c}{Z_r} \text{Sin} \{\text{Cos}^{-1} \left[\frac{-E}{E + V_c}\right]\}$$

$$I_a = \frac{E + V_c}{Z_r} \frac{\sqrt{V_c(E + V_c)}}{E + V_c}$$

$$I_a = \frac{\sqrt{V_c(E + V_c)}}{Z_r} \qquad 4.3–5$$

$$I_a = \frac{\sqrt{156(336+156)}}{12.65} = 21.9\text{A}$$

The time period t_2 to t_3 during which the inductor current decays linearly to zero and energy is returned to the supply will be given by:

$$t_L = \frac{I_a L_r}{E} = \frac{L_r}{E} \frac{\sqrt{V_c(E + V_c)}}{Z_r}$$

$$t_L = \frac{\sqrt{V_c(E + V_c)}}{\omega_r E} \qquad 4.3–6$$

A major requirement is that t_w be less than 2.5μS under worst case conditions.

$$t_w = \frac{1}{\omega_r} \text{Cos}^{-1} \left[\frac{-E}{E + V_c}\right] + \frac{\sqrt{V_c(E + V_c)}}{\omega_r E} \qquad 4.3–7$$

$$t_w = \frac{1}{1.58} \times \text{Cos}^{-1}\left[\frac{-336}{336 + 156}\right] + \frac{\sqrt{156(336+156)}}{1.58 \times 336} = 2\mu\text{S}$$

This gives adequate margin from the minimum IGBT on time of 2.5μS to allow for component variations. The reverse recovery loss in diode D_r can now be evaluated. Diode D_s is in series with D_r during this period, reverse current will be established in both diodes after t_3, however D_s recovers into zero volts and therefore experiences no loss whereas D_r recovers into E regardless of whether D_s recovers first or not. Therefore the switching losses in D_r are not effected by the behavior of D_s.

Because the current wave shape is sinusoidal for the purposes of the reverse recovery calculation the forward current will be taken to be the average for the period t_1 to t_2 and the dI/dt to be the slope of the linear portion of the current decay.

The average current is calculated as follows:

$$i_{L_r}(t) = \frac{E + V_c}{Z_r} \mathrm{Sin}(\omega_r t)$$

$$I_{avg} = \frac{1}{t_r} \frac{E + V_c}{Z_r} \int_0^{t_r} \mathrm{Sin}(\omega_r t)\, dt$$

$$I_{avg} = \frac{1}{t_r} \frac{2E + V_c}{Z_r \ \omega_r} \qquad 4.3\text{–}8$$

$$I_f = I_{avg} = \frac{1}{1.47} \times \frac{672 + 156}{12.65 \times 1.58} = 28.2\mathrm{A}$$

The dI/dt is given by:

$$\frac{dI}{dt} = m = \frac{E}{L_r} = \frac{336}{8.0} = 42.0\ \mathrm{A}/\mu\mathrm{S}$$

Using the methods outlined in Chapter 3:

$$T_t(\text{DSEI60–10A}) = 0.13\mu S \ @T_j = 125^oC$$

$$T_o = \frac{I_f}{m} = \frac{28.2}{42.0} = 0.67\mu S$$

$$\frac{T_o}{T_t} = \frac{0.67}{0.13} = 5.15$$

From Table 3.1

$$\frac{T_x}{T_t} = 5.9$$

$$T_x = T_t \times 5.9 = 0.13 \times 5.9 = 0.77\mu S$$

$$I_{rm} = m\ T_x - I_f = 42 \times 0.77 - 28.2 = 4.1\ A$$

The maximum reverse voltage for D_r is E so the switching losses assuming instantaneous rise of the reverse voltage would be given by:

$$P_s = f_s\ V_{rm}\ \frac{I_r^2}{2} = 0.05 \times 336 \times \frac{4.1^2}{2\times 42} = 3.4 \text{ watts}$$

The conduction losses for D_r will now be calculated, also assuming a junction temperature of 125^oC. The average current during t_1 to t_2 has already been calculated, the RMS current will be found as follows:

$$I_{rms} = \sqrt{\frac{1}{t_r}\int_0^{t_r}\left[\frac{E + V_c}{Z_r}\ \text{Sin}(\omega_r t)\right]^2\ dt}$$

$$I_{rms} = \frac{E + V_c}{Z_r} \sqrt{\left[\frac{1}{2} - \frac{\mathrm{Sin}(2\omega t_r)}{2\omega_r t_r} \right]} \qquad 4.3\text{–}9$$

$$I_{rms} = \frac{336 + 156}{12.65} \sqrt{\left[\frac{1}{2} - \frac{\mathrm{Sin}(2 \times 1.58 \times 1.47)}{2 \times 1.58 \times 1.47} \right]}$$

$$= 32.9 \text{ A}$$

The conduction loss associated with t_r is therefore:

$$P_c(t_r) = V_{to}\, I_{avg} \frac{t_r}{T} + R_f I_{rms}^2 \frac{t_r}{T} \qquad 4.3\text{–}10$$

From Chapter Three the diode forward voltage and resistance will be given by:

$$V_{to} = -3\times10^{-3}\, T_j + 1.85\text{V} = 1.48\text{V} \quad @T_j = 125^{o}\text{C}$$

$$R_f = 6\times10^{-3}\ \Omega$$

Therefore:

$$P_c(t_r) = 1.48 \times 28.2 \times \frac{1.47}{20} + 6\times10^{-3} \times 32.9^2 \times \frac{1.47}{20}$$

$$= 3.5 \text{ watts}$$

The conduction losses during period t_L will be given by:

$$P_c(t_L) = V_{to} \frac{I_a}{2} \frac{t_L}{T} + R_f \frac{I_a^2}{3} \frac{t_L}{T} \qquad 4.3\text{–}11$$

$$P_c(t_L) = 1.48 \times \frac{21.9}{2} \times \frac{0.52}{20} + 6\times10^{-3} \times \frac{21.9^2}{3} \times \frac{0.52}{20}$$

$$= 0.45 \text{ watts}$$

The total loss in diode D_r will be:

$$P_t = P_s + P_c(t_r) + P_c(t_L)$$
$$= 3.4 + 3.5 + 0.45 = 7.4 \text{ watts}$$

The diode is isolated from the heatsink by a silicon pad so the junction temperature will be given by:

$$T_j = P_t(R_{th(j-c)} + R_{th(c-h)}) + T_h$$
$$= 7.8(0.75 + 0.75) + 80^{\circ}C$$
$$= 91.0\ ^{\circ}C$$

Since this is much lower than the assumed junction temperature the conduction losses would be higher but the switching losses would be lower, the result being that the actual figure would still be close to 91°C. As long as T_j is less than 125°C under worst case conditions the design is considered to be safe.

The losses in diode D_s can now be calculated. The diode D_s only has significant switching loss when the minimum off time limit is violated which occurs at load currents of less than 15A as discussed in Section 4.2. Above 15A the losses in D_s are dominated by conduction losses. Losses due to the forward recovery will be neglected since they are thought to be less than 1 watt at full load. During the period t_1 to t_2 of Figure 4.3 the current in D_s rises linearly to the full load current over t_f. The loss associated with this will be given by:

$$P_1 = V_{to} \frac{I_L}{2} \frac{t_f}{T} + R_f \frac{I_L^2}{3} \frac{t_f}{T} \qquad 4.3\text{–}12$$

From Chapter Three the DSEI60–10A forward characteristics are as follows:

$$V_{to} = -3\times10^{-3}\ T_j + 1.85V = 1.48V\ @T_j = 125^{\circ}C$$
$$R_f = 6\times10^{-3}\Omega$$

During the period t_2 to t_3 of Figure 4.3 the current in D_s is constant and equal to the load current. Therefore:

$$P_2 = V_{to}\, I_L \frac{t_L}{T} + R_f\, I_L^2 \frac{t_L}{T} \qquad 4.3\text{–}13$$

The time required can be found using equation 4.2–7 will be:

$$t_L = \frac{2E\ C_s}{I_L} - \frac{t_f}{2}$$

Therefore:

$$P_2 = f_s \left[\frac{2E\ C_s}{I_L} - \frac{t_f}{2} \right] [V_{to}\, I_L + R_f\, I_L^2] \qquad 4.3\text{–}14$$

The diode D_s also carries current during the resonant resetting period as indicated previously. The conduction loss associated with this as it was for D_r will be:

$$P_3 = P_c(t_L) = V_{to} \frac{I_a}{2} \frac{t_L}{} + R_f \frac{I_a^2}{3} \frac{t_L}{T}$$

$$P_3 = 0.87 \text{ watts}$$

This is independent of the load current. The total conduction loss can be shown to be:

$$P_t = P_1 + P_2 + P_3$$

$$P_t = f_s\, [\, 2EC_sV_{to} + 2EC_sR_fI_L + \frac{-t_fR_f}{6} I_L^2] + P_3$$

$$P_t = 0.05 \times [\, 49.7 + 0.2\, I_L - 2\times10^{-4}\, I_L^2] + P_3$$

The square term is small compared with the others. The conduction losses increase weakly with load and have a large constant component. The total loss at full load will be:

$$P_t = 0.05 \times [\, 49.7 + 0.2 \times 100 - 2e{-}4 \times 100^2] + 0.87 = 4.3 \text{ watts}$$

It can be seen that full load is not the worst case operating condition for diode D_s. In Section 4.3 it was found at low load currents the switching loss becomes substantially greater than the value above.

While the value of C_s has been established the exact specification of C_s needs to be carefully examined. The losses in C_s can be dangerously high if it is not selected correctly. In fact no single capacitor had the capability required, and multiple capacitors were used. Dielectric losses cause capacitor self heating which, if not allowed for will cause a thermal runaway effect and failure to occur. Manufacturers usually state the losses for sinusoidal excitation as Tan δ which is the ratio of active to reactive power:

$$P = Q \text{ Tan } \delta$$

A low loss capacitor therefore has a low Tan δ, polypropylene capacitors for example have values below 1×10^{-3} as compared to electrolytic capacitors which may approach 0.1. The Tan δ is known to increase with operating frequency, the relationship normally being assumed to be linear:

$$\text{Tan } \delta = \text{Tan } \delta_0 + k\, f$$

Tan δ_0 – low frequency value of Tan δ

k – proportionality constant

In this application the excitation is squarewave rather than sinewave so more than a single frequency is involved. In order to calculate the exact dielectric losses for squarewave excitation it is necessary to calculate the the losses for each harmonic and form an addition. An approximate solution for the dielectric power loss for squarewave excitation is , [34].:

$$P = \frac{\pi}{4} C f_s (\Delta V)^2 \text{ Tan } \delta_0 + \frac{k}{2\pi C} I^2 \qquad 4.3\text{–}15$$

∇V – Voltage swing

I – RMS current

For this case the voltage swing from Figure 4.3 is $(2E + V_c)$. The rms current can be calculated from observation of the current waveform. There are two periods when the current flows in the capacitor. First when the IGBT turns off the current is approximately square in shape with a height equal to the load current for a duration t_s determined by equations 4.2–5, 4.2–7 and 4.2–11:

$$t_s = \frac{t_f}{2} + \frac{2E\ C_s}{I_L} + \frac{1}{\omega_s} \text{Sin}^{-1}\left[\frac{V_c}{Z_s\ I_L}\right] \qquad 4.3\text{–}16$$

The rms value for the period t_s is equal to the load current I_L. The second time that C_s carries current is during the resonant resetting period. The rms current for this period has already been derived equation 4.3–9 when the conduction losses for diode D_r were being calculated. This current can be assumed to be independent of the load and in the worst case is $I(t_r)_{rms} = 32.9A$ for a period of $t_r = 1.47\mu S$ as previously calculated. The resultant rms current for the two components can be calculated as follows:

$$I_{rms} = \sqrt{\frac{t_s}{T} I_L^2 + \frac{t_r}{T} I(t_r)_{rms}^2} \qquad 4.3\text{–}17$$

At full load current t_s will be:

$$t_s = \frac{t_f}{2} + \frac{2E\ C_s}{I_L} + \frac{1}{\omega_s} \mathrm{Sin}^{-1}\left[\frac{V_c}{Z_s\ I_L}\right]$$

$$t_s = \frac{0.2}{2} + \frac{672 \times 0.05}{100} + \frac{1}{3.16} \mathrm{Sin}^{-1}\left[\frac{156}{6.32 \times 100}\right] = 0.52\mu S$$

At full load the effective current carried by C_s is:

$$I_{rms} = \sqrt{\frac{t_s}{T} I_L^2 + \frac{t_r}{T} I(t_r)_{rms}^2}$$

$$I_{rms} = \sqrt{\frac{0.52}{20} \times 100^2 + \frac{1.47}{20} \times 32.9^2} = 18.4\ A$$

Therefore from equation 4.3–15 the dielectric loss in the worst case would be given by:

$$P = \frac{\pi}{4} C_s f_s (2E + V_c)^2 \mathrm{Tan}\ \delta_o + \frac{k}{2\pi\ C_s} 18.4^2$$

$$P = \frac{\pi}{4} \times 0.05 \times 0.05 \times (672 + 156)\ \mathrm{Tan}\ \delta_o + \frac{18.4^2}{2\pi \times 0.05 \times 10^{-6}} k$$

$$P = 1346\ \mathrm{Tan}\ \delta_o + 1078 \times 10^{-6}\ k \qquad 4.3\text{–}18$$

The best available capacitor has the following characteristics, [38]:

$$\mathrm{Tan}\ \delta_o = 0.3 \times 10^{-3} \quad @\ f = 1kHz$$

$$k = 1.2 \times 10^{-8}$$

This would result in:

$$P = 1346\ \mathrm{Tan}\ \delta_o + 1078 \times 10^{-6}\ k$$

$$P = 1346 \times 0.3 \times 10^{-3} + 1078 \times 10^{-6} \times 1.2 \times 10^{-8} = 13.33\ \mathrm{watts}$$

This verifies that a single capacitor would be grossly overloaded. In addition to this Roderstien, [38] do not recommend operating voltages greater than $500V_{rms}$ for their 2kV rated capacitors in 50kHz sinewave applications. This suggested that two series capacitors would be required plus a number of parallel paths to reduce the effective current in each capacitor. The real strength in using multiple capacitors lies in the increased surface area available for dissipation of heat. Availability dictated the use of 2200pF 2kV (MKP 1841) capacitors in a series parallel array (46 parallel paths ; two series capacitors) to build up the 0.05 μF capacitor. This would reduce the effective current in each capacitor to 0.4A and the voltage swing to 414V so that the loss per capacitor would now be:

$$P = \frac{\pi}{4} \times 2.2\times10^{-9} \times 0.05\times(414)^2\times 0.3\times10^{-3} + \frac{0.4^2}{2\pi \times 2.2\times10^{-9}} 1.2\times10^{-8}$$
$$= 0.14\text{watts}$$

The total loss would therefore be, 92 × 0.14 which is equal to 12.9watts. Which is the same as before but in the multiple capacitor case this power is dissipated over a substantially greater surface area. The surface area of the 92 capacitors is approximately $0.044m^2$. The following equation relates the temperature rise to power dissipation for natural convection cooling, [39]:

$$\Delta T = \left[\frac{P}{3\ A}\right]^{0.8} = \left[\frac{12.9}{3 \times 0.044}\right]^{0.8} = 39.1^{o}C \qquad 4.3\text{–}19$$

Assuming $50^{o}C$ ambient temperature the capacitor temperature would be approximately $90^{o}C$. Since this is a worst case condition and the capacitors are rated for operation at $100^{o}C$, the selected configuration will be conservative. A conservative approach is necessary since these capacitors must be mounted close to the IGBT for the snubber to be effective, which means ambient temperatures are high. Also a significant amount of heat will be conducted to the capacitor by the connection from the IGBT which contributes to this temperature rise.

4.4 Clamping System Design

The IGBT clamping system consists of diode D_c and the Self oscillating inverter (SOI). The reverse maximum voltage subjected to the diode D_c is $2E + V_c = 828V$ plus any overshoot due to forward recovery and stray inductance. This was considered to be to high for a single 1000V diode. Hence two diodes are used in series with appropriate voltage sharing/clamping networks. Additionally under surge conditions these diodes are subjected to high switching loss as well as high conduction losses. To accommodate this two parallel paths were required as discussed in Section 4.2. Figure 4.10 shows the complete snubber module including the current balancing transformer which forces dynamic current sharing between the parallel sets. The losses under the worst case condition have already been calculated in Section 4.2 an so they are not repeated here. However as part of the cooling requirement calculation the losses in D_c will be calculated at full load and 50% duty ratio in a later Section 4.7.

Shown in Figure 4.11 is a schematic diagram of the 500 watt self oscillating converter (SOI) which provides the clamping action on the IGBT collector emitter voltage during turn off. The self oscillating type converter is ideal for this application as it is self contained requiring no control circuitry, [9]. This makes it very robust in the high EMI environment where it must work. The output section of the SOI is a simple bridge rectifier which feeds the DC bus. The DC bus voltage via the transformer turns ratio is reflected to the input. This makes the clamp voltage equal to (13/28)×E. The voltage across the input capacitors $C_3 - C_{12}$ is voltage stiff. This is necessary since it is being supplied from essentially a pulsed current source. Because the SOI must be located some distance from the power circuit local decoupling capacitors were also necessary as shown in Figure 4.10.

The series inductor L_3 acts to smooth the the input current to the SOI.

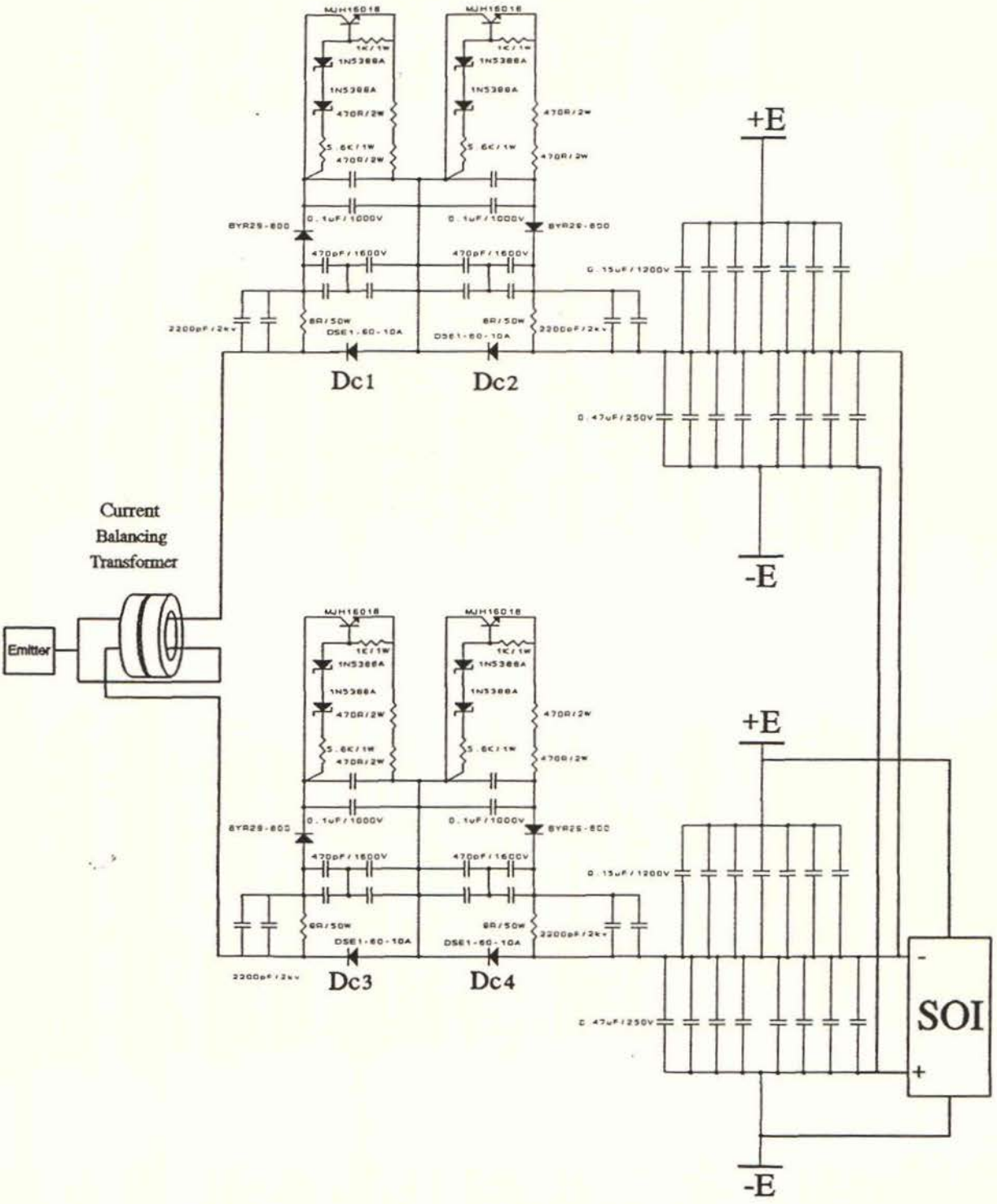


Figure 4.10 Clamp Module Schematic

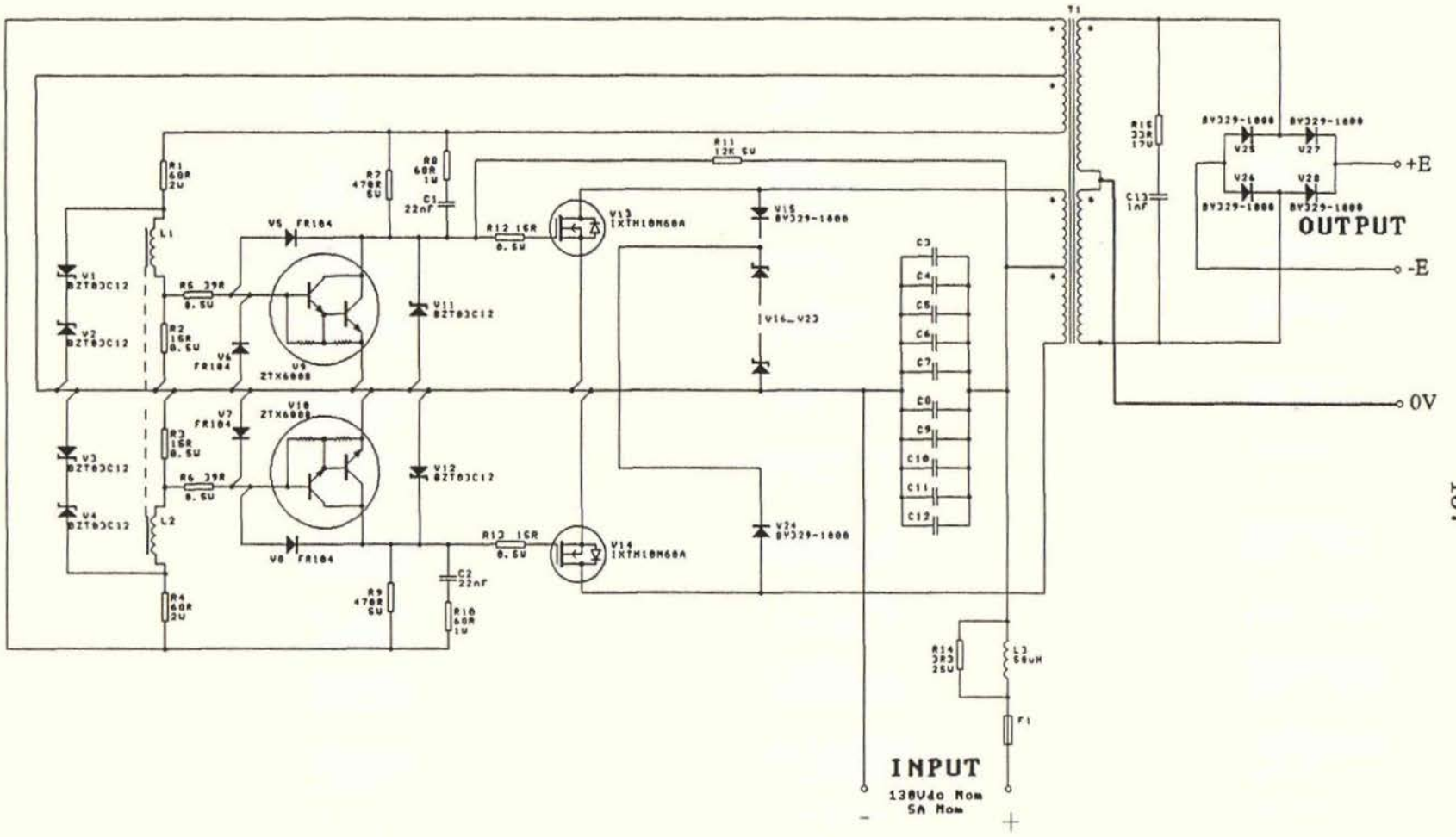


Figure 4.11 500watt Self Osccillating Inverter Schematic

The pulsed currents are absorbed by the local decoupling capacitors which are sized to limit the resulting voltage ripple to a low level. A relatively constant DC current flows to the SOI via L_3 into a constant voltage determined by the bus voltage. Resistor R_{14} of Figure 4–11 provides damping for the L–C circuit formed. The SOI uses saturation of an auxiliary inductor L_1/L_2 to provide the necessary positive feedback to give oscillation. This is similar in principle to the use of an auxiliary transformer, [9]. The traditional self oscillating converter relies on saturation of the main transformer for its operation. This however results in very high core losses and unacceptable operating temperatures. The auxiliary transformer overcomes this problem since only it saturates while the main transformer can be designed to run at much lower peak flux levels.

The SOI is started by R_{12} feeding a current to the gate of V_{13}. The resistance from V_{13} gate to ground is 470Ω, (R_7 via feedback winding on T1). This means that an input voltage of around 75V is necessary to obtain the mosfet threshold voltage of 3V. Once the mosfet starts to turn on, voltage is applied across the primary of T1 which excites the feedback winding. This causes the gate voltage of V_{13} to rise via the R_7,R_8/C_1 network, and hence the mosfet will turn solidly on. The R_8/C_1 series circuit quickens the charging of the fet gate. The Zener diode V_{11} clamps the gate voltage at a safe level. The other fet, V_{14}, is maintained in an off state by a negative voltage applied to its gate which is limited to 0.7V by V_{12} conducting in the forward direction. The feedback voltage also excites the coupled inductors L_1 and L_2.

The voltage applied across L_1/L_2 is maintained essentially constant by zener diodes V_1,V_2,V_3 and V_4. This makes the magnetisation of L_1/L_2 independent of the bus voltage and hence, the operating frequency is independent of the bus voltage. The current in L_1/L_2 rises linearly until saturation occurs. Under saturation the current increases rapidly. The inductor has been designed to saturate at 80mA which also corresponds to a 1.2V drop across R_2 (15Ω).

The voltage across R_2 drives the high gain darlington transistor V_9. Because of the saturation in the inductor the transistor is driven strongly and therefore turns on quickly. Once the transistor turns on the mosfet,V_{13}, gate voltage is removed and hence it is turned off. The magnetising flux in the main transformer T_1 which is at its peak level will cause a secondary current to be established such that V_{27} and V_{26} are forward biased. Hence the voltage across the winding reverses and the core begins to de–magnetise. The reversal of the voltage causes fet V_{14} to obtain positive gate drive and it switches on. The inductor L_1/L_2 now excited with a reverse voltage will eventually saturate in the opposite direction resulting in V_{14} being switched off and V_{13} switching on again. The saturation level of L_1/L_2 and the value of R_2/R_3 control the operating frequency. This is not effected by the bus voltage since the magnetising voltage for L_1/L_2 is clamped by zener diodes.

The inductor L_1/L_2 is ungapped and preferably should have a square B–H characteristic to provide high drive to the transistor. Siemens N30 material is appropriate, [9]. A Siemens RM10–N30 core was successfully used in this design. The oscillation frequency was set to be 30kHz. The main transformer is designed using normal high frequency design techniques, the core being used is a Siemens EC–70 ; N27. The average current input to the SOI at full load can be calculated as follows. From equation 4.2–15 and 4.2–16 the average current flowing through the clamp at high loads ($I_L >> \frac{V_c}{Z_s}$) is approximately:

$$I_{avg} \approx \frac{I_L}{2}$$

This current flows for the period t_4 to t_5 shown in Figure 4.3 which is given by:

$$t_5 - t_4 \approx \frac{I_L L_f}{V_c}$$

The charge transferred per cycle under the worst case conditions will be:

$$Q_c = \frac{I_L^2 \; L_f}{2 \; V_c} = \frac{100^2 \times 2}{2 \times 104} = 96\mu C$$

The SOI average current will therefore be:

$$I_{soi} = f_s \times Q_c = 0.05 \times 96 = 4.8A$$

This is calculated at the lowest bus voltage which yields the minimum operating clamp voltage (104V) and hence the maximum SOI current. The Power being transferred would be:

$$I_{soi} \; V_{soi} = \; 4.8 \times 104 = 499watts$$

Since as V_c increases the clamps current decreases the SOI power remains constant.

The complete SOI was accurately modeled using the Spice circuit simulation package, [16], prior to construction. In fact the prototype design was debugged using this simulation tool. This was a great advantage since no debugging was necessary on the actual unit. The simulation file together with the node diagram a presented in Appendix A.

Figure 4–12 shows a plot of the measured efficiency as a function of input current. It was found that the converter had a maximum efficiency of 92.5% at 3.25A falling off to 90% at 5A. Because the unit uses mosfets the low load efficiency is also quite good achieving 70% efficiency at 0.5A.

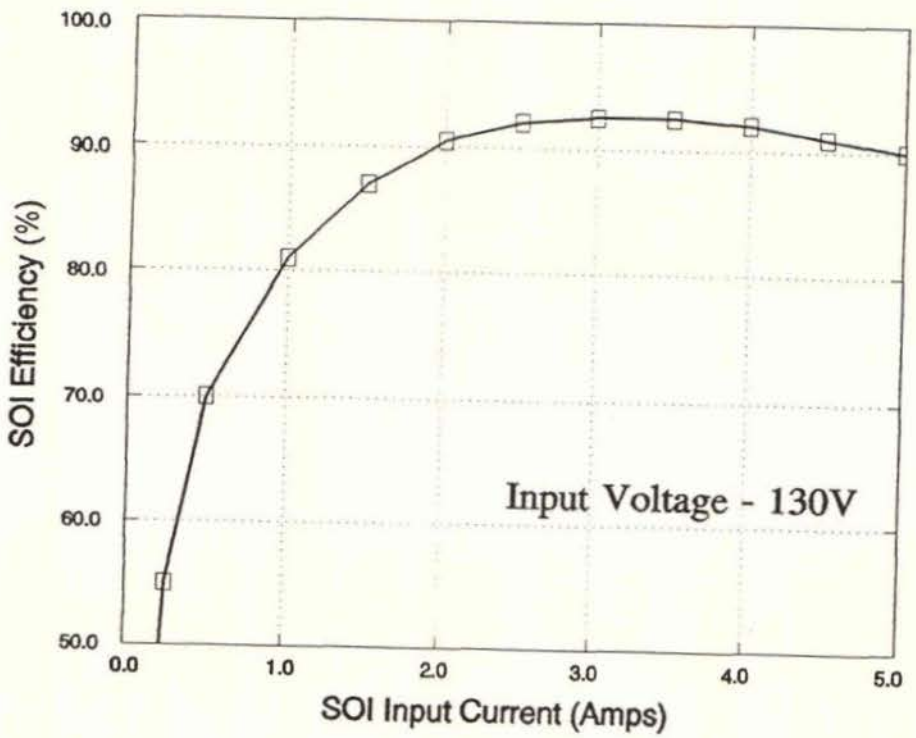


Figure 4.12 SOI Efficiency as a Function of Input Current

4.5 Freewheel Diode Module Design

Shown in Figure 4.13 is a schematic diagram of the freewheel diode module. Following is a brief description of the function of the components which make up this module. To obtain acceptable levels of stress on the components it was necessary to use a system of six parallel sets of two DSEI 60–10A diodes in series. Each diode has small individual snubbers to assist in dynamic voltage sharing and to assist in reducing the maximum reverse voltage at snap off. Diodes may not share reverse voltage in steady state due to differences in their reverse leakage currents. This is corrected by placing "swamping" resistors in parallel with the diodes.

Current flowing in each freewheel diode at snap off is diverted to individual clamp diodes which together form D_x. Capacitor C_x decouples the cathodes of D_x to the anodes of D_f and the energy originally stored in L_f is dissipated in R_x.

The resistors collectively denoted R_f have the function of forcing current sharing in the six parallel sets of diodes. This is necessary since the forward voltage drop can vary between diodes. Selection of R_f will now be considered. Selection of the value of R_f depends on the expected variation in the forward threshold potential V_{to} over the number of parallel diodes used. In many cases manufactures will give typical and maximum (90% Confidence) values for V_{to}. From this the variance and hence the standard deviation can be determined assuming a normally distributed population. The resistors R_f are than sized such that for the given variation in V_{to} the variation in I_d is an acceptable amount. A relationship relating the variance in diode forward current to the variance in forward voltage drop for a given value of series resistance is derived in Appendix B. This expression is shown to be:

$$\sigma_v = R\ \sigma_i \qquad 4.5\text{–}1$$

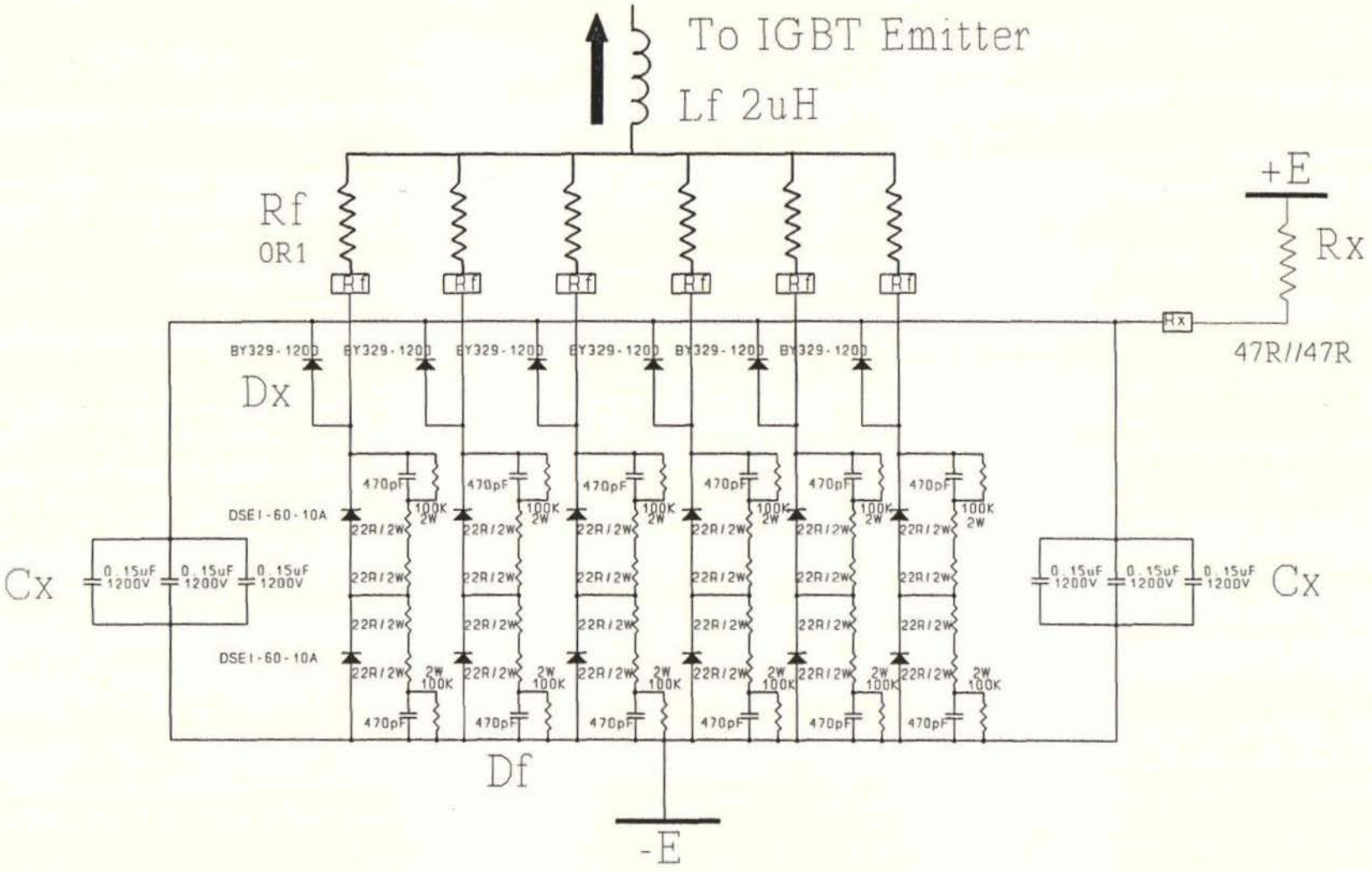


Figure 4.13 Freewheel Diode Module Schematic

Unfortunately the manufacturer of the DSEI60–10A diode only supplies a maximum value for V_{to}. Review of data from other diode manufacturers indicates that the typical standard deviation for V_{to} is 150mV, [20–22]. The Freewheel diode module is six sets of two series diodes. Two series diodes would exhibit a standard deviation of $\sqrt{2}$ times the standard deviation for a single unit. Therefore:

$$\sigma_v = \sqrt{2} \times 0.15 = 0.21V$$

The value of R_f was chosen to be 100mΩ which will now be shown to be an appropriate value. The mean current is given by:

$$\overline{I} = \frac{I_f}{n} = 16.67A \text{ @ } I_f = 100A \text{ and } n = 6(\text{six diodes})$$

From equation 4–2 the current standard deviation will be given by:

$$\sigma_i = \frac{\sigma_v}{R} = \frac{0.21}{0.1} = 2.1A$$

For 90% confidence the maximum current for any diode will be within 1.28 standard deviations of the mean assuming a normally distributed population, [40]. Therefore:

$$I_d = \overline{I} \pm 1.28\ \sigma_i = 16.67 \pm 1.28 \times 2.1 = 16.67 \pm 2.7A$$

This is 16% which represents an acceptable maximum deviation from the mean value.

The worst case power dissipation in R_f will be at the minimum duty ratio (12.5%) at the full rated output of 100A.

$$P = \left[\sqrt{1 - D}\ \frac{I_L}{n}\right]^2 R_f \qquad 4.5\text{–}2$$

$$P = \left[\sqrt{1 - 0.125\,\frac{100}{6}}\right]^2 0.1 = 24.3\text{watts}$$

The total power dissipation R_f is therefore 146 Watts at 100A . From the Arcol Metal Clad Resistor data sheet, [41], it can be deduced that the resistor element to case thermal resistance for 50 watt resistors are:

$$50\text{watt} \quad R_{th(e-c)} = 5^{O}\text{C/watt}$$

Also the maximum allowed internal element temperature (T_e) is 275^{O}C. All the metal clad resistors are mounted on the main heatsink. The assumed heatsink temperature as discussed in Section 4.1 is 80^{O}C, which means that $T_c = 80^{0}$C. Using this information the maximum internal element temperature will be:

$$T_e = P_e\, R_{th(e-c)} + T_c$$
$$T_e = 24.3 \times 5 + 80 = 202^{0}\text{C}$$

The freewheel diode temperature rise will now be calculated at a load of 100A and at the worst case duty ratio of 12.5%. The diode switching loss will be accurately calculated Using the method outlined in Chapter Three: From the DSE1 60–10A data sheet ,[19]:

$$I_{rm} = 32\text{A} \;@\; m = 480\text{A}/\mu\text{S},\; I_f = 60\text{A},\; T_j = 100^{O}\text{C}$$

A junction temperature of 125^{O}C will be assumed. The maximum bus voltage, 672V, will also be used since this represents the worst case. The calculation of the reverse maximum current is done in Appendix C and is shown to be 5.87A . The total freewheel diode maximum reverse current would then be 35.2A.

The switching component of the power loss assuming instantaneous rise of reverse voltage would be given by:

$$P_s = f_s V_{rm} Q_2$$

Assuming that $Q_1 = Q_2$:

$$Q_2 = Q_1 = \frac{I_{rm}^2}{2\ m}$$

$$= \frac{(5.87)^2}{2 \times 56.0} = 0.308\mu C$$

$$P_s = f_s V_{rm} Q_2$$

$$= 0.05 \times 336 \times 0.308 = 5.17 \text{watts}$$

The diode conduction loss will now be calculated according to Chapter Three:

$$I_{favg} = \frac{(1 - D) I_L}{6} \qquad 4.5\text{–}3$$

$$= \frac{(1\text{–}0.125)\ 100}{6} = 14.58 \text{Amps}$$

$$I_{favg} = \frac{\sqrt{1 - D}\ I_L}{6} \qquad 4.5\text{–}4$$

$$I_{frms} = \frac{\sqrt{1 - 0.125}}{6} \times 100 = 15.59 \text{A}$$

$$V_{to} = [-3\times10^{-3}\ T_j + 1.85]$$

$$R_f = 6\times10^{-3}$$

$$P_c = I_{favg} V_{to} + I_{frms}^2 R_f \qquad 4.5\text{–}5$$

$$P_c = 14.58 \times [-3\times10^{-3}\times 125 + 1.85] + 6\times10^{-3}\times (15.59)^2 = 23.0 \text{ watts}$$

The total loss per diode will be:

$$P_t = 23 + 5.17 = 28.2\text{watts}$$

And the total freewheel diode loss would be 338watts. The junction temperature rise would be determined by the total thermal resistance to the heatsink and the heatsink temperature. The diodes are isolated from the heatsink by silicon rubber isolation sheet which has a thermal resistance of $0.75^{O}C$/watt.From the DSEI60–10A data the junction to case resistance is $0.75^{O}C$/watt. The junction temperature will therefore be:

$$T_j = T_h + R_{th(c-s)} \times P_t + R_{th(j-c)} \times P_t \qquad 4.5\text{–}6$$
$$T_j = 80 + 0.75 \times 28.2 + 0.75 \times 28.2 = 122^{O}C$$

The assumption of $T_j = 125^{O}C$ was conservative in this instance. The junction temperature is high but as this is a worst case operating condition it is considered safe.

The diode D_x consists of 6× BY329–1200 medium speed diodes. Medium speed diodes have been used in an effort to reduce the forward recovery voltage as previously discussed. The anodes of D_x are decoupled by C_x to the anodes of the freewheel diodes to provide an initial low inductance path for the reverse recovery current that has been established in L_f.

The components L_f,C_x and R_x form a parallel LCR circuit as indicated in Figure 4.14. The components R_x and C_x are selected such that the reverse current in L_f is reduced to zero within the minimum on time for the IGBT and the overshoot voltage across D_f restricted to the lowest possible amount. At t_1 the reverse recovery current in diode D_f reaches its maximum level (I_{rm}). During the period t_1 to t_2 diode D_f has snapped off and the current in L_f is diverted to C_x and R_x via D_x.

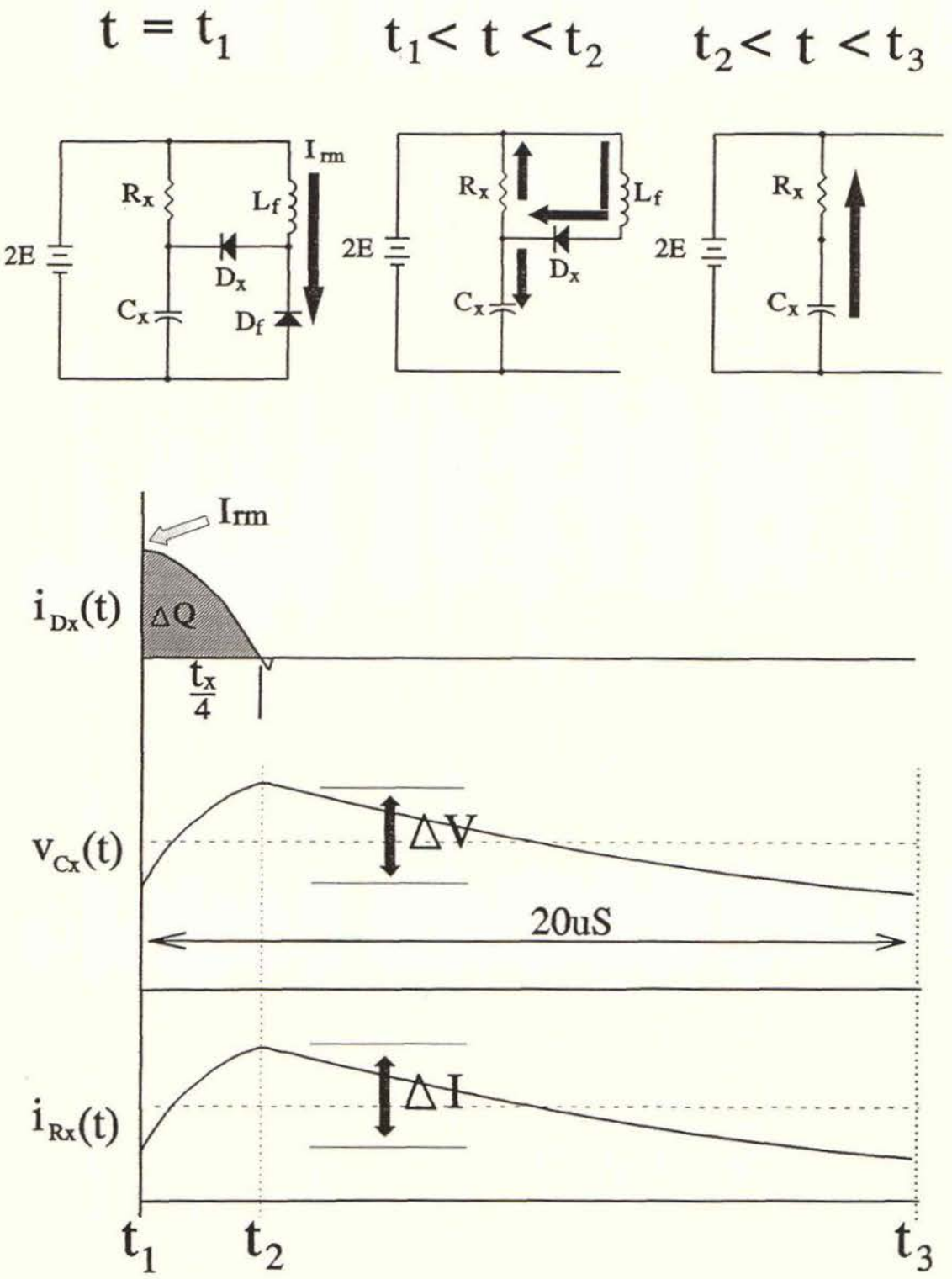


Figure 4.14 Voltage Clamping Action of Cx and Rx

The LCR circuit is made underdamped so that the diode D_x ceases conduction within the minimum IGBT on time which is 2.5μS. If the diode D_x is still conducting when the IGBT turns off its current will be reduced at a high rate due to the quickly rising emitter voltage. This results in an excessive commutating dI/dt for diode D_x. During period t_2 to t_3 capacitor C_x partially discharges through R_x and the supply voltage. It can be shown that the inductor current during period t_1 to t_2 of the transient is given by:

$$I_L = \frac{I(0)}{\sqrt{1 - \zeta_x^2}} \, e^{-at} \sin [\omega t + \phi] \qquad 4.5\text{–}7$$

$$\phi = \tan^{-1}\left[\frac{\sqrt{1 - \zeta_x^2}}{\zeta_x}\right] \qquad 4.5\text{–}8$$

$$a = \zeta_x \omega_x \qquad 4.5\text{–}9$$

$$\omega = \omega_x \sqrt{1 - \zeta_x^2} \qquad 4.5\text{–}10$$

$$\omega_x = \frac{1}{\sqrt{L_f C_x}} \qquad 4.5\text{–}11$$

$$\zeta_x = \frac{1}{2} \frac{Z_x}{R} \qquad 4.5\text{–}12$$

$$Z_x = \sqrt{\frac{L_f}{C_x}} \qquad 4.5\text{–}13$$

If the damping ratio (ζ_x) is small (< 0.05) equation 4–5 approximates to:

$$I_L = I(0) \sin[\omega_x t + \tfrac{\pi}{2}] \qquad 4.5\text{–}14$$

The initial current I(0) is just I_{rm}. The inductor current decays sinusoidally during the period t_1 to t_2 until D_x is reverse biased. The total charge transferred through D_x each cycle is given by:

$$\Delta Q = I_{avg} \frac{t_x}{4} \qquad 4.5\text{–}15$$

Where:

$$I_{avg} = \frac{2}{\pi} I_p = \frac{2}{\pi} I_{rm}$$
$$t_x = \frac{2\pi}{\omega_x}$$

Therefore:

$$\Delta Q = \frac{I_{rm}}{\omega_x} \qquad 4.5\text{–}16$$

Initially some charge flows in R_x and the remainder is stored in C_x. Finally all the charge must flow through R_x. The average current in R_x is therefore:

$$I_{R_x(avg)} = \Delta Q \, f_s = \frac{I_{rm}}{\omega_x} f_s \qquad 4.5\text{–}17$$

The average capacitor voltage will then be:

$$V_{C_x(avg)} = 2E + I_{R_x(avg)} R_x \qquad 4.5\text{–}18$$

The capacitor voltage increment during period t_1 to t_2 can be calculated by recognising that the average charge transfer rate through R_x is $I_{R_x(avg)}$.

Therefore:

$$Q_{R_x(2)} = I_{R_x(avg)} \frac{T}{4} = I_{R_x(avg)} \frac{\pi}{2\omega_n}$$

It follows that the charge stored in C_x must be given by:

$$Q_{C_x(2)} = \Delta Q - Q_{R_x(2)}$$

Therefore the increment in voltage will be:

$$\Delta V = \frac{Q_{C_x(2)}}{C_x} \qquad 4.5\text{–}19$$

It is the maximum voltage generated across C_x which is of interest to us since this appears across the freewheel diodes. $V_{C_x(max)}$ is given by:

$$V_{C_x(max)} = V_{C_x(avg)} + \frac{\Delta V}{2} \qquad 4.5\text{–}20$$

The values selected for C_x and R_x is as follows:

$$C_x = 0.9\mu F$$
$$R_x = 23.5\Omega$$

Therefore:

$$\omega_x = \frac{1}{\sqrt{L_f C_x}} = \frac{1}{\sqrt{2 \times 0.9}} = 0.745 \text{ Mr/s} = 745\times10^3 \text{ r/s}$$

$$t_x = \frac{2\pi}{\omega_x} = 8.4\mu S$$

$$\Delta Q = \frac{I_{rm}}{\omega_x} = \frac{35.22}{745e3} = 47.3\mu C$$

$$I_{R_x(avg)} = \Delta Q\ f_s = 47.3 \times 0.05 = 2.36A$$

$$V_{C_x(avg)} = 2E + I_{R_x(avg)}\ R_x = 672 + 2.36 \times 23.5 = 728V$$

$$Q_{R_x(2)} = I_{R_x(avg)}\ \frac{T}{4} = 2.36 \times \frac{8.4}{4} = 5.0\mu C$$

$$Q_{C_x(2)} = \Delta Q - Q_{R_x(2)} = 47.3 - 5.0 = 42.3\mu C$$

$$\Delta V = \frac{Q_{C_x(2)}}{C_x} = \frac{42.3}{0.9} = 47V$$

$$V_{C_x(avg)} = V_{C_x(avg)} + \frac{\Delta V}{2} = 728 + 23.5 = 752V$$

The conduction time for diode D_x will be given by:

$$t_{D_x} = \frac{T}{4} = 2.1\mu S$$

Which is inside the required $2.5\mu S$ with sufficient margin to allow for component variations. At time t_1 the reverse voltage seen by D_f will be 705V plus the forward recovery voltage across D_x (approximately 50V) giving a total of 755V. The voltage t_2 is approximately the same as this. This is quite acceptable since it is shared across two diodes. However had only single diodes been used for D_f it was felt that there would not be sufficient margin.

The power dissipation in R_x will be:

$$P_{R_x} = \frac{1}{2} L_f I_{rm}^2 f_s$$
$$= 0.5 \times 2 \times (5.78 \times 6)^2 \times 0.05 = 60\text{watts}$$

The resistor R_x was constructed from two parallel 47Ω 50watt metal clad resistors. The losses in diode D_x can be calculated from the following previously derived data. The charge transferred through D_x is (per diode):

$$Q_x = \frac{\Delta Q}{6} = \frac{47.3}{6} = 7.9\mu C$$

$$\text{Average current} = \frac{4Q_x}{T} = \frac{4 \times 7.9}{8.4} = 3.76A$$

BY329–1200 forward voltage drop(max) @4A = 1.3V, [22]

The current wave form is sinusoidal and so the maximum dI/Dt occurs at the zero crossing, using this figure plus taking the forward current as being the average for the period will give a reasonable estimate for the reverse recovery loss:

$$dI/dt = I_{rm}\,\omega_n = 5.87 \times 0.74 \quad 4.4A/\mu S \text{ (per diode)}$$
$$I_f = 3.76A$$

Since the reverse voltage across D_x is clamped by D_f:

$$V_{rm} = V_{C_x(max)} = 752V$$

From the Philips power diode data book, [22], the BY329–1200 diodes switching power loss can be determined from the given nomogram (Figure 8).

For the operating conditions above the switching loss is 3.5watts at a junction temperature of 150^{o}C. The conduction loss will be given by:

$$P_c \approx V_f \, Q_x \, f_s = 1.3 \times 7.9 \times 0.05 = 0.5\text{watts}$$

Then the total loss per diode (P_{D_x}) will be 4watts and the total loss (P_t) in D_x is 24watts under worst case conditions. The six diodes that make up D_x are mounted on a separate aluminum U–section heatsink. If an ambient temperature of 50^{o}C and a worst case heatsink temperature of 100^{o}C is assumed, then the required thermal resistance of the heatsink will be:

$$R_{th(h-a)} = \frac{100 - 50}{24} = 2^{o}\text{C/watt}$$

The diodes are isolated from the heatsink using silicon pads which have a thermal resistance of 1.3^{o}C/watt for the TO220 case device. The diodes junction to case thermal resistance is 3^{o}C/watt. Therefore:

$$T_j = P_{D_x} [R_{th(j-c)} + R_{th(c-h)}] + P_t \, R_{th(h-a)} + T_a$$

$$T_j = 4 \times (3 + 1.3) + 24 \times 2 + 50 = 115^{o}\text{C}$$

This is quite acceptable for a worst case condition.

4.6 IGBT Module Design

This module consists of the IGBT and its associated gate driver. First the gate drive system will be discussed. In Appendix D there is a full schematic of the gate drive circuit. Only a brief discussion of the operational features will be given here, rather than a detailed circuit analysis. Shown in Figure 4.15 is a block diagram of the gate driver.

The basic requirement of the driver is to be able to supply pulsed currents to charge and discharge the IGBT gate capacitance to $\pm$15V. Because the IGBT's used are quite large the effective input capacitance is also considerable, in the order of 50,000pF. Accordingly the drive requirements are also considerable. A gate charge of 0.75μC must be supplied to bring the IGBT into full conduction. To obtain the rise time that the devices are capable, the 0.75μC must be supplied within 150nS at a rate of 5A. This represents 50mA of dc current from the power supply for a 50kHz switch freqency. A similar current would be associated with turning the IGBT off.

The gate driver is isolated from ground and is at the emitter potential and therefore swings at rates up to 2000V/μS relative to ground as the IGBT switches. As well as this the gate driver is located in close proximity to the power circuit where EMI would be high. These factors dictated the use of special techniques to yield a reliable design. Previous experience in other projects had taught that standard integrated circuit devices can display erratic operation in these conditions. Presumably because the currents often used in these circuits are in the microamp range, the extreme dV/dt's that are present in high power converters can induce currents that modify the circuit operation. For example at 2000V/μS, 2mA would flow in a capacitance of only 1pF. It was therefore decided from the outset to the design the gate driver using completely discrete circuitry with current levels in the region of tens of milliamps where possible.

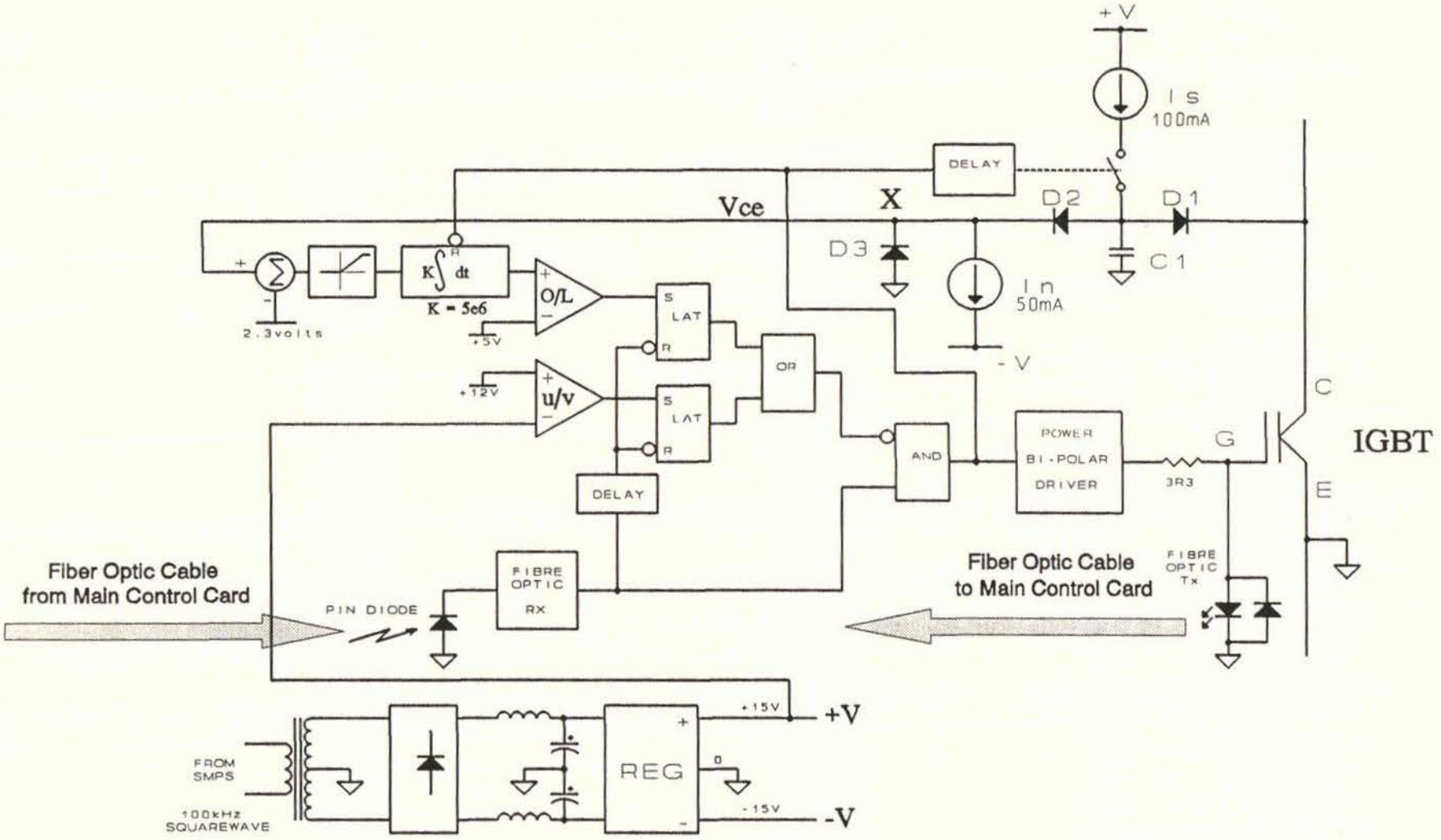


Figure 4.15 Gate Driver Block Diagram

The drive signal is delivered to the driver via a fiber optic cable which avoids any coupling back into the main control circuits. The main controller can be located quite remotely from the converters and suitably screened so there is no possibility of induced signals and therefore erratic and perhaps dangerous operation. Power is supplied to the driver from an SMPS at 100kHz squarewave. This is transformer coupled, rectified and filtered before being passed through a discrete $\pm$ 15V current limited regulator. Because of the relatively high current levels used in the circuit plus the reasonably high drive requirements the positive regulator has to be capable of 500 mA. Current limiting is set at 800mA.

The output stage is bipolar supplying $\pm$ 15V via a 3Ω resistance to the gate. The "ON" status of the IGBT gate is fed back to the main controller via a second fiber optic cable. This is used by the controller to verify the integrity of the driver and IGBT.

An important feature of the driver is the collector emitter voltage sensing system. This system ensures in the event of a complete control system failure that the IGBT cannot be destroyed. In fact this driver a current controller in its own right. The collector emitter voltage (V_{ce}), is sensed in the on state via a diode D_1 as indicated in Figure 4.16. This diode has the function of blocking the high V_{ce} when the IGBT is off. The capacitor C_1 decouples the reverse recovery current in D_1. The diode D_2 is used to match the voltage drop of diode D_1 so that the voltage at point **X** is V_{ce}. Thermally induced forward voltage drop variations are canceled using this method. A current source I_s supplies 100mA to both diodes. The current through D_2 is regulated at 50mA by Current source I_n so that the current through D_1 is also always forced to be 50mA regardless of the level of V_{ce}. Since the diode currents are always identical this further increases the accuracy that the voltage at point **X** reproduces V_{ce}.

The current source I_s and hence the V_{ce} sensing system becomes active after a short delay after the IGBT turns on. This allows time for the V_{ce} to fall to normal conduction levels before it is sensed, otherwise false tripping would occur. The V_{ce} is subtracted from a 2.3V reference and fed to an integrator. The output from the integrator is compared with another reference which determines the volt–time product tripping level. If the volt time product exceeds this level a latch is tripped which inhibits the drive signal and the IGBT is switched off. The off status is transmitted to the main control board via a fiber optic cable and the drive command is removed for the remainder of the cycle. Regardless of the operation of the controller the latch is set for the remainder of the cycle and can only be reset by absence of the drive command for a finite period. Under normal operating conditions the volt–time product is not exceeded and no tripping occurs. In this case once the drive command goes low in the normal manner the integrator is reset ready for the next cycle.

The reason for subtracting the V_{ce} from 2.3V is to make the circuit more sensitive to actual overloads. Because the voltage increases only by approximately 0.5V for a increase in collector current of around 100A the sensitivity of the sensing circuit is quite important. If the IGBT in its on condition is looked upon as a crude current shunt then the V_{ce} tripping circuit operates similarly to a charge controller. That is the total charge that is allowed to pass each cycle is limited to a preset value. This means the device power dissipation can be limited to a safe level. The main controller uses output current control plus there is independent hysteresis current limiters on each buck converter. The V_{ce} sensing is a backup to these and is hence co–ordinated to operate at a higher device current, it should only become active if there is a malfunction in the controller, gate driver or the IGBT itself.

The gate driver +15V supply rail is also monitored and the IGBT is inhibited if it is below 12V. This ensures that any malfunction of the driver or SMPS which causes low supply voltage can in no way damage the IGBT. Again the drive is latched off for the remainder of the cycle. Repeated inhibiting of the drive will cause the main controller to shut down the converter. The philosophy here is that critical monitoring and protection should be implemented as part of the the switching device itself. This thinking is also being applied to the numerous "SMART" power devices which are now becoming commercially available, [42].

Great effort has been taken to optimise the speed of each stage to minimise the delay time between logic high in the controller to the commencement of current flow to the gate. This optimisation process was done using a SPICE, [16], computer model of the basic fiber optic amplifier and bipolar power driver. Details of this model are presented in Appendix E. It was possible to reduce the delay time to less than 400nS using various speed up networks and Schottky diode base collector clamps to the limit transistor saturation levels.

The IGBT worst case operating condition will now be examined. This occurs at maximum bus voltage, full load current and maximum duty ratio ($T_{on} = 17.5\mu S$). A factor that complicates the calculation is that during the first $2\mu S$ the collector current is substantially above the load current due to the resonant reversal of the snubber capacitor and the reverse recovery of the freewheel diodes. This is further complicated by the fact that during the first $0.4\mu S$ the device exhibits a high foward drop due to the absence of full conductivity modulation, as explained in chapter three.

Figure 4.16 shows the estimated collector current and collector emitter voltage for the first $2\mu S$.

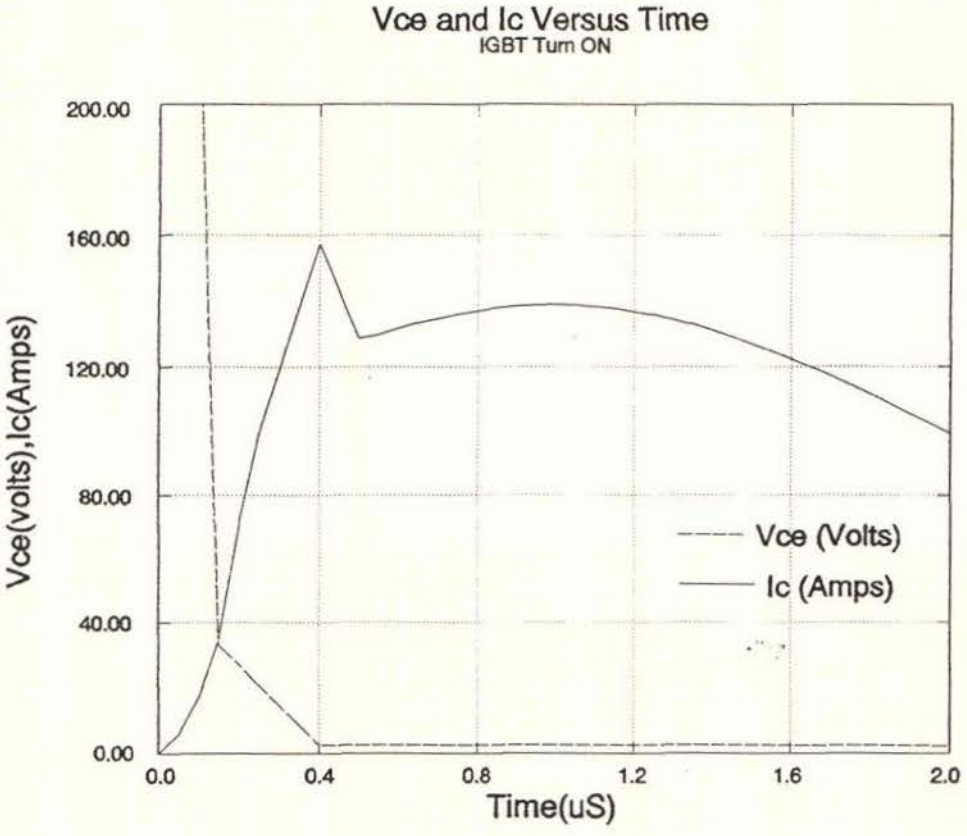


Figure 4.16 Predicted IGBT Voltage and Current During Turn On

The first 0.15μS period is based on equation 3.7–3 and takes account of the fact that the voltage across L_f linearly increases over this period.The waveforms were generated using a spreadsheet as shown in Table 4–1 with the following relationships:

$$0 < t < 0.15 \quad I_c = \frac{E}{L_f t_r} t^2 + 39\mathrm{Sin}(\omega_r t),\ V_{ce} = -4480\ t + 672$$

$$0.15 < t < 0.4 \quad I_c = \frac{2E}{L_f} t + 39\ \mathrm{Sin}(\omega_r t),\ V_{ce} = -109t + 46$$

$$0.4 < t < 0.5 \quad I_c = \frac{-2E}{L_f} t + 0.8\ \frac{2E}{L_f} + 39\mathrm{Sin}(\omega_r t),\ V_{ce} = 1.8 + 5\times10^{-3} I_c$$

$$0.5 < t < 2.0 \quad I_c = 100 + 39\mathrm{Sin}(\omega_r t),\ V_{ce} = 1.8 + 5\times10^{-3} I_c$$

The steady state collector emitter voltage at $T_c = 80^{O}C$ was shown to be $1.8 + 5 \times 10^{-3} I_c$ in Chapter Three. The actual spreadsheet data is displayed in Table 4.1. The loss associated with each segment can be determined as follows:

$$E_i = P\ dt = P_i\ (t_i - t_{i-1})$$

$$P_t = f_s \sum_{i=1}^{n} P_i$$

This has been done for E = 336 V with the total loss associated with the first 2μS of the conduction period being 48.7watts. For the remaining 15.5μS for the collector current will be equal to the load currentof 100A. The associated power dissipation from chapter three will be given by:

$$P_2 = \frac{15.5}{20} \times [1.8\ I_L + 5\times10^{-3} I_L^{\,2}]$$

$$= \frac{15.5}{20} \times [\ 1.8\times100 + 5\times10^{-3}\times\ 100^2]$$

$$= 178.3 \text{ watts @ } T_c = 80^{O}C$$

t(uS)	Ic(amps)	Vce(volts)	Pi(w)	Ei(uJ)
0.00	0.00	672.00	0.00	0.00
0.05	5.88	448.00	2633.25	131.66
0.10	17.34	224.00	3883.35	194.17
0.15	34.36	33.00	1133.77	56.69
0.20	72.12	27.00	1947.24	97.36
0.25	99.01	21.00	2079.16	103.96
0.30	118.60	15.00	1779.02	88.95
0.35	138.08	9.00	1242.76	62.14
0.40	157.44	2.59	407.33	20.37
0.45	143.25	2.52	360.46	18.02
0.50	128.70	2.44	314.49	15.72
0.55	129.78	2.45	317.83	15.89
0.60	131.68	2.46	323.72	16.19
0.65	133.37	2.47	329.02	16.45
0.70	134.86	2.47	333.69	16.68
0.75	136.13	2.48	337.70	16.89
0.80	137.18	2.49	341.01	17.05
0.85	137.99	2.49	343.60	17.18
0.90	138.57	2.49	345.43	17.27
0.95	138.91	2.49	346.50	17.33
1.00	139.00	2.49	346.80	17.34
1.05	138.85	2.49	346.32	17.32
1.10	138.46	2.49	345.07	17.25
1.15	137.82	2.49	343.06	17.15
1.20	136.96	2.48	340.31	17.02
1.25	135.86	2.48	336.83	16.84
1.30	134.53	2.47	332.66	16.63
1.35	133.00	2.46	327.84	16.39
1.40	131.25	2.46	322.39	16.12
1.45	129.32	2.45	316.38	15.82
1.50	127.19	2.44	309.84	15.49
1.60	122.46	2.41	295.40	29.54
1.70	117.16	2.39	279.52	27.95
1.80	111.44	2.36	262.67	26.27
1.90	105.43	2.33	245.34	24.53
2.00	99.28	2.30	227.99	22.80
			E = Sum	974.62 uJ
			Pt =fs.E	48.73 watts

Table 4. IGBT Turn On Power Dissipation Spreadsheet

The remaining loss is that associated with switch off and can be found from the previously derived equations 3.7–8 and 3.7–9:

$$P_{s3} + P_{s4} = \frac{f_s \, I_L{}^2 t_f{}^2}{24 \, C_s} + \psi_d \, I_L \, f_s$$

$$P_{s3} + P_{s4} = \frac{0.05 \times 100^2 \times 0.2^2}{24 \times 0.05} + 3 \times 100 \times 0.05$$

$$= 31.7 \text{ watts}$$

The total IGBT loss at maximum bus volts and full load current with maximum duty ratio is therefore:

$$P_t = P_{s1} + P_{s2} + P_{s3} + P_{s4}$$

$$= 48.7 + 178.3 + 31.7 = 259.0 \text{ watts}$$

The junction to case thermal resistance is $0.104^{o}C$/watt and the IGBT is mounted directly on the main heatsink.Therefore the worst case junction temperature will be:

$$T_j = P_t \times R_{th} + T_h$$
$$= 259.0 \times 0.104 + 80 = 107^{o}C$$

This is a quite satisfactory result. The turn on and turn off losses are also quite satisfactory since reducing them further by increasing L_f and/or C_s would really only make a marginal improvement in the overall IGBT loss

4.7 Determination of the Cooling Requirement

In order calculate the cooling requirements the total power dissipation will be calculated at full load and maximum bus voltage with 50% duty ratio. The major power dissipating devices mounted on the heatsink are as follows:

(a) IGBT

(b) Freewheel diodes (D_f)

(c) Freewheel diodes current balancing resistors (R_f)

(d) Freewheel diode clamping resistor (R_x)

(e) Snubber diodes (D_s)

(f) Snubber resonant reversing diode (D_r)

(g) Clamp diodes (D_c)

(h) SOI

Each of these will be dealt with in turn.

IGBT

The power loss for 87.5% duty ratio is calculated in section 4.6. The loss in the first 2μS after turn on and the turn off loss will be the same for the 50% case. However the

conduction time is now 8μS. The loss associated with this at 100A will be:

$$P_2 = (1.8\, I_L + 5\times10^{-3} I_L^2) \times \frac{8}{T}$$

$$= (1.8 \times 100 + 5\times10^{-3} \times 100^2) \times \frac{8}{20}$$

$$= 92\text{watts} \ @T_c = 80^{O}C$$

The total IGBT loss will therefore be:

$$P_t = P_1 + P_2 + P_3$$
$$= 48.7 + 92 + 31.7 = 173.3\text{watts}$$

Freewheel Diode

Again the switching loss will be the same as calculated in Section 4.5. which was 5.17watts per diode. The average and rms currents for 50% duty ratio will be given by:

$$I_{avg} = \frac{1-D}{D} I_L = \frac{1-0.5}{6} \times 100 = 8.3A$$

$$I_{rms} = \frac{\sqrt{1 - D}}{6} \times 100 = 11.8A$$

The loss will be given by:

$$P_c = 1.48 I_{avg} + 6 \times 10^{-3} I_{rms}^2$$
$$= 1.48 \times 8.3 + 6 \times 10^{-3} \times 11.8^2$$
$$= 13.12\text{watts}$$

The total loss per diode then is:

$$P \text{ (per diode)} = 13.12 + 5.17 = 18.3\text{watts}$$
$$P_t = 12 \times 18.3 = 219\text{watts}$$

Current Balancing Resistor (R_f)

The rms current carried by each resistor from the previous calculation is 11.8A. therefore the power dissipation will be:

$$P = I_{rms}^2 R_f = 11.8^2 \times 0.1 = 13.9 \text{ watts}$$

Therefore the total loss will be:

$$P_t = 6 \times 13.9 = 83.4 \text{ watts}$$

Freewheel Diode Clamping Resistor (R_x)

The power dissipated in this resistor is not effected by the duty ratio so the losses will be as calculated in section 4.5:

$$P_t = 60 \text{ watts}$$

Snubber Diodes (D_s)

This diode under normal conditions does not have any significant switching loss. The conduction losses have been calculated in section 4.3 and is 4.3 watts/diode. Since there is two diodes the total loss is 8.6 watts.

Clamp Diode (D_c)

The diode D_c which is composed of two parallel paths at full load carries the following average rms currents:

$$I_{avg} = \frac{1}{2} \times \frac{I_L}{2}$$

$$I_{rms} = \frac{1}{2} \times \frac{I_L}{\sqrt{3}}$$

For a time duration approximated by:

$$t_c = \frac{I_L \; L_f}{V_c} = \frac{100 \times 2}{156} = 1.28\mu S$$

The conduction loss will therefore be given by:

$$P_c = (I_{avg} V_{to} + I_{rms}^2 R_f) \frac{t_c}{T}$$

$$P_c = (\frac{I_L}{2} V_{to} + \frac{I_L^2}{12} R_f) \frac{t_c}{T}$$

$$= (\frac{100}{4} \times 1.48 + \frac{100^2}{12} \times 6 \times 10^{-3}) \times \frac{1.28}{20} = 2.7 \text{watts}$$

In normal operation this diode also exhibits switching loss. The dI/dt per diode being determined by the clamp voltage and L_f:

$$\frac{dI}{dt} = m = \frac{1}{2} \frac{V_c}{L_f} = \frac{156}{4} = 39A/\mu S$$

The forward current in each diode decays at $39A/\mu S$ from an initial value of 50A to zero over $1.28\mu S$. Prior to this however the diode was carrying no current. The effective forward current prior to commutation is therefore estimated to be half the initial current. It is thought that this will yield a realistic answer for the maximum reverse recovery current:

$$I_f \approx \frac{I_L}{4} = \frac{100}{4} = 25A$$

In Appendix F I_{rm} is found to be 3.9A. Assuming $Q_1 = Q_2$ and the the maximum reverse voltage of $V_c = 156V$ is reached instantaneously at snap off:

$$P_s = f_s V_c \frac{I_{rm}^2}{2\,m}$$
$$= 0.05 \times 156 \times \frac{3.9^2}{2 \times 39}$$
$$= 1.5 \text{ watt/diode}$$

The total loss would be:

$$P_t = (1.5 + 2.7) \times 4$$
$$= 16.9 \text{watts for 4 diodes}$$

SOI

The SOI efficiency at 500 watts which corresponds to operation at 100A is 90%. Therefore the loss must be given by:

$$P_{loss} = 0.1 \times 500 = 50 \text{ watts}$$

The heatsink requirements will now be calculated. The total heatsink load will be the sum of the above losses:

IGBT – 173 watts

D_f – 219 watts

R_f – 83 watts

Rx – 60 watts

D_s – 9 watts

D_c – 17 watts

SOI – 50 watts

Total– 611 watts

Adding 10% to allow for the miscellaneous heat sources such as diode snubbers gives a total heatsink load of 672 watts. To maintain a temperature of 80^{o}C in 50^{o}C ambient the heatsink thermal resistance will be given by:

$$R_{th(h-a)} = \frac{T_h - T_a}{P_t}$$

$$= \frac{80 - 50}{672} = 0.045^{o}\text{C/watt}$$

The heatsink chosen has a thermal resistance of 0.15^{o}C/watt with natural convection cooling. Forced air cooling is used to reduce this down to 0.045^{o}C/watt. The required air velocity is found by using the curve supplied in [43]. To obtain the required thermal resistance the air velocity would need to be 6m/s. The surface area through which the air flows is estimated to be 0.009 m^2. The volumetric air flow will therefore be given by:

$$Q_{air} = 0.009 \times 6 = 0.054\ m^3/s = 54\ l/s\ (120\ cfm)$$

Based on this calculation three 43 cfm fans were installed to provide the necessary cooling.

4.8 Buck Converter Experimental Results

A full scale buck converter was constructed to test the power circuit performance and determine any modifications that may be necessary. The only major change required to the original design was to the freewheel diode module. Because of the extra peak reverse voltage due to the unexpected high forward recovery in diode D_x the freewheel diode had to be constructed from two series diodes. This has already been discussed in Chapter Three. The disadvantage of the use of two series diodes is the additional power loss.

In Section 4.7 the power loss was calculated for 100A output at 50% duty ratio and the nominal bus voltage. Based on assumptions presented in previous sections the power loss was calculated to be 672 watts. Verification of this is particularly difficult since it represents only a small percentage of the output power. The only available power meters had a maximum current capability of 25A. At this level the accuracy is 0.1%. In order to extend the current capability two external shunts were paralleled with the existing units. It is expected that combined unit had an accuracy of 0.5%. Although this was considered to be adequate for accessing the basic functioning of the converter it is not good enough to verify the predicted power loss. The following calculation illustrates the problem.

For a bus voltage of 560V, Load current of 100 A and 50% duty ratio the absolute power loss error can be calculated. Assuming a 0.5% error in the input and the output power measurement and a nominal power loss of 672 watts:

$$\Delta P_{in} = 0.005 \times 28672 = 143 \text{ watts}$$

$$\Delta P_{out} = 0.005 \times 28000 = 140 \text{ watts}$$

Since the power loss is given by:

$$P_{loss} = P_{in} - P_{out}$$

The error in P_{loss} will be:

$$\Delta P_{loss} = \sqrt{\Delta P_{in}^2 + \Delta P_{out}^2}$$

$$\Delta P_{loss} = \sqrt{143^2 + 140^2} = 200 \text{ watts}$$

An actual loss of 672 watts could be measured as low as 472 watts or as high as 872 watts. The conclusion is that this metering system is not accurate enough to verify the predicted loss. In addition to this because of the limited loading banks available the converter could not be loaded beyond 21 kW. The converter was tested at an output current of 75A at 50% duty ratio (21 kW for a bus voltage of 560V) with the following results:

$$P_{in} = 21733 \pm 109 \text{ watts}$$

$$P_{out} = 21043 \pm 105 \text{ watts}$$

$$P_{loss} = 690 \pm 151 \text{ watts}$$

The measured heatsink temperature with 120 cfm of forced air cooling was 55^0C in 30^0C ambient temperature. From Section 4.7 the effective thermal resistance of the heatsink is 0.045^0C/watt. This would imply that the power loss is:

$$P_{loss} = \frac{T_{rise}}{R_{th}} = \frac{25}{0.045} = 556 \text{ watts}$$

This indicates that the actual loss is well on the low side of the error range. The power loss is dominated by "proportional to load current" components and therefore at a load of 100A with other conditions remaining the same, the expected loss would be 741 watts, based on the temperature rise measurements above. The heatsink temperature at 50^0C ambient would be 83^0C. Since the design in all respects is conservative this result is acceptable. The case temperatures of all the major semiconductors was also measured and found to be acceptable for the load of 75A.

The converter waveforms were recorded using a Tektronix 2232 storage oscilloscope linked to a plotter. Only voltage waveforms could be obtained. The reason is that to obtain this measurement current shunts or CT's have to be inserted, the output voltage from these are very low and the high EMI environment causes excessive disturbance of the measurement.

Figure 4.17 shows the IGBT collector emitter voltage for a load current of 40A at a bus voltage of 566 V. Attention is drawn to the following points:

Turn–off dV/dt of approx. 750 V/μS (A to C)
Peak overshoot of 150V (at C)
Voltage fall time of 200nS (at D)
Turn–on tail, 35V to 0 over 0.3μS(at E)

The same waveform (except inverted) for a load of 75A and a bus voltage of 585V is presented in Figure 4.18. Notice the increase in turn–off dV/dt to 1500V/μS. The Freewheel diode anode cathode voltage waveform (two series diodes) for a load current of 60A and a bus voltage of 560V is shown in Figure 4.19. Attention is drawn to the peak reverse voltage of 634V. This would not be expected to rise to 750V at full load and maximum bus voltage.

Figure 4.20 shows the anode cathode voltage (single diode) of diode D_s and the IGBT collector emitter voltage for a load current of 40A at a bus voltage of 510 V. The following aspects are of interest:

Forward recovery, 94V/diode (at A)
Peak reverse voltage of 300V/diode (at B)
Resonant reversing period (at C)

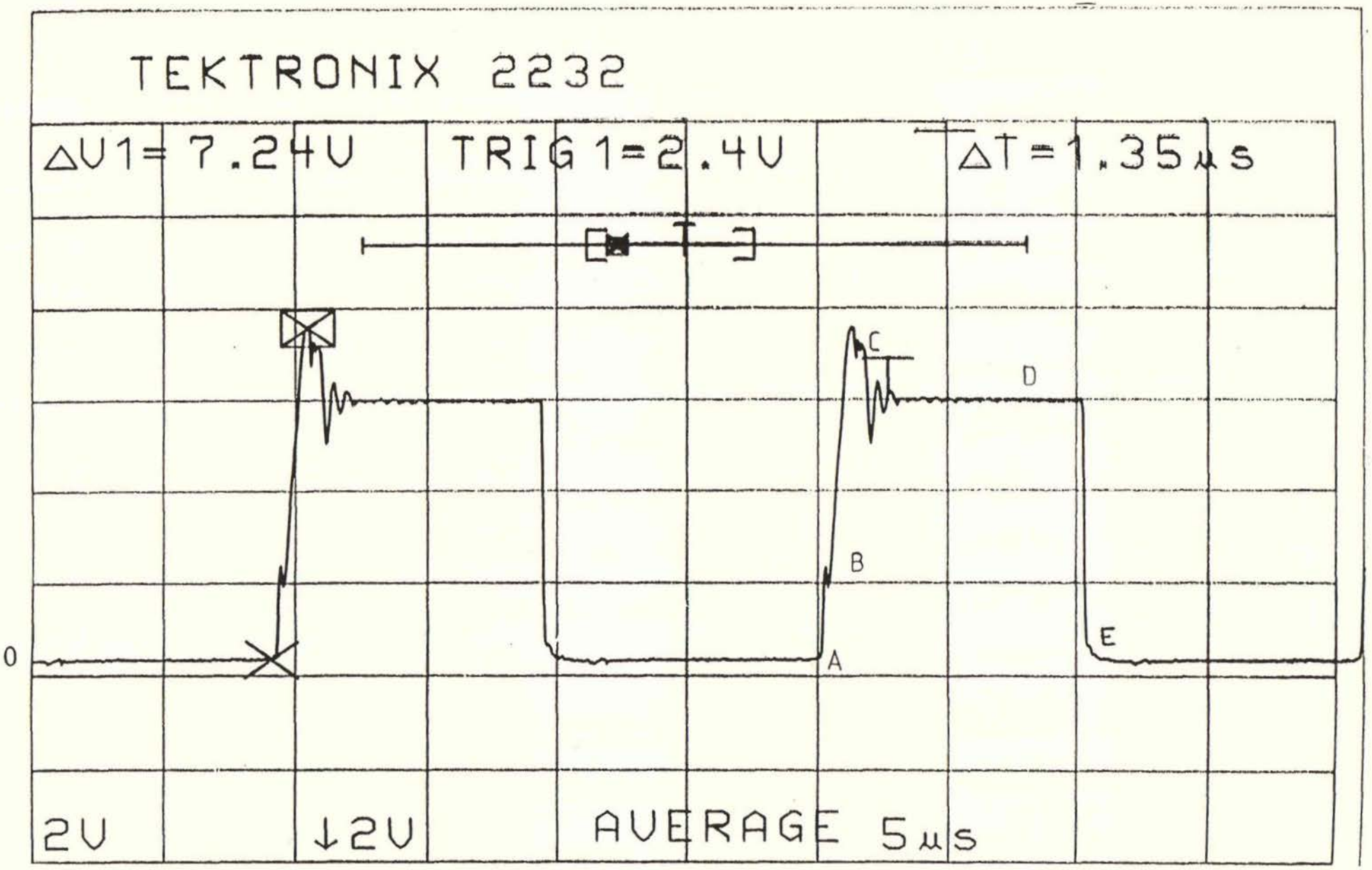


Figure 4.17 Actual IGBT Collector Emitter Voltage (200V/div)

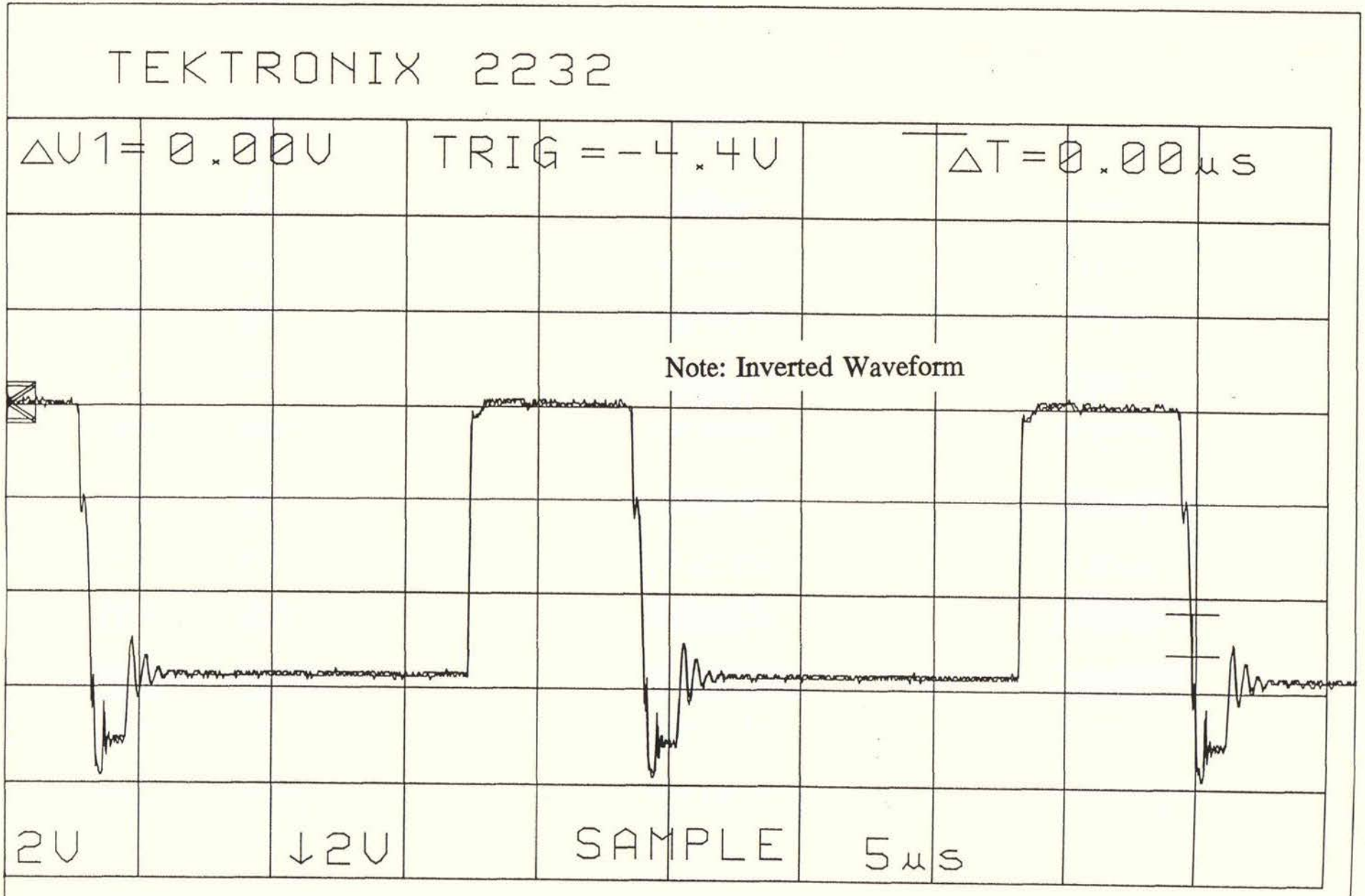


Figure 4.18 IGBT Collector Emitter Voltage (200V/div)

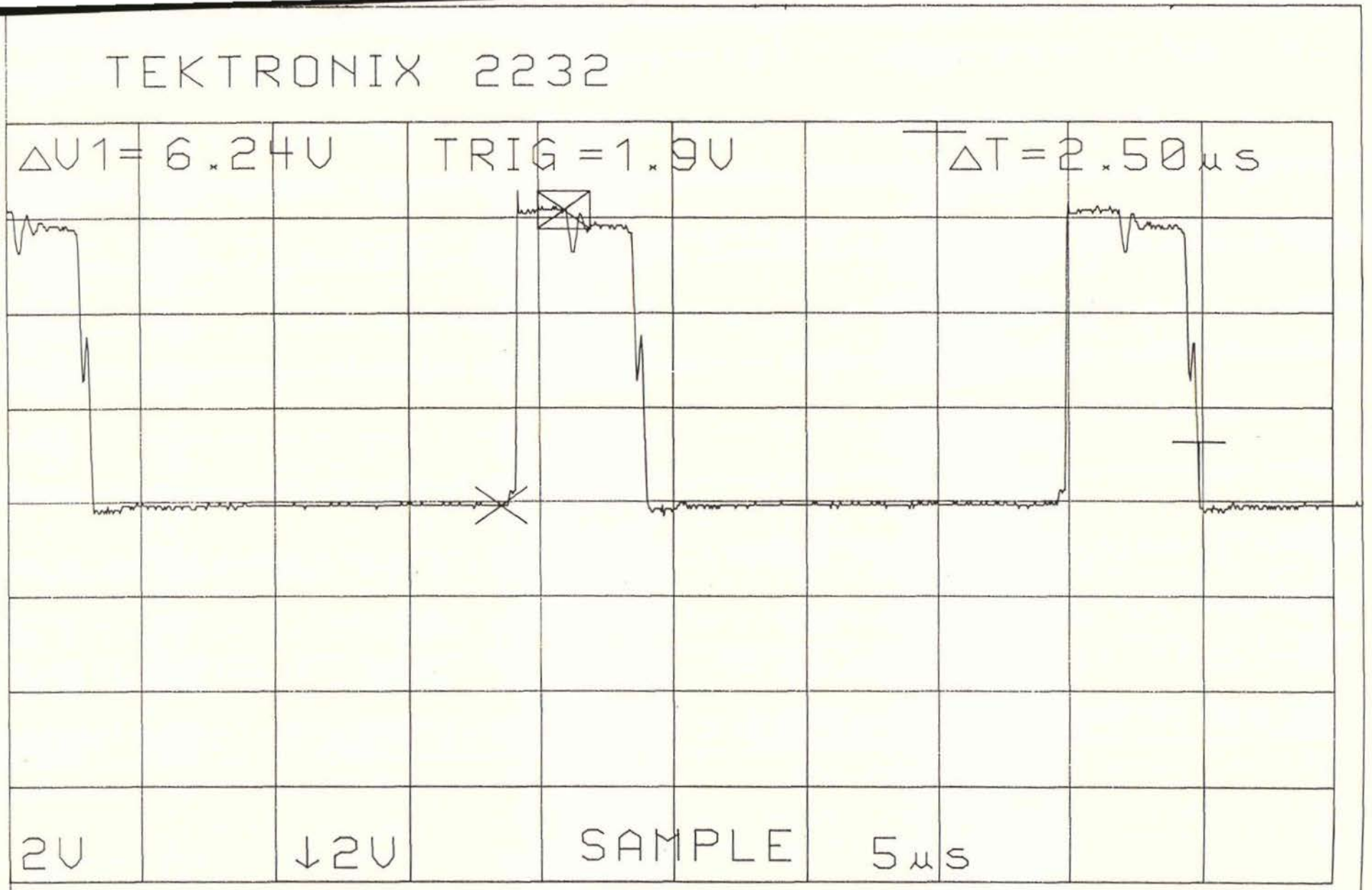


Figure 4.19 Freewheel Diode Anode Cathode Voltage (200V/div)

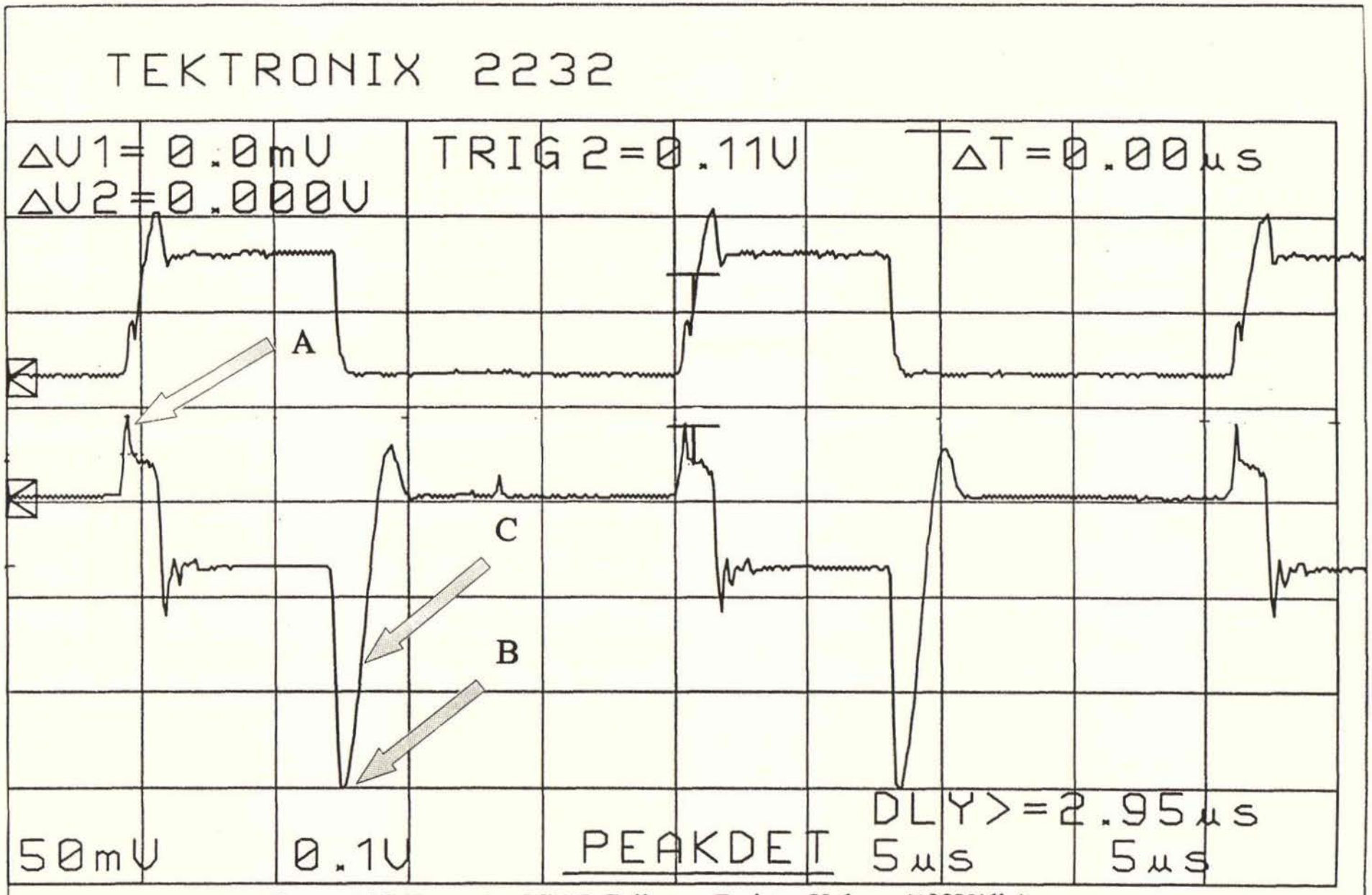


Figure 4.20 Trace 1 - IGBT Collector Emitter Volage (400V/div)

Trace 2 - Diode Ds Anode Cathode Voltage (100V/div)

5. CONTROLLER OPERATION AND DESIGN

The new converter topology outlined in Chapter Two requires a specialized control system to complete the amplifier. This chapter is devoted to the operation and design of this control system. The first section gives an overview of the control strategies employed. The major topics include the output and the leg bias control loops and the four phase modulation technique with frequency dropping to extend the dynamic range. The basic hardware implementation philosophy is also briefly discussed in the first section.

In subsequent sections the detailed operation of each section of the controller is discussed. These include:

(a) Phase/Ramp Generator

(b) Bias Current Control

(c) Output Current Control Including Frequency Dropping

(d) Current Limiter

Following this, a detailed control systems analysis is presented. Of particular importance is the development of expressions describing the interaction between the output current and the bias current control loops.

5.1 Control Strategy

A simplified block diagram of the controller is presented in Figure 5.1. As outlined in Chapter Two there are two primary control loops required for this converter. The first controls the load current by adjustment of the average output voltage via the five level pulse width modulation technique.

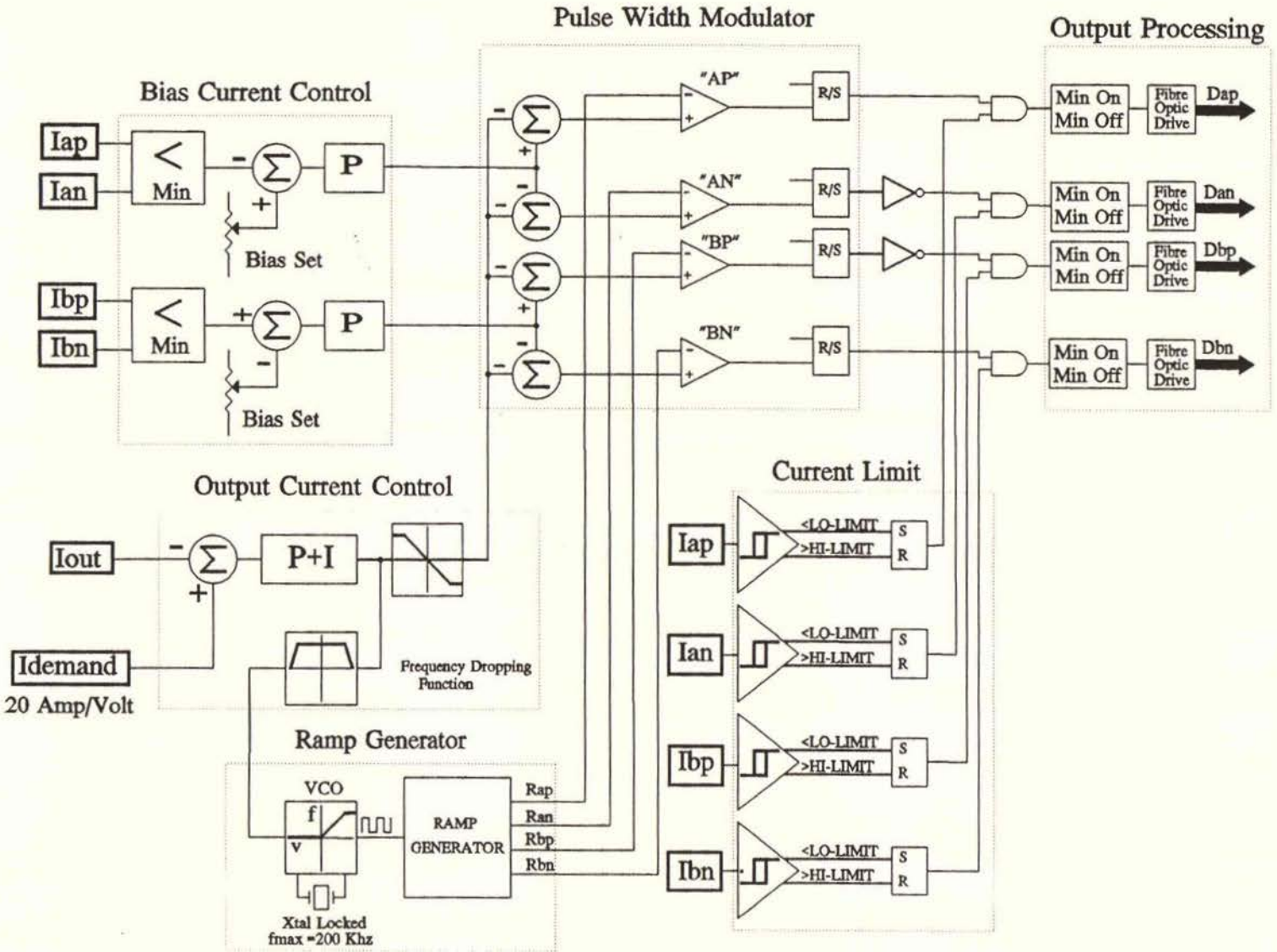


Figure 5.1 Amplifier Controller Simplified Block Diagram

The second controls the bias current which flows down each phase leg in order to keep the idle buck converter in conduction. All buck converters must remain in conduction in order for the five level modulation to be achieved. A simplified schematic of the modified bridge inverter is repeated in Figure 5.2.

Assuming that the "AP" converter is supplying the output current I_o, the coupling transformer magnetizing current I_{ma} must be maintained above $I_o/2$ for the "AN" converter to maintain conduction. The "AN" chopper is said to be in its idle state. The current being carried by the "AN" chopper during this period is termed the bias current and at any time will be the minimum of the out of the two converter currents. The function of the bias current control loop is to maintain the magnetizing current above $I_o/2$. The magnetizing current can be manipulated by adjustment of the differential volt seconds across the transformer. Forcing an average differential voltage between V_{ap} and V_{an} will cause the magnetizing current to increase or decrease depending on the polarity. The magnetizing current can therefore be controlled.

The bias current is the difference between it and $I_o/2$. In control systems terminology this means that the bias current control loop is "disturbed" by the output current. As discussed in Chapter Two at high rates of change of output current a large differential voltage must be applied to keep the bias current constant. If excessive, this gives rise to high levels of 50 kHz spectral content in the output voltage, which is undesirable. In the ideal five level system the 50 kHz component is completely absent as is seen in Figure 2.10. In the practical implementation of this topology a 50 kHz component must be accepted.However this can be kept to a low level by limiting the bandwidth of the bias current control loop. At higher frequencies the bias current is allowed, to a limited extent, to be disturbed by the output current to avoid excessive differential voltages from being generated. The bias current is raised to avoid discontinuous operation.

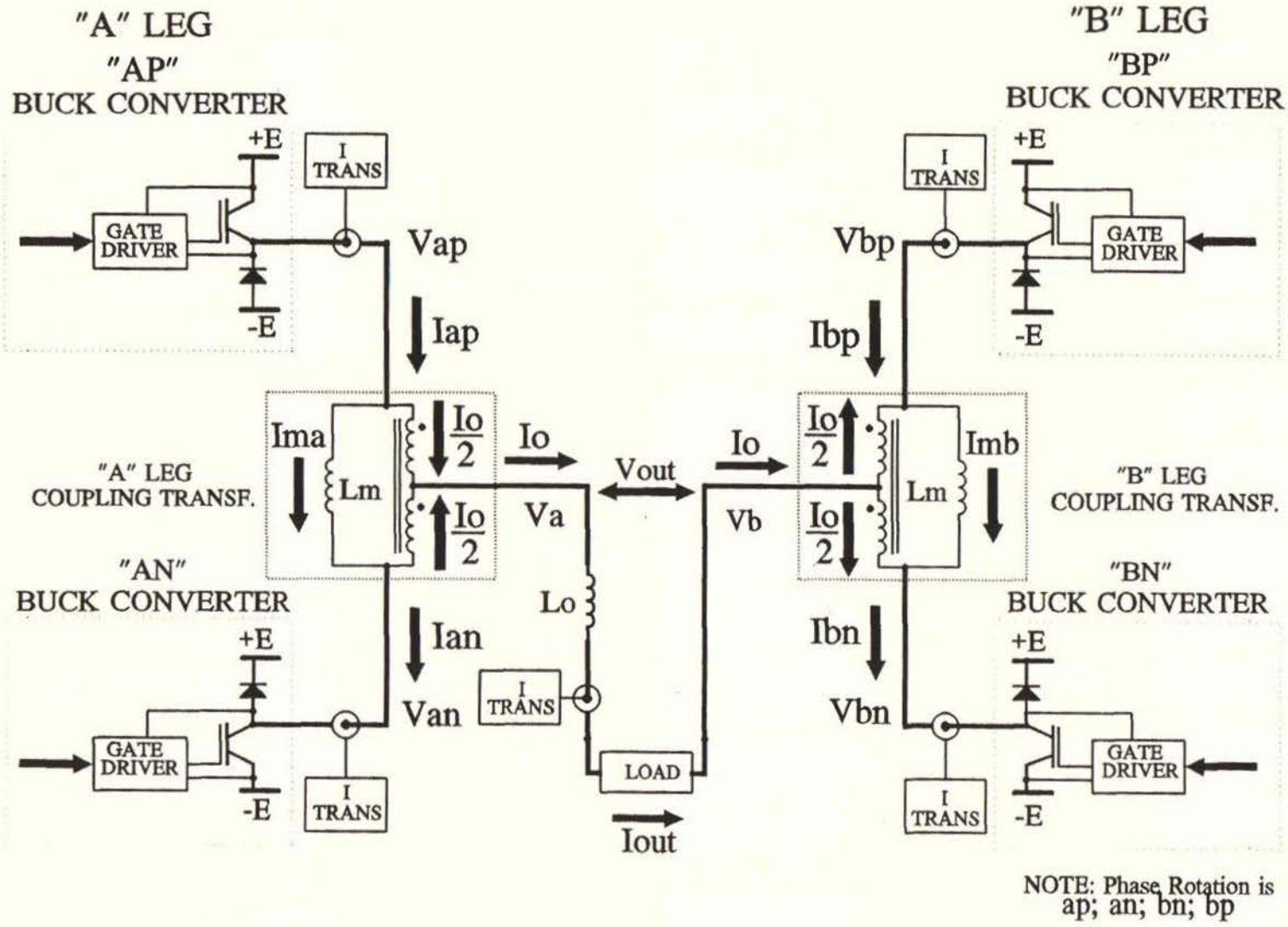


Figure 5.2 Amplifier Bridge Inverter

In Chapter Four it was shown that because of constraints imposed by the snubbing system a minimum off and on time was required to be enforced. This causes the difficulty of not being able to obtain the full potential output voltage swing. The average output voltage for the bridge inverter is given by the following:

$$V_{ab}(avg) = 2E\ (2D-1) \qquad 5.1\text{–}1$$

The minimum on time is 2.5μS which in a 20μS period gives a duty ratio of 0.125. From equation 5.1–1 this results in a minimum output voltage of (@ E = 280V) –420V. Likewise the maximum output voltage is +420V. This represents an unacceptable restriction on the amplifier's performance. It is overcome by reducing the switching frequency, while maintaining a constant on or off time. In this way the modulator duty cycle is extended to 0.01 to 0.99. This strategy yields a constant modulator gain over nearly the full duty cycle range.

The frequency dropping function is implemented by a VCO from which all the modulator ramp signals are derived. This will be discussed in further in Section 5.2. The minimum off and on times are enforced just before the drive signals are dispatched to the drive modules so that there is no possibility of violation. The minimum times are generated digitally by counters. These are clocked by a 6 MHz crystal locked signal to ensure their accuracy. The output current controller is a simple proportional plus integral system. This drives a pulse width modulator and VCO via function generators such that frequency dropping commences once the control voltage reaches a level which corresponds to the production of minimum on or off times. The upper VCO frequency is crystal locked to ensure stable operation of the ramp generators.

The amplifier output current is controlled and the input demand is limited.

This means under normal operating conditions an overload condition is not possible. However additional current limiting has been incorporated which will only become operational in abnormal conditions such as a control system or power circuit failure. The current limiting is achieved by independent synchronized hysteresis control on each buck converter. The limit level is set above the normal maximum operating current but still at a safe value.

The control strategy discussed above requires the independent measurement of each buck converters current in addition to the output current. Figure 5.2 shows the circuit location of the five current transducers. The transducers use a hall effect device plus a high gain amplifier followed by a buffer/driver. The bandwidth of the transducer unit is 100 kHz.

The entire controller is constructed on a single printed circuit board with the analog circuitry being implemented using wide bandwidth LF353 operational amplifiers and LM319 high speed comparators. The digital logic is entirely implemented using Philips PAL technology. This has the advantage of greatly reducing the integrated circuit count. Perhaps more importantly PALs give the ability to implement functional blocks in a single package allowing easier circuit development. For example the minimum ON/OFF generator is implemented in a single PAL. This circuit can then be developed and tested independently of the remainder of the controller.

An overview of the controller function blocks showing details of the interconnections is shown in Figure 5.3. Each major signal has been labeled with an abbreviated name which is descriptive of its function. For example, the signal "APpwm" is the "AP" converters PWM signal. Reference will be made to these signals in the sections following.

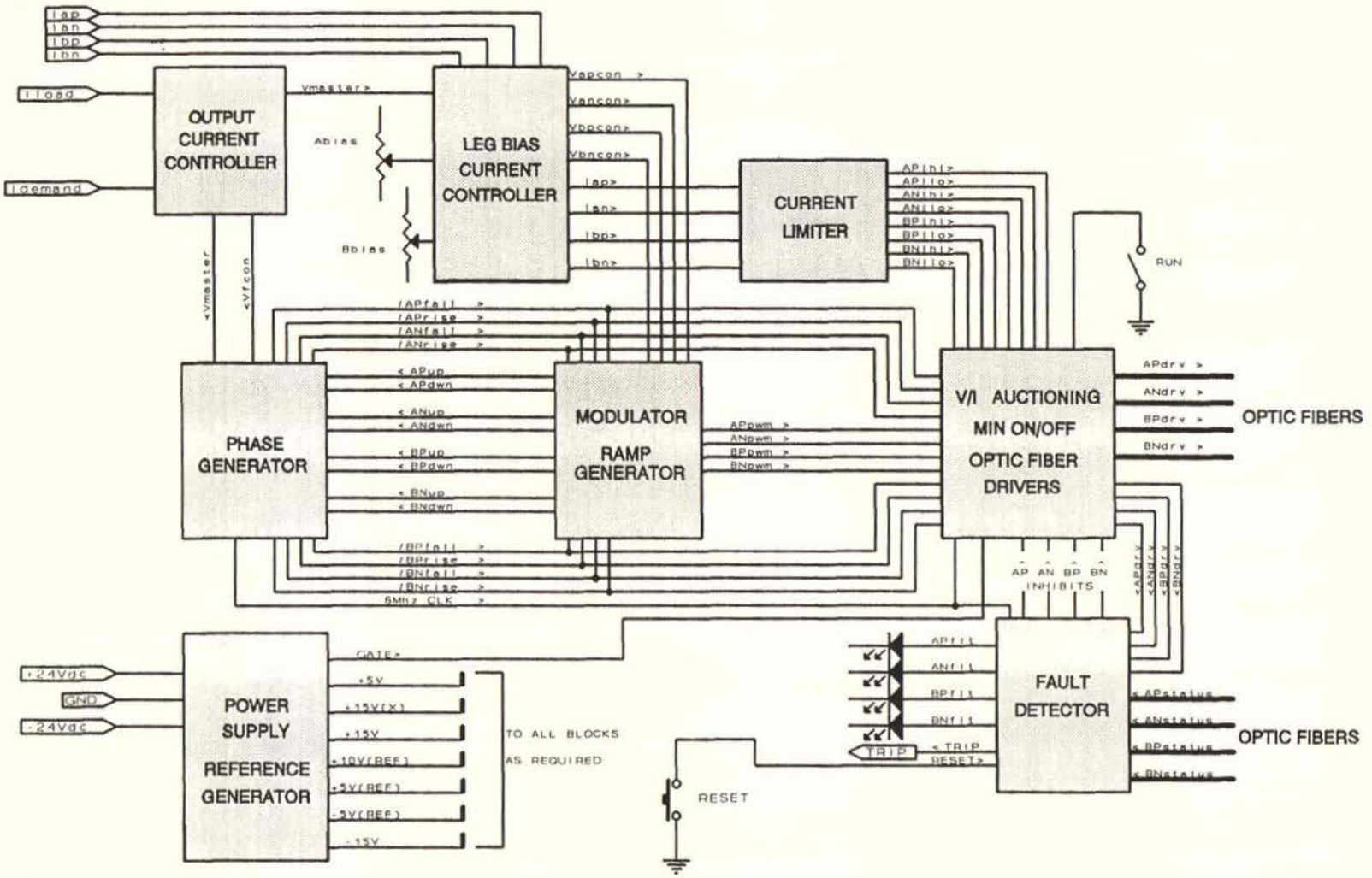


Figure 5.3 Controller System Overview

5.2 Phase/Ramp Generator Operation

The ramp generator function could not be implemented using standard PWM integrated circuits because of several special requirements:

(a) Frequency dropping function

(b) Four phase ramp signals

(c) Symmetrical ramp signals

Symmetrical ramps are not absolutely essential but yield a significantly improved output spectrum as compared to a fixed sawtooth which is most commonly implemented in switchmode power supply control I.C. The type of ramp used in switchmode supply I.C's makes no difference since the modulation is a DC signal. The symmetrical ramp yields what is known as a trailing and leading edge modulator, the benefits of this is discussed in [1].

As previously outlined the frequency dropping function is implemented to extend the dynamic voltage range of the power circuit. At the minimum on and off times of 2.5μS and for a $\pm$ 5V ramp with a 20μS period the modulating signal will be at +3.75V or –3.75V. At these levels, V_{master}, which is the output current loops input to the modulator, is clamped by a analog circuit utilizing precision rectifiers as illustrated in Figure 5.4. At the same levels the VCO control voltage, v_{fcon}, begins to reduce from an initial voltage of 5V. The signal V_{fcon} reduces so that when the control voltage V_{con} reaches $\pm$ 5V it will reach zero volts which corresponds to zero frequency. Provision has been made to enable the minimum switching frequency to be set. For the setting shown in Figure 5.4, V_{fcon} would be limited at 0.5V which would result in a minimum switching frequency of 5kHz and therefore a maximum duty ratio of 0.9875. In practice it was found that lower limits could be used with no apparent difficulty.

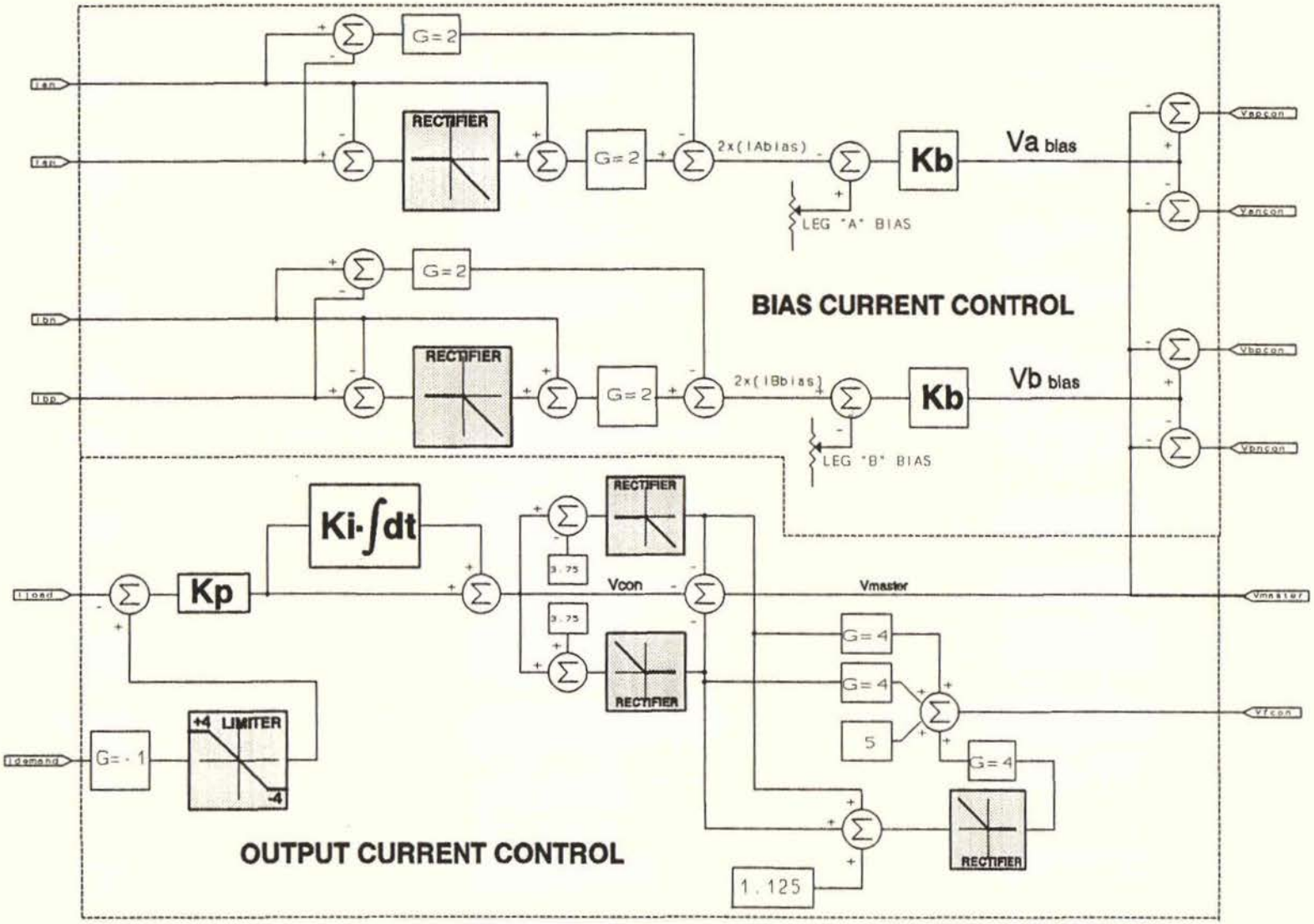


Figure 5.4 Controller Detailed Block Diagram Part "A"

The signal V_{master} is combined with signals originating from the two leg bias current controllers to provide the analog input signals Vap_{con}, Van_{con}, Vbp_{con} and Vbn_{con} to the four modulators. Figure 5.5 shows the block diagram of the remainder of the controller including the Phase/Ramp Generator and Modulator. The VCO provides a nominal frequency of 200kHz to the synchronisation generator which uses frequency dividers to obtain the four phase pulse train. A detailed schematic diagram of the phase generator is shown in Figure 5.6.

The design of the VCO is quite novel in that it displays a crystal locked upper frequency. This is a very important feature since any deviation above the nominal frequency of 200kHz will cause pulse dropping and result in output noise. It was found in practice that relying on a fixed maximum analog voltage to fix the maximum frequency was deficient in this respect. Noise on the V_{fcon} causes random dropping of pulses. To overcome this problem two VCO's are employed one is crystal locked at 3.2000MHz and the other has RC timing such that its output frequency is approximately 3.2000Mhz with a control voltage of 5V. By lightly coupling the output of the crystal locked oscillator into the other VCO's timing circuit via resistor R_x it will tend to synchronize them together. The reason for this is that the capacitor C_x is being charged by an internal current source plus a small current coupled in from the other oscillator. At some voltage across C_x a comparator will be triggered. If the natural oscillation frequency of VCO "A" is above that of the crystal locked oscillator the average charging rate will be reduced which will tend to drive it to a lower frequency. The opposite happens if the VCO "A" frequency is low. Hence there is a tendency for the two VCO's to phase lock. When the control voltage is lowered the two will initially stay locked but a point will be reached where the small amount of signal which is coupled into VCO "A" is insufficient, the frequency will deviate and be determined by the control voltage.

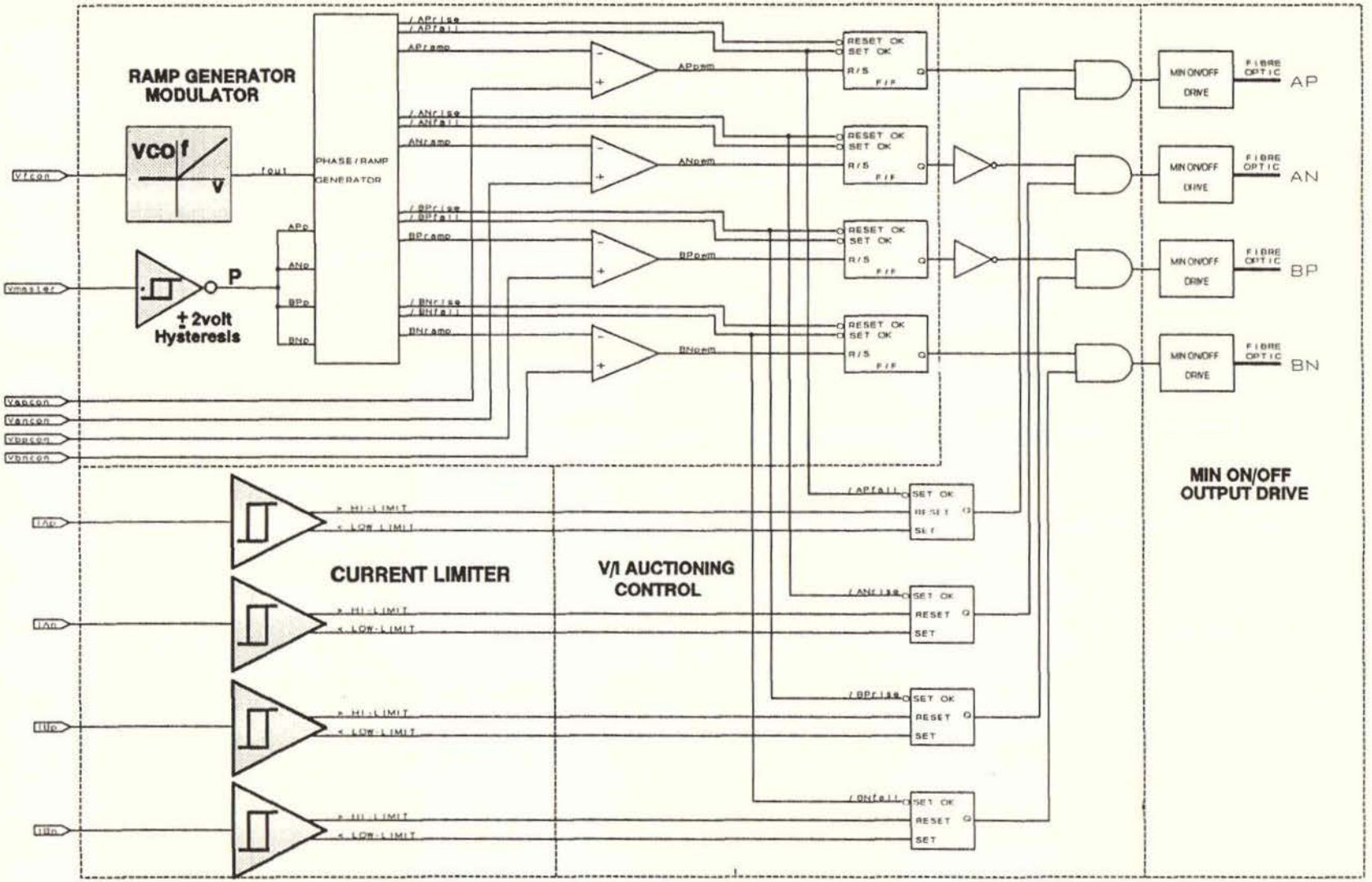


Figure 5.5 Controller Detailed Block Diagram Part "B"

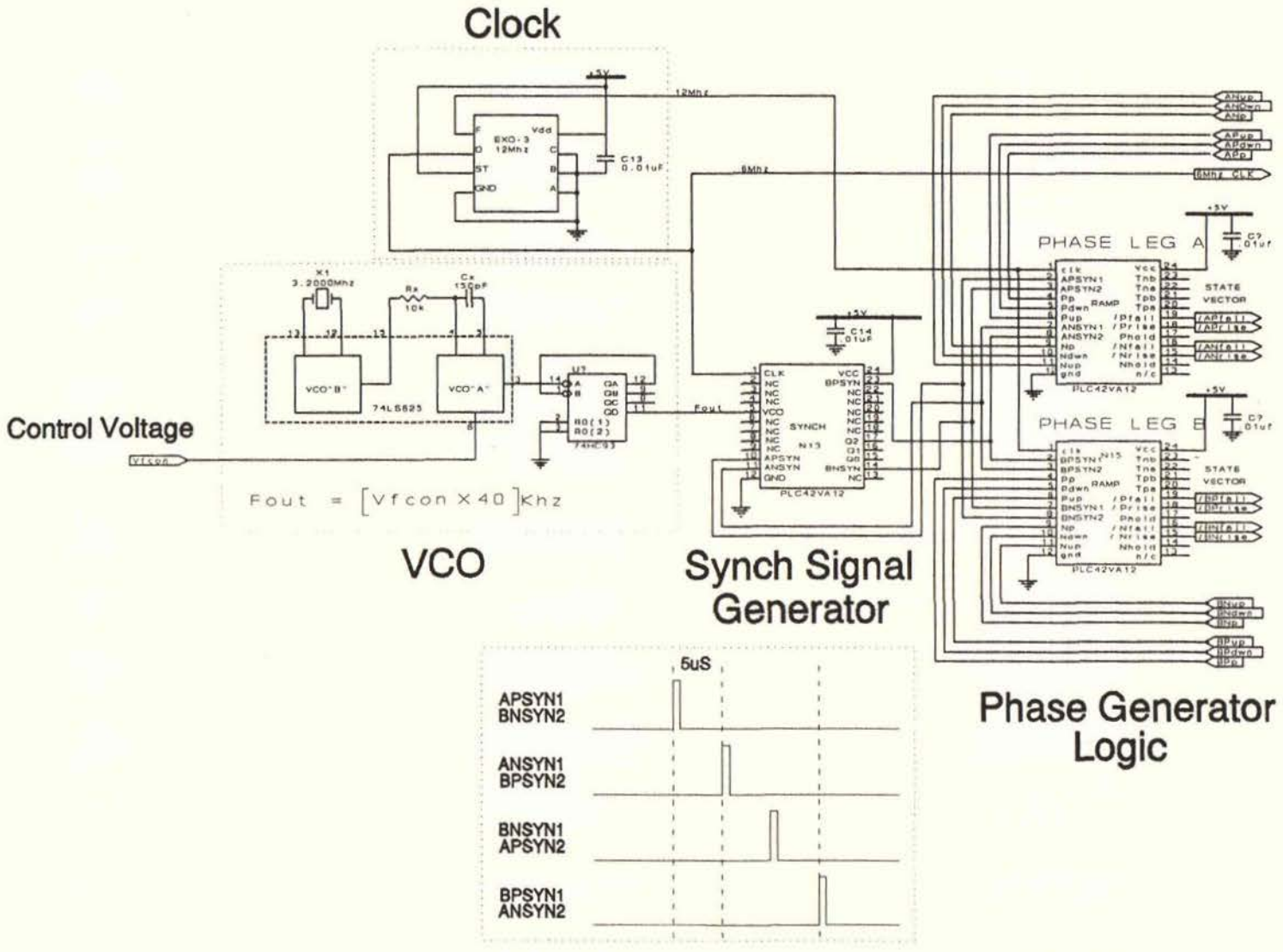


Figure 5.6 Phase Generator Schematic Diagram

This introduces a dead zone non–linearity to the control loop. The dead zone must be sufficiently large so as it contains the maximum peak to peak noise on the analog signal. Fortunately because the analog noise is already low the dead zone need only be small (5 – 4.85V was used). Since the dead zone non–linearity, in classical control systems terms, acts to reduce the gain and does not cause any phase shift there is no effect on the loop stability. In practice for the small dead zone introduced there is no apparent effect on the the closed loop control performance. The output of the VCO "A" is nominally 3.2000Mhz, this is divided down by a binary counter to give f_{out} = 200.0kHz signal. The f_{out} signal is fed to the synchronisation generator which gives the four phase output, AP_{syn}, AN_{syn}, BP_{syn} and BN_{syn}. These signals are used to trigger the ramp generator cycles. The synchronisation generator logic is implemented in a PLC42VA12 PAL.

Figure 5.7 describes the ramp generator operation. The ramp generator works in one of two different cycles depending if V_{master} is positive (which corresponds to a negative output voltage) or negative. The signal "P" determines which cycle the ramp generator operates in. When "P=1" the output voltage is positive and the ramp generator works in a RISE, FALL followed by HOLD mode. The reason that the ramp generator is configured this way is that the minimum off time for the PWM signal, which is determined by the 3.75V clamping level as previously discussed, is allowed to remain constant while the on time is stretched during the hold period. The synchronisation pulse determines when the hold period finishes and the next cycle begins. The logic causes the ramp signal to rise to +5V at which time the "UP=1" signal triggers the ramp to fall until –5V is reached where the "DWN=1" signal causes the ramp to go into a hold and the logic waits for the next synchronisation pulse. The frequency of the synchronisation pulses reduces as the VCO frequency reduces. During the negative output voltage when "P=0" the cycle becomes FALL, RISE and HOLD the ramp waveform is therefore inverted to that of "P=1".

This means that the PWM on time is allowed to remain constant while the off time is stretched. Two synchronisation pulses are actually used, when "P=1" The SYN1 signal is used and the ramp is synchronised on the rising ramp, when "P=0" the cycle is synchronised on the falling ramp with the SYN2. SYN2 is delayed by half a cycle from SYN1. The SYN2 signals are simply the SYN1 from another phase as shown in Figure 5.6. The use of two synchronisation signals ensures there is minimum disturbance during the transition from "P=1" to "P=0" to the five level modulation scheme.

The logic that controls the ramp generator cycle is implemented as a state machine. The state transition diagram shown in Figure 5.7 illustrates the operation described above diagrammatically. The two state machines for one leg are implemented in a single PLC42VA12 PAL. The next state logic expressions are also displayed in Figure 5.6.

The analog ramps are generated by converting the digital state to an appropriate analog voltage which is fed to an inverting integrator as illustrated in Figure 5.8. During the rise phase the integrator is presented with –5V and during the fall phase +5V. In the following discussion the "AP" converter control is used as an example. The digital signals $/AP_{rise}$ and $/AP_{fall}$ drive an Op–amp circuit via mosfets V_1 and V_2 which provides the desired analog voltages. With V_1 turned on and V_2 off the circuit becomes a non–inverting amplifier with a gain of unity with a 5.00V input voltage. This corresponds to the falling phase. With V_2 turned on and V_1 turned off the circuit becomes an inverting amplifier of unity gain with a 5.00V input. This corresponds to the rising phase. The 5.00V input voltage is generated from a precision reference. When both V_1 and V_2 are switched on the integrator input is zero volts and the HOLD period is entered. The integrator ramp times are controlled by an RC time constant. The capacitor is a high accuracy low drift type. The resistors are adjusted to make the ramp up time plus the ramp down time be as close to the synchronisation pulse period, when not frequency dropping, as possible.

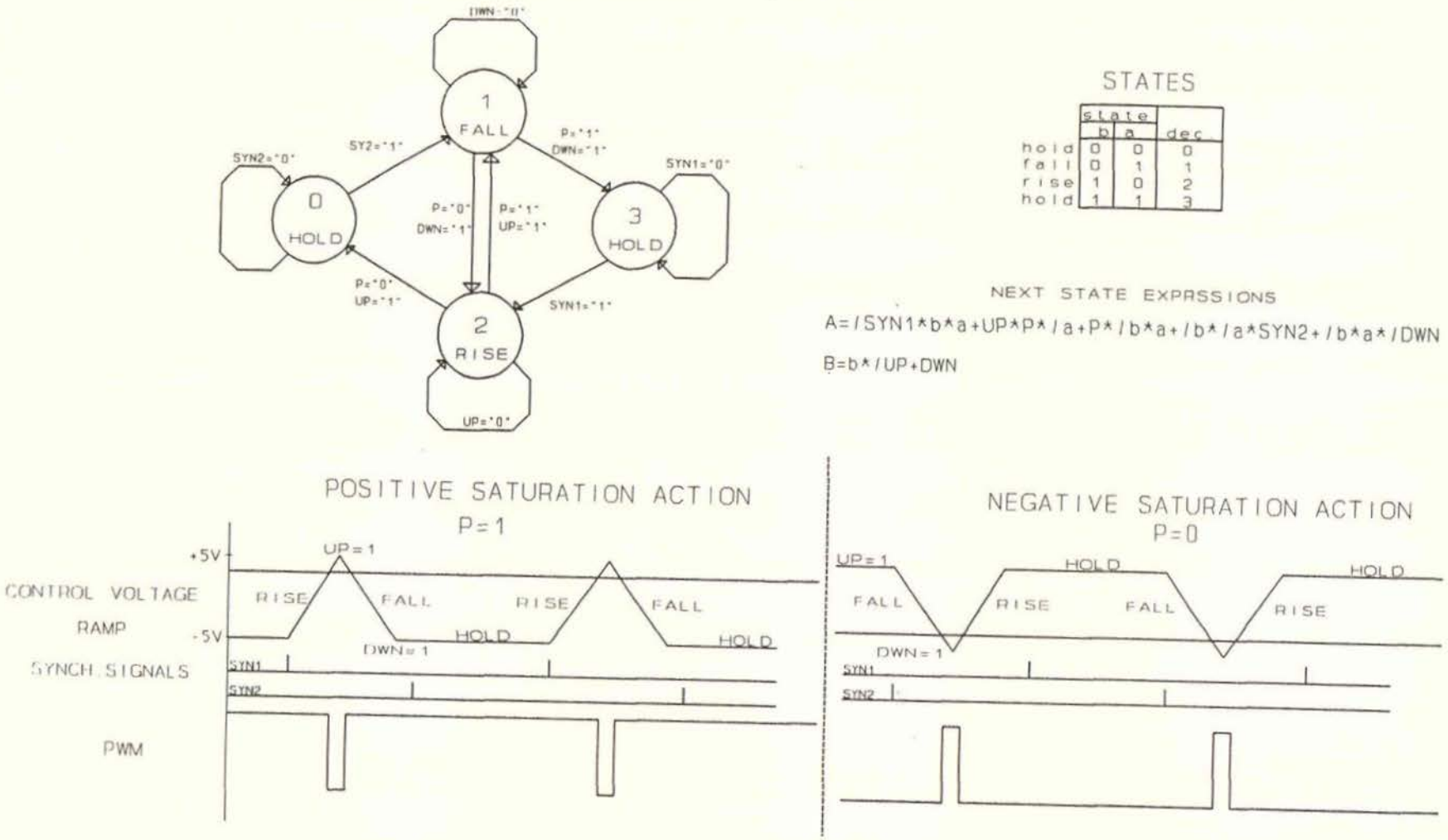


Figure 5.7 Phase Generator Logic Operation

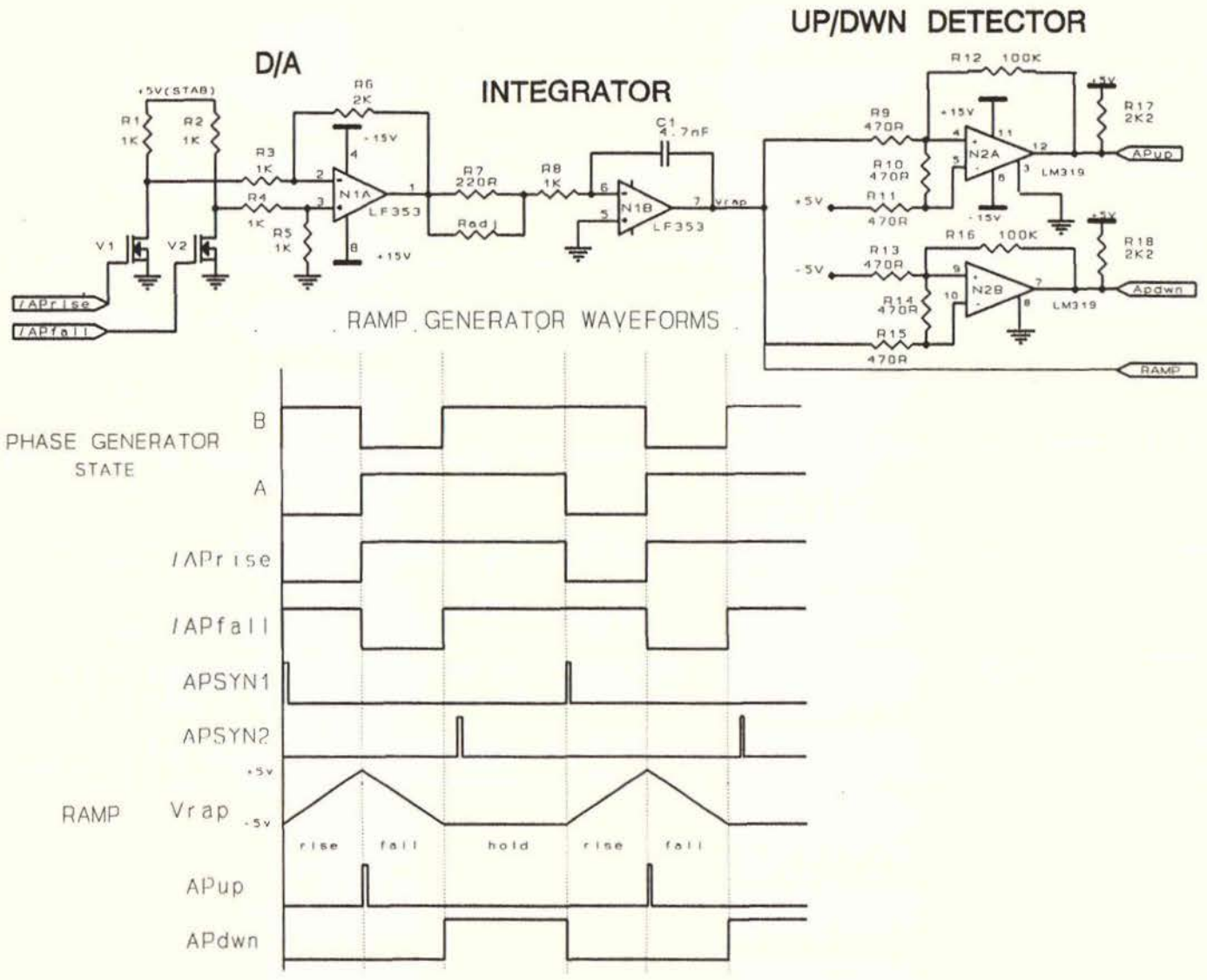


Figure 5.8 Ramp Generator Analog Operation

It is impossible to make this adjustment perfect since any ramp period variations will cause synchronisation pulses to be missed resulting in pulse dropping. This means the state machine will always enter the hold period for a small period, in practice this is adjusted down to approximately 0.5μS. The adverse effect of this is that during the "P=1" to "P=0" transition or visa–versa there will be a 0.5μS jump in the pulsewidth which represents a 28V jump in output voltage. The effect of this is to introduce a slight distortion in the output, this however has not posed a serious problem since it is suppressed by the overall amplifier negative feedback. Also the hysteresis which is applied in the detection of "P" is wide being $\pm$2V so that at low signal levels there is no change in "P" and therefore no duty cycle jump. The upper and lower limits of the integrator output are detected by comparators which generate the AP_{up} and AP_{dwn} signals. These feedback to the phase generator logic to initiate the next part of the cycle. The ramp limits are set at $\pm$5V. Example waveforms for the "AP" converter for the "P=1" case are shown in Figure 5.8.

The four phase shifted ramp signals feed the pulse width modulator comparators together with the appropriate analog control signal for each phase. The PWM output is fed to flip flops which are implemented to prevent switching chatter from occurring. The flip flops are the reset/set(reset dominant) type. These are implemented as part of the V/I auctioning subcircuit PALs. They also have "RESET OK" and "SET OK" gates. During the rising ramp the flip flops are allowed to reset but a set is inhibited. During the falling ramp a set is allowed and the reset is inhibited. The fall and rise signals from the phase generator are used to gate the flip flops. This system prevents multiple switching or chatter that often occurs in switch mode equipment as a result of noise originating from the power circuits.

It should be noted that the "AN" PWM signal is inverted before being delivered to the drivers. The reason for this is to produce positive output voltage the "AN" converters IGBT must be switched off and the current allowed to flow in the freewheel diode. Also the "BP" and "BN" choppers are driven in the inverse manner to the "AP" and "AN" choppers so as to produce the inverse average voltage at the coupling transformer center tap, that is the two legs are driven differentially to produce the resultant output voltage.

5.3 Bias Current Control Operation

The bias current as discussed earlier is the minimum of the two converter currents for one phase leg. In terms of an average current expression it is given by the following:

$$I_{bias}(t)= \frac{I_{ap}(t)+I_{an}(t)-abs[I_{ap}(t)-I_{an}(t)]}{2} \qquad 5.3\text{–}1$$

An analog circuit was developed to achieve this expression. This is shown in Figure 5.4. When $I_{ap} > I_{an}$ the output becomes:

$$V_{bias}(t) = [-(I_{ap}(t) - I_{an}(t)) + I_{an}] \times 2 - [I_{an}(t) - I_{ap}(t)] \times 2$$

$$V_{bias}(t) = -2I_{ap}(t) + 4I_{an}(t) + -2I_{an}(t) + 2I_{ap}(t)$$

$$V_{bias}(t) = 2I_{an}(t) = 2I_{bias}(t) \qquad 5.3\text{–}2$$

When $I_{ap} < I_{an}$ the output becomes:

$$V_{bias}(t) = [I_{an} \times 2] - [I_{an} - I_{ap}] \times 2$$

$$V_{bias}(t) = 2I_{ap}(t) = 2I_{bias}(t) \qquad 5.3\text{–}3$$

So this analog system has an output two times the minimum of the two currents. The circuit implementation of this consists of three op–amps, one configured as a precision rectifier and the other two as subtracting amplifiers.

The bias current is compared with an adjustable setpoint and fed to a proportional controller. It should be noted the "B" leg bias controller error junction is reversed to that of the "A" leg. This is necessary because of the inversion in the drive signals for the "B" leg which is required to produce the differential action as previously explained. The bias current control signal drives the control signals for each converter differentially that is it is added to positive converters control signal and subtracted from the negative converters control signal. For example if more bias current is required in the "A" leg the bias current control signal will increase V_{apcon} and decrease V_{ancon} which results in a positive average voltage ($V_{ap} - V_{an}$) across the magnetizing inductance.

The bias current control loop gain is set by adjustment of K_b which in practice is simply done by changing a resistor value. The selection of K_b will be discussed in Section 5.7.

5.4 Output Current Control Operation

The output current control action is proportional plus integral as shown in Figure 5.4. The integral term is clamped at $\pm$5V which corresponds to the dynamic limit for the pulse width modulator. This minimises the overshoot during transients where the system saturates. Without clamping the system can suffer from "wind–up reset" type behavior where the integral term increases excessively during a transient due to saturation some where in the system. This causes a large overshoot during the wind–up stage and a less but still large undershoot during the reset period. The P+I control is implemented using a single Op–amp with zener diode clamping across the integration capacitor.

The current demand is passed through a limiting amplifier which sets the maximum output current in either direction. This is normally set at $\pm$4V which corresponds to $\pm$80A. With 20A of Bias current this would mean that two converters would carry 100A which corresponds to their maximum continuous rating. Providing that the control system is functioning correctly the maximum continuous rating will never be exceeded.

The main control signal V_{con} is fed through a specialized limiter circuit to obtain V_{master} and also through a function generator to give the frequency control signal V_{fcon} as presented in Figure 5.4. The function generator and limiter is actually an integrated system. This is necessary to ensure that V_{fcon} commences to be reduced at precisely the same level V_{master} is clamped. If $0 < V_{con}(t) < 3.75V$ (3.75V corresponds to 0.875 duty ratio):

$$V_{master}(t) = -V_{con}(t)$$

$$V_{fcon} = 5V$$

$$f_s = 50kHz$$

If $-3.75 < V_{con}(t) < 3.75V$:

$$V_{master}(t) = (V_{con}(t) - 3.75) - V_{con}(t) = -3.75V$$

$$V_{fcon}(t) = -(V_{con}(t) - 3.75) \times 4 + 5$$
$$= 4\,(5 - V_{con}(t))V$$

$$f_s = 40.0\,(5 - V_{con}(t))kHz$$

If $V_{con}(t) > 4.875V$

$$V_{master}(t) = -3.75V$$

$$V_{fcon}(t) = 0.5V$$

$$f_s = 5.0kHz$$

The 5kHz switching frequency is the minimum in this case. The same procedure applies for $-4.875 < V_{con}(t) < 0$. The duty ratio is given by:

$$D = \frac{T_{on}}{T_{on} + T_{off}} = 1 - \frac{T_{off}}{T_s}$$

The off time for $V_{con} > 3.75V$ during frequency dropping is fixed at 2.5 μS and the period T_s is given by:

$$T_s(t) = \frac{1}{0.04\ (5 - V_{con}(t))}\ \mu S$$

Therefore during frequency dropping the transfer function from control voltage to duty ratio becomes:

$$D(t) = 1 - 2.5 \times 0.04(5 - V_{con}(t))$$

$$D(t) = 0.1\ V_{con}(t) + 0.5$$

The modulator transfer function for each segment can be similarly found:

$-4.875 < V_{con}(t) < -3.75$ $D(t) = 0.1\ V_{con}(t)+0.5$ (frequency dropping)

$-3.75 < V_{con}(t) < 0$ $D(t) = 0.1\ V_{con}(t)+0.5$

$0 < V_{con}(t) < 3.75$ $D(t) = 0.1\ V_{con}(t)+0.5$

$3.75 < V_{con}(t) < 4.875$ $D(t) = 0.1\ V_{con}(t)+0.5$ (frequency dropping)

Using the frequency dropping strategy yields a constant relationship throughout the entire duty cycle range. The minimum frequency limit can be set by changing resistor values. The value selected was 5kHz though this is arbitrary. In practice frequencies down to 1kHz have been found to work quite satisfactory, however the VCO starts to become non–linear in this range. The important advantages of the frequency dropping scheme over the traditional pulse dropping system commonly found in variable speed motor drives is that first the relationship between converter output and control voltage remains linear.

For this topology it is important that the five level modulation is preserved throughout the duty cycle range. The low frequency operation does not present any control system stability problems. The reason for this is, it is excessive switching ripple that causes the control system to behave abnormally. The ripple is determined by the volt–second area of the minimum on or off pulses, which remains constant. The ripple does not increase during frequency dropping.

Figure 5.9 shows an actual oscillograph trace taken from the scale model when operating in the frequency dropping mode. The V_{fcon} signal on a scale of 2V/div and the output current on a scale of 4A/div, which is equivalent to 40A/div on the full scale unit, are shown. A 1kHz modulating signal is used. The V_{fcon} signal normally rests at 5V and reduces when required by the controller. In this case V_{fcon} reduces to its lower limit of 0.5V corresponding to f_s = 5kHz. Notice that the frequency minimum and hence the output voltage maximum occurs before the current maximum, This simply reflects the lagging power factor of the load. Even though the modulator is being driven through its full range with maximum frequency dropping the output current waveshape is still of high quality. This verifies the high standard of performance that this new strategy offers.

In Figure 5.10 the "AP" converter output voltage on a scale of 20V/div and the output current on a scale of 4A/div are shown for a 1kHz modulating signal. The frequency dropping period is clearly indicated by the pulse stretching in the PWM. Note the good pulse regularity and the absence of distortion in the output current waveform during the frequency dropping period.

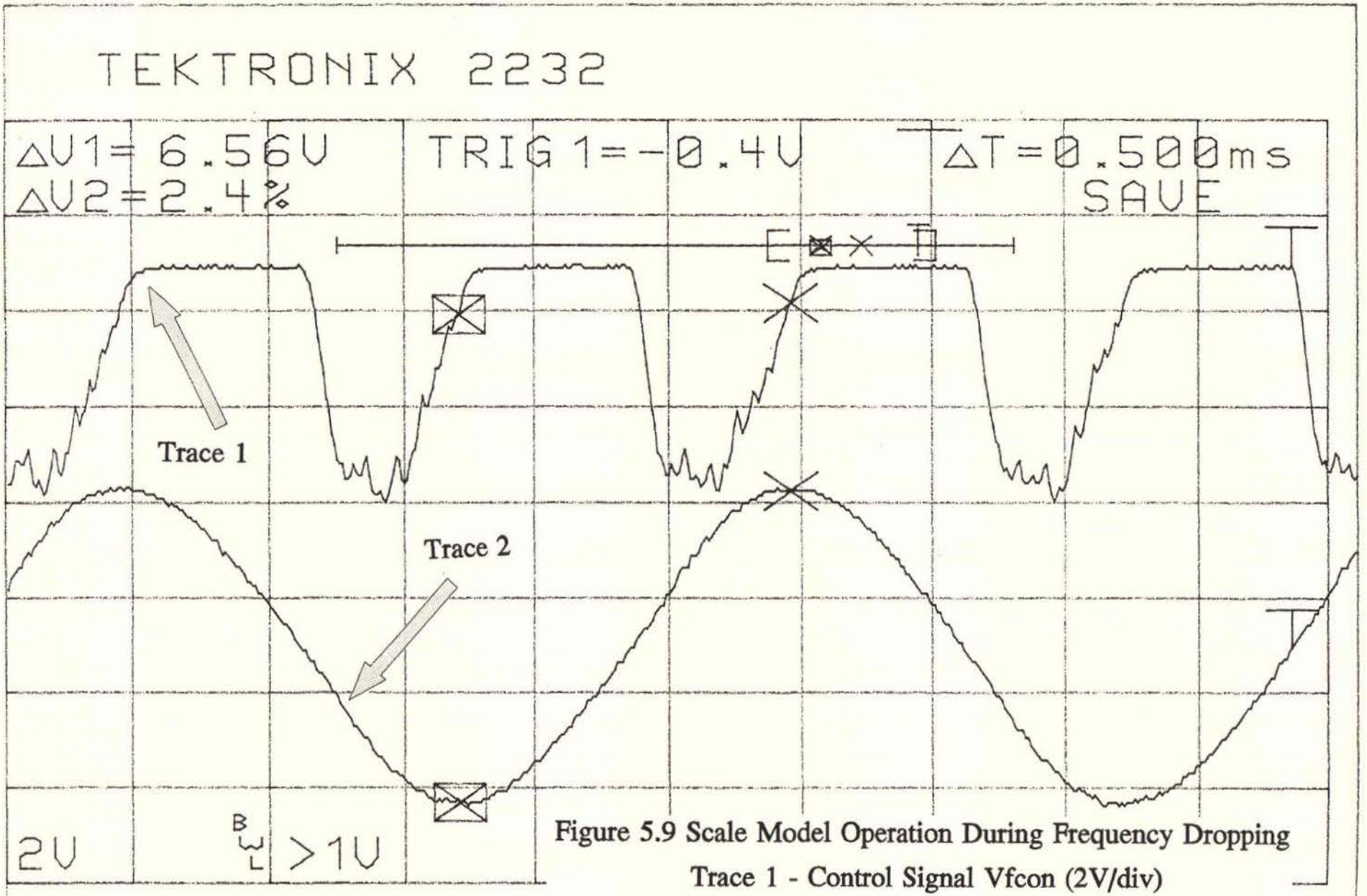


Figure 5.9 Scale Model Operation During Frequency Dropping

Trace 1 - Control Signal Vfcon (2V/div)

Trace 2 - Output Current (4A/div)

Time Base - 0.2mS/div

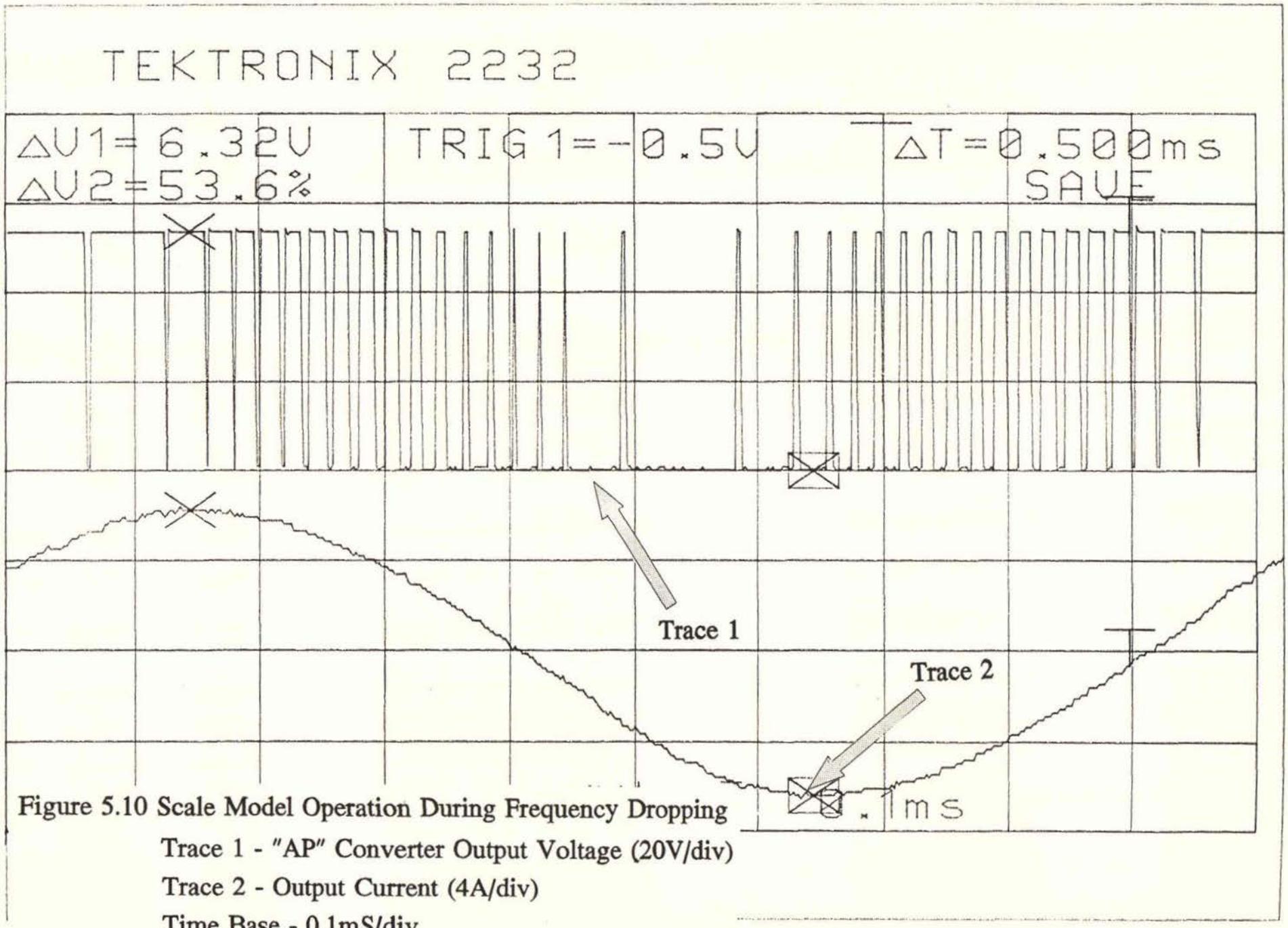


Figure 5.10 Scale Model Operation During Frequency Dropping

Trace 1 - "AP" Converter Output Voltage (20V/div)

Trace 2 - Output Current (4A/div)

Time Base - 0.1mS/div

5.5 Current Limiter Operation

Under normal conditions the output is naturally current limited, however failure of the controller, transducers or the power circuit may cause an elevation in converter currents and possible catastrophic failure. To reduce the probability of this occurring additional hysteresis type current limiting has been implemented as shown in Figure 5.5.

The output current from each converter is compared against a high and a low level reference. If the current exceeds the high level a R/S flip flop is reset which turns the appropriate IGBT off. Since flywheeling now occurs the current will decrease. Once the current reduces below the low level setpoint the flip flop will be set and therefore the IGBT is turned back on. The set signal is gated by either a FALL or RISE logic signal from the phase generator so that the leading edge generated by the current limiter is always synchronized with a leading edge generated by the pulse width modulator. The use of this strategy yields the smoothest possible operation of the current limit and prevents the possibility of sustained high frequency switching. The high limit setpoint should be set at 110A and the low level limit setpoint should be set at 90A. This means under hysteresis control the average converter current will be limited to 100A. In normal operation the high limit should never be exceeded. The current limiter protects the converter against faults such as failure of a current transducer, failure of a buck converter or malfunction of the main or bias control loops.

Shown in Figure 5.11 is an actual oscillograph trace of the output for the scale model under control of the current limiter. In this case the current limiter setpoints have deliberately been set lower than the normal current demand which is also shown. The operation of the "AP" current limiter on the scale model with the "AN" IGBT short circuited was also tested and found to protect the entire unit from further damage.

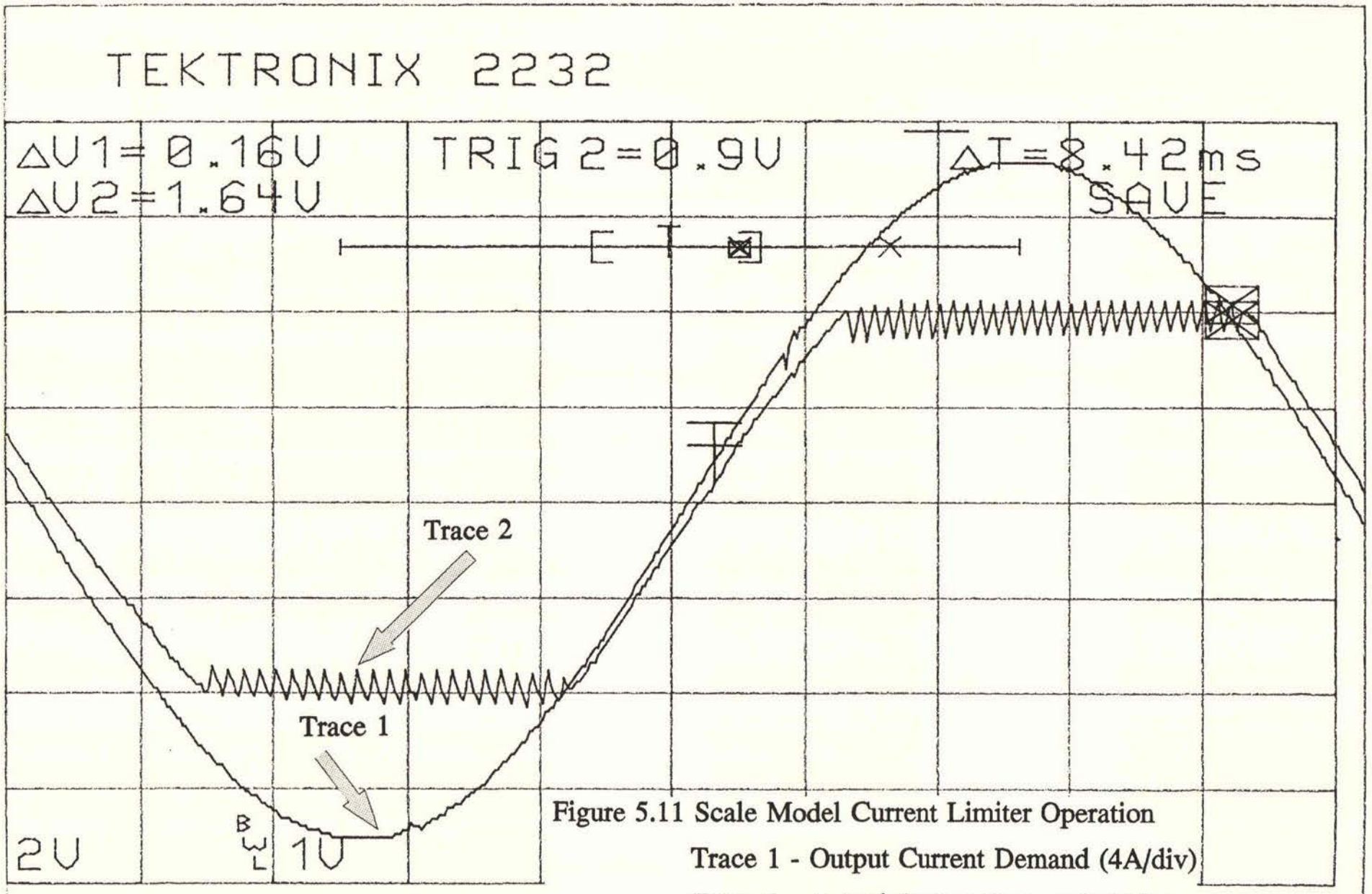


Figure 5.11 Scale Model Current Limiter Operation

Trace 1 - Output Current Demand (4A/div)

Trace 2 - Actual Output Current (4A/div)

5.6 Control Systems Design

In this section the parameter settings for the the output and bias current control loops will be discussed. A control systems block diagram is shown in Figure 5.12. In this application the switching ripple is sufficiently small to allow state space averaging to be applied. As a result classical analysis is applicable. First consider the transfer function for the modulator and bridge combination. The pulsewidth modulators use naturally sampled with symmetrical ramps. This means that from the classical control point of view they do not introduce any phase shift in the system, [44]. From Section 5.4 it was shown that the modulator transfer function is:

$$D(t) = 0.1\ V_{con}(t) + 0.5 \qquad 5.5\text{–}1$$

The average voltage at the coupling transformer center tap is:

$$\text{"A" LEG: } V_a(t) = \frac{V_{ap}(t)+V_{an}(t)}{2} \qquad 5.5\text{–}2$$

$$\text{"B" LEG: } V_b(t) = \frac{V_{bp}(t)+V_{bn}(t)}{2} \qquad 5.5\text{–}3$$

Therefore the output voltage will be:

$$V_o(t) = \frac{V_{ap}(t)+V_{an}(t)}{2} - \frac{V_{bp}(t)+V_{bn}(t)}{2} \qquad 5.5\text{–}4$$

From equation 5.5–1:

$$D_{ap}(t) = 0.1\ V_{apcon}(t) + 0.5 \qquad 5.5\text{–}5$$

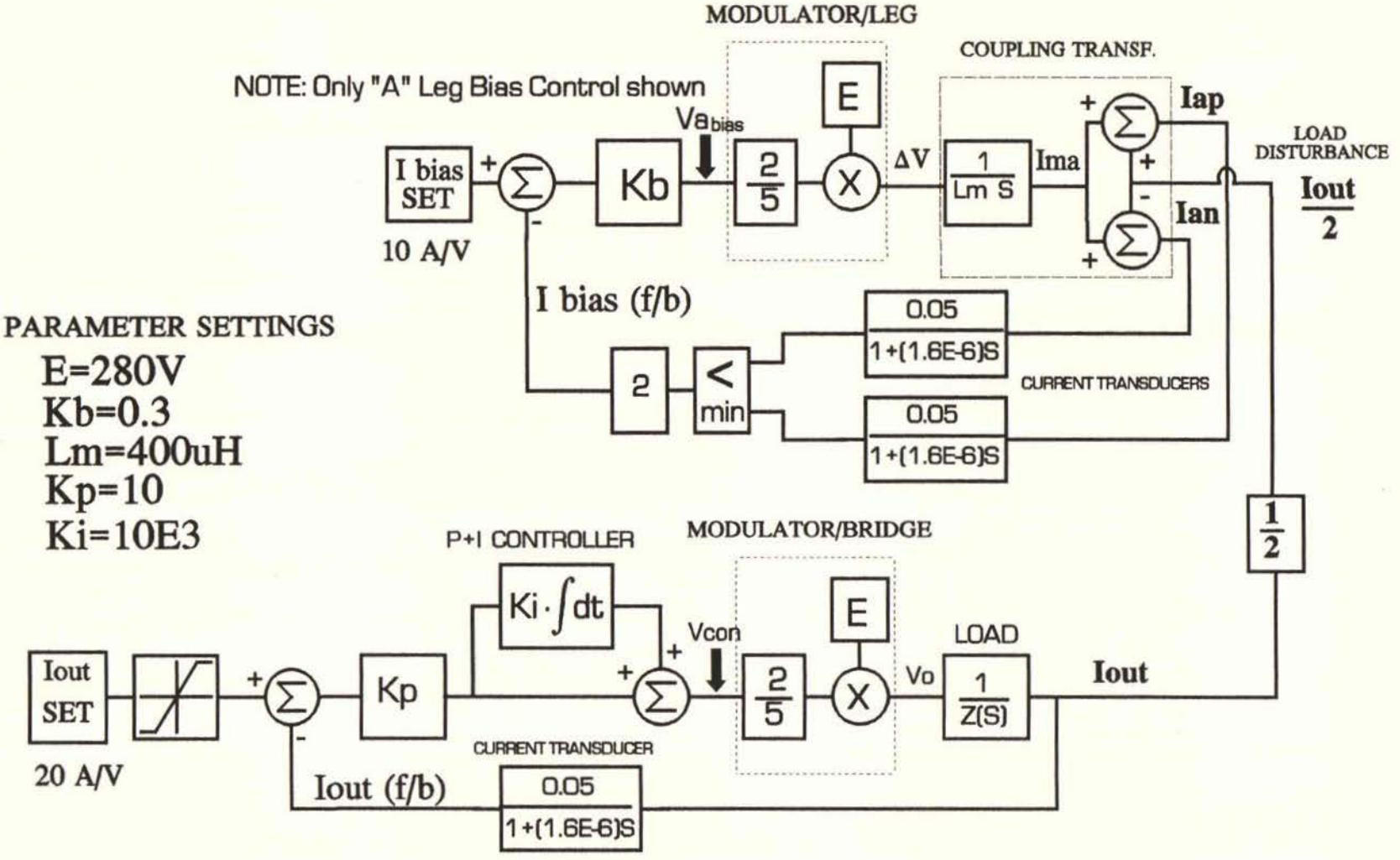


Figure 5.12 Amplifier Control Systems Block Diagram

$$D_{an}(t) = 0.1\ V_{ancon}(t) + 0.5 \qquad 5.5\text{–}6$$

$$D_{bp}(t) = 0.1\ V_{bpcon}(t) + 0.5 \qquad 5.5\text{–}7$$

$$D_{bn}(t) = 0.1\ V_{bncon}(t) + 0.5 \qquad 5.5\text{–}8$$

The converter transfer function is:

$$V(t) = E\ [2D(t) - 1] \qquad 5.5\text{–}9$$

Therefore:

$$\begin{aligned} V_{ap}(t) &= E[2(0.1\ V_{apcon}(t)+0.5)-1] \\ &= 0.2E\ V_{apcon}(t) \end{aligned} \qquad 5.5\text{–}10$$

$$\begin{aligned} V_{an}(t) &= E[2(0.1\ V_{ancon}(t)+0.5)-1] \\ &= 0.2E\ V_{ancon}(t) \end{aligned} \qquad 5.5\text{–}11$$

$$\begin{aligned} V_{bp}(t) &= -E[2(0.1\ V_{bpcon}(t)+0.5)-1] \\ &= -0.2E\ V_{bpcon}(t) \end{aligned} \qquad 5.5\text{–}12$$

$$\begin{aligned} V_{bn}(t) &= -E[2(0.1\ V_{bncon}(t)+0.5)-1] \\ &= -0.2E\ V_{bncon}(t) \end{aligned} \qquad 5.5\text{–}13$$

The "BP" and "BN" converters have inverted logic drives which effectively inverts the output voltage, this produces the differential action between phase legs.

The modulator control voltages are a function of both $V_{master}(t)$ and hence $V_{con}(t)$ and $Va_{bias}(t)$ or $Vb_{bias}(t)$:

$$V_{apcon}(t) = V_{con}(t) + Va_{bias}(t) \qquad 5.5\text{–}14$$

$$V_{ancon}(t) = V_{con}(t) - Va_{bias}(t) \qquad 5.5\text{–}15$$

$$V_{bpcon}(t) = V_{con}(t) + Vb_{bias}(t) \qquad 5.5\text{–}16$$

$$V_{bncon}(t) = V_{con}(t) - Vb_{bias}(t) \qquad 5.5\text{–}17$$

Therefore the output voltage will be given by:

$$V_o(t) = \frac{V_{ap}(t)+V_{an}(t)}{2} - \frac{V_{bp}(t)+V_{bn}(t)}{2}$$

$$V_o(t) = 0.2E\left[\frac{V_{con}(t)+Va_{bias}(t)+V_{con}(t)-Va_{bias}(t)}{2}\right]$$

$$+ 0.2E\left[\frac{V_{con}(t)+Vb_{bias}(t)+V_{con}(t)-Vb_{bias}(t)}{2}\right]$$

$$V_o(t) = 0.4E\ V_{con}(t) = \frac{2}{5}E\ V_{con}(t) \qquad 5.5\text{–}18$$

Notice that because of the method of implementation the bias current control term cancels out. This means that the main control loop works independently of the bias control loop. To analyze the bias current control loop it is necessary to determine the transfer function relating $Vb_{bias}(t)$ to the differential voltage across the coupling transformer $\Delta V(t)$.

The differential voltage across the coupling transformer is given by:

$$\Delta V(t) = V_{ap}(t) - V_{an}(t) \qquad 5.5\text{–}19$$

From equations 5.5–10 to 5.5–17:

$$\Delta V(t) = 0.2E(V_{con}(t) + Va_{bias}(t) - (V_{con}(t) - Va_{bias}(t)))$$

$$\Delta V(t) = 0.4\ Va_{bias}(t) = \frac{2}{5} Va_{bias}(t) \qquad 5.5\text{–}20$$

The coupling transformer is modeled by recognizing that the the differential voltage is applied across the magnetising inductance L_m resulting in a magnetising current $I_{ma}(t)$. The transfer function is therefore:

$$\frac{I_{ma}(s)}{\Delta V(s)} = \frac{1}{L_m(s)} \qquad 5.5\text{–}21$$

The magnetising current adds with $I_o(t)/2$ to give $I_{ap}(t)$ and $I_o(t)/2$ is subtracted to give I_{an}. As previously mentioned $I_o(t)/2$ acts as a disturbing influence on the bias current control loop. Two Hall effect current transducers measure each current and the bias current is derived from these by taking the minimum. Because of the circuit implementation the minimum multiplied by two is actually generated. The current transducer has a sensitivity of 20A/V and a bandwidth 100kHz, therefore the transfer function will be:

$$\frac{V_{trans}(s)}{I_{trans}(s)} = \frac{0.05}{1 + 1.6\times10^{-6}s} \qquad 5.5\text{–}22$$

The output current transducer is of the same type. The Proportional plus Integral output current controller implemented is shown in Figure 5.12. The transfer function for the PI controller will be:

$$\frac{V_{con}(s)}{V_{err}(s)} = K_p\left[1 + \frac{K_i}{s}\right] = K_p\left[\frac{s + K_i}{s}\right] \qquad 5.5\text{–}23$$

This completes the control systems model as presented in Figure 5.12. The bias control analysis will now be considered. Figure 5.13 parts A,B and C shows how the bias current control loop can be simplified. First in Chapter Two (equation 2.3–11) it was shown that the magnetising current is disturbed by the modulus of $I_o(t)/2$, that is:

$$I_{bias}(t) = I_m(t) - \left|\frac{I_o(t)}{2}\right|$$

The feedback transducer plus the minimum block is replaced by a constant gain block of value 0.1. This valid since as will be shown the bandwidth of this loop is more than a decade less than the feedback pole frequency and so its effect on the performance of the loop is very minor.

It is the effect of the output disturbance on the bias current which is of interest to us, so a rearrangement is done to express the bias current in relation to the disturbance. The simplified block diagram of Figure 5.13 (B) is valid under steady state conditions which is quite acceptable for this analysis. At steady state the bias current is equal to the set point current plus the disturbing influence of the output current. A further simplification in Figure 5.11(C) shows that the bias current is disturbed by a filtered version of the rate of change of $\left|I_o(t)/2\right|$.

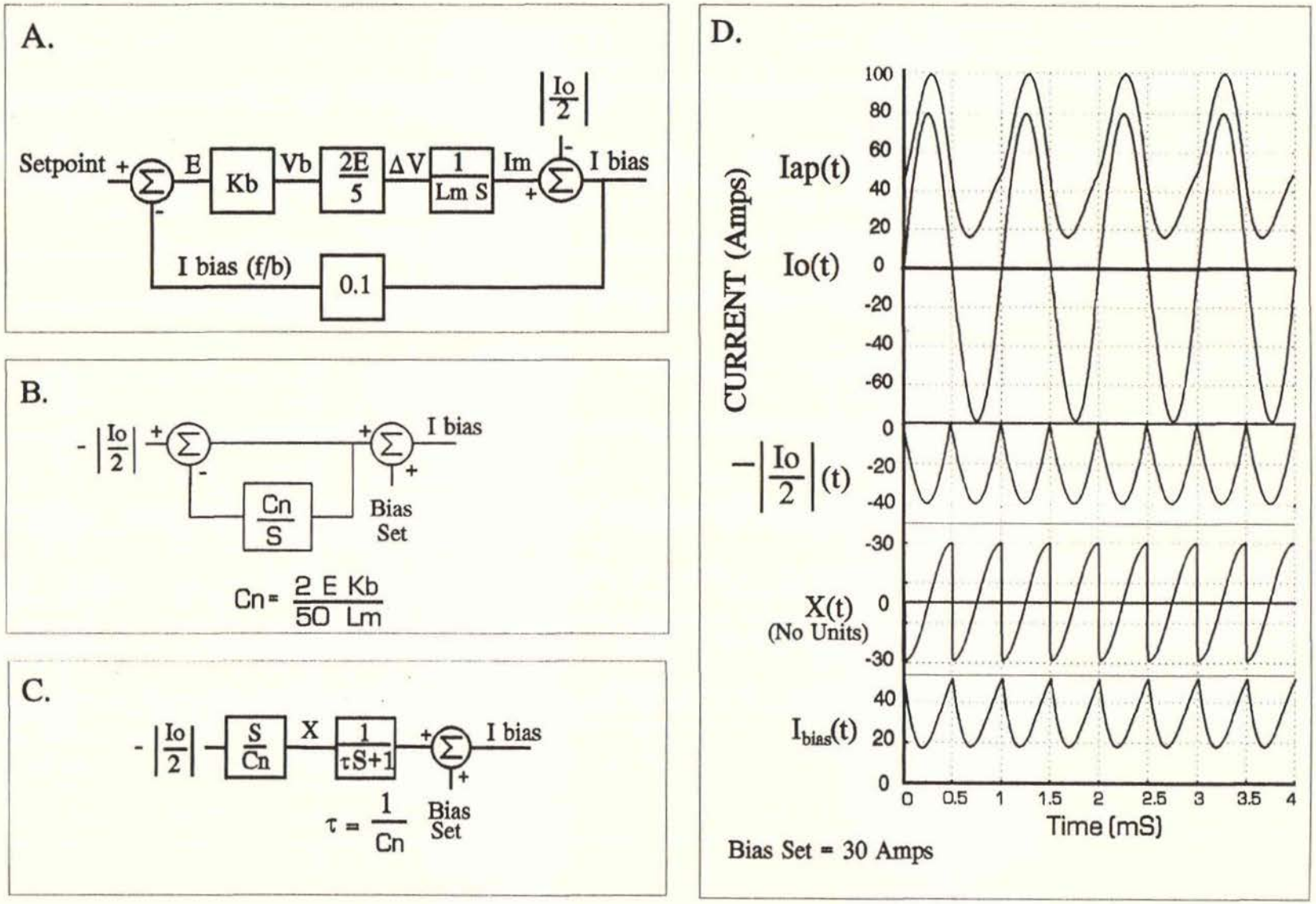


Figure 5.13 Bias Current Control Loop Operation

In the steady state frequency domain the following expression can be written:

$$I_{bias}(j\omega) = I_{set}(j\omega) + [-\left| \frac{I_o}{2} \right|(j\omega)] \frac{j\omega}{j\omega + C_n} \qquad 5.5\text{–}24$$

$$C_n = \frac{2E\ K_b}{50\ L_m} \qquad 5.5\text{–}25$$

At low frequencies ($\omega < C_n/10$) the influence of the disturbance is small. At $\omega > C_n$ the disturbance approaches its maximum level of $\left|I_o/\ 2\right|$. As explained in Section 5.1 and also in Chapter Two, use of a wide bandwidth will improve the attenuation of the disturbance at higher frequencies. However the resulting high coupling transformer differential voltages cause a high level 50kHz spectral component to be generated. Therefore the philosophy adopted is to set the bandwidth at the minimum level possible. The conflicting factor is this is that as the disturbance magnitude becomes larger eventually the idle converters will be forced out of conduction, causing a breakdown in the five level waveform. Therefore a method of calculating the disturbance magnitude for sine wave modulation is desirable. The required relationship will now be derived.

It will be assumed that the output current is sinusoidal with a peak value of I_p and therefore will be given by:

$$I_o = I_p \sin(\omega_m t) \qquad 5.5\text{–}26$$

The bias current disturbance will be:

$$-\left|\frac{I_o(t)}{2}\right| = \frac{-I_p}{2} |\sin(\omega_m t)| \qquad 5.5\text{–}27$$

This can be expressed in the following fourier series expansion:

$$\left|\frac{I_o(t)}{2}\right| = -\frac{I_p}{2}\left[\frac{2}{\pi} - \frac{4}{\pi}\left[\frac{\cos(2\omega_m t)}{1\cdot 3} + \frac{\cos(4\omega_m t)}{3\cdot 5} + \frac{\cos(6\omega_m t)}{5\cdot 7} + \cdots\right]\right]$$

Because the 4th and higher harmonics are relatively small in magnitude using only the 2nd harmonic gives a close approximation:

$$-\left|\frac{I_o(t)}{2}\right| \approx -\frac{I_p}{2}\left[\frac{2}{\pi} - \frac{4}{\pi}\left[\frac{\cos(2\omega_m t)}{3}\right]\right] \qquad 5.5\text{–}28$$

The system of Figure 5.13 will not pass the DC term of equation 5.5–28 and the 2nd harmonic will be attenuated. The 2nd harmonic term is given by:

$$I_{2nd}(t) = \frac{2I_p}{\pi}\left[\frac{\cos(2\omega_m t)}{3}\right] \qquad 5.5\text{–}29$$

The gain and phase of the system at the 2nd harmonic frequency is found from equation 5.5–24 to be:

$$G_{2nd} = \frac{2\omega_m}{\sqrt{4\omega_m{}^2 + C_n{}^2}} \qquad 5.5\text{–}30$$

$$\phi_{2nd} = 90 - \mathrm{Tan}^{-1}\left[\frac{2\omega_m}{C_n}\right] \qquad 5.5\text{–}31$$

The disturbing current magnitude will therefore be approximated by:

$$I_{dist} \approx \frac{2I_p}{3\pi} \times \frac{2\omega_m}{\sqrt{4\omega_m{}^2 + C_n{}^2}} \qquad 5.5\text{–}32$$

The Bias current will therefore be approximated by:

$$I_{bias}(t) \approx I_{set}(t) + \frac{4I_p\omega_m}{3\pi} \frac{1}{\sqrt{4\omega_m{}^2 + C_n{}^2}} \cos(2\omega_m t + \phi_{2nd}) \qquad 5.5\text{–}33$$

The minimum converter current will therefore be:

$$I_{min} = I_{set} - \frac{4I_p\omega_m}{3\pi} \frac{1}{\sqrt{4\omega_m{}^2 + C_n{}^2}} \qquad 5.5\text{–}34$$

Simulations and trials on the scale model were run using the following parameter values:

$$E = 280 \text{ V}, K_b = 0.3, L_m = 400\mu\text{H}$$

Using these values the corner frequency C_n from equation 5.5–25 will be:

$$C_n = \frac{2E\ K_b}{50\ L_m} = \frac{2 \times 280 \times 0.3}{50 \times 400 \times 10^{-6}} = 8400 \text{ r/sec}$$

A control systems simulation based on the model presented Figure 5.13 was run for an 80A peak 1 kHz sinusoidal modulating signal. The results are presented in Figure 5.13 (D) of Figure 3. The bias current setpoint was given a value of 30A . The output current the bias current and the resulting converter current are presented. In addition to this the waveform at point "X" in Figure 5.13 (C) is displayed in order to give a conceptual appreciation of how the bias current and hence the converter current obtains its shape. The signal $-|I_o/2|$ is differentiated and then passed through a low pass filter. The accuracy of 5.5–34 will now be tested against the simulation result.

The minimum bias current from equation 5.5–34 becomes:

$$I_{min} \approx I_{set} - \frac{4I_p\omega_m}{3\pi} \frac{1}{\sqrt{4\omega_m{}^2 + C_n{}^2}}$$

$$I_{min} \approx I_{set} - I_p \frac{4 \times 1000 \times 2\pi}{3\pi} \frac{1}{\sqrt{4 \times (1000 \times 2\pi)^2 + 8400^2}}$$

$$I_{min} \approx I_{set} - 0.176I_p$$

For an 80A peak current:

$$I_{min} \approx I_{set} - 14.1A$$

$$I_{min} \approx 30 - 14.1 = 15.9A$$

The actual simulation shows that the minimum current is 17A which indicates the approximate formula gives a good result. This is an important formula since it allows a decision to be made on the bias current setpoint and the value of K_b. For frequencies above 1kHz (6283 rads/sec) I_{min} increases only weakly with increasing ω_m since this is near the corner frequency of 8400 rads/sec. Therefore lowering the bias current set point to 20A would not present a problem. This would mean that the minimum converter current would be 5.9A at 1kHz and would rise to 20A at low frequencies. Also the peak converter current is at its highest at low frequencies and will be 100A with a bias current setpoint of 20A. The power circuit has been designed to continuously supply 100A.

To complete the analysis the stability of the bias current control loop must be considered.

The forward path transfer function is given by:

$$G(S) = \frac{2\ E\ K_b}{5\ L_m}\frac{1}{s} \qquad 5.5\text{–}35$$

The feedback transducer cascaded with the circuit that derives the bias current has the following transfer function:

$$H(s) = \frac{6.25\times10^4}{(s + 6.25\times10^5)} \qquad 5.5\text{–}36$$

Therefore the open loop transfer function will be:

$$GH(s) = \frac{C_n}{s} \times \frac{6.25\times10^5}{(s + 6.25\times10^5)} \qquad 5.5\text{–}37$$

For the parameter settings already presented:

$$GH(s) = \frac{8400}{s} \times \frac{6.25\times10^5}{(s + 6.25\times10^5)} \qquad 5.5\text{–}38$$

Figure 5.14 shows a bode diagram for this system. There are two aspects of interest, first the phase margin and secondly the influence of switching ripple in the system. The phase margin is 90° and the closed loop response is virtually first order since the feedback pole occurs at a low open loop frequency. So from a stability point of view the proposed settings are excellent. The switching ripple frequency in this loop at 50kHz from Chapter Two has a peak to peak level of 8.4A @ E = 280V;L_m = 400μH. The ripple current is superimposed on the magnetising current and hence also on the bias current. After passing through the transducers it becomes a 0.76$V_{p\text{-}p}$ ripple. Since K_b is 0.3 the ripple level at the input to the modulator is 227m$V_{p\text{-}p}$.

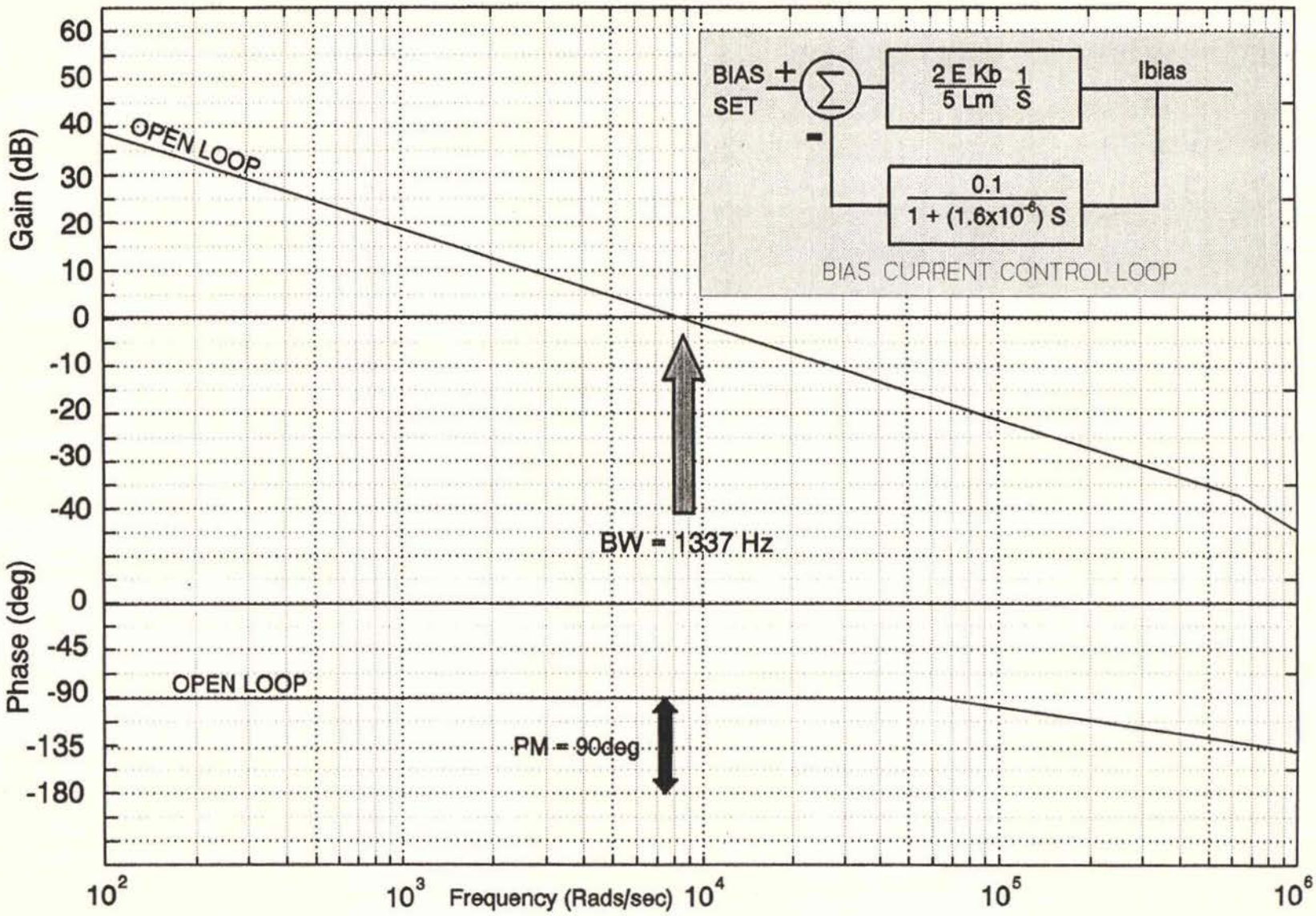


Figure 5.14 Bias Current Control Loop Open Bode Plot

The average rate of rise of ripple voltage will be given by:

$$\frac{dV_r}{dt} = \frac{2\ V_{p\text{-}p}}{T_s} = \frac{2 \times 0.227}{20} = 22.7\ mV/\mu S$$

The dV/dt for the ramps is $1V/\mu S$, so the ripple rate is more than an order of magnitude less than the ramp rate. An order of magnitude is considered necessary to ensure that the modulator behaves as a "classical" gain block. The value of K_b could be increased by four times without any effect on the stability of the loop in relation to the switching ripple or the phase margin.

As previously pointed out the unwanted 50kHz output current spectral component will become a problem at higher modulating frequencies. As will be shown in Chapter Six, where the scale model test results are presented, the 50 kHz component is acceptably low for the parameter settings used in the above analysis. Since from all other aspects these parameters are acceptable they will be adopted in the full power unit. The only difference is that because of practical constraints the value of L_m will be $325\mu H$ rather than $400\mu H$, this however from a control systems aspect will have negligible effect.

The main control loop has three sections in its forward path transfer function, the P+I controller, the modulator/buck converter and the load. The load represents a variable quantity and as a result the control system performance will also vary. The relative and absolute stability of the system is dictated by the closed loop pole/zero positioning in the complex plane. The forward path transfer function is given by:

$$G(s) = K_p \times \frac{s + K_i}{s} \times \frac{2}{5} E \times \frac{a}{s + a} \times \frac{1}{R} \qquad 5.5\text{–}39$$

$$a = \frac{R}{L}$$

L – Total load inductance; R – Load resistance

The feedback path transfer function is given by:

$$H(s) = \frac{1}{20\,s + b}\,\frac{b}{} \qquad 5.5\text{–}40$$

$$b = 6.25\times10^5$$

The closed loop transfer function will be given by:

$$\frac{C(s)}{R(s)} = \frac{G(s)}{1 + G(s)H(s)} \qquad 5.5\text{–}41$$

It is proposed to use the following parameter settings:

$$K_p = 10,\ K_i = 1\times10^4$$

The analysis will be done assuming that E is 280 V. The closed loop transfer function from equations 5.5–39,5.5–40 and 5.5–41 can be shown to be:

$$\frac{C(s)}{R(s)} = \frac{40E\,K_p a\,(s + K_i)\,(s + b)}{100R\,s^3 + 100R(a+b)\,s^2 + (100Rab + 2E\,K_p b)\,s + 2E\,K_p K_i ab}$$

Using the parameter settings above and a range of loads the pole/zero positions were calculated using "MATLAB", [33], and are displayed on the complex plane in Figures 5.15 and 5.16. The system is dominated by a complex pair of poles and a real zero at 6.25×10^5 rads/sec. The zero originates from the open loop feedback pole. There is also a pole zero pair at around 1×10^4 rads/sec but because these are relatively close for the load range considered they only have a small effect on the response. The behavior of the pole/zero pair with load changes is presented in Figure 5.16.

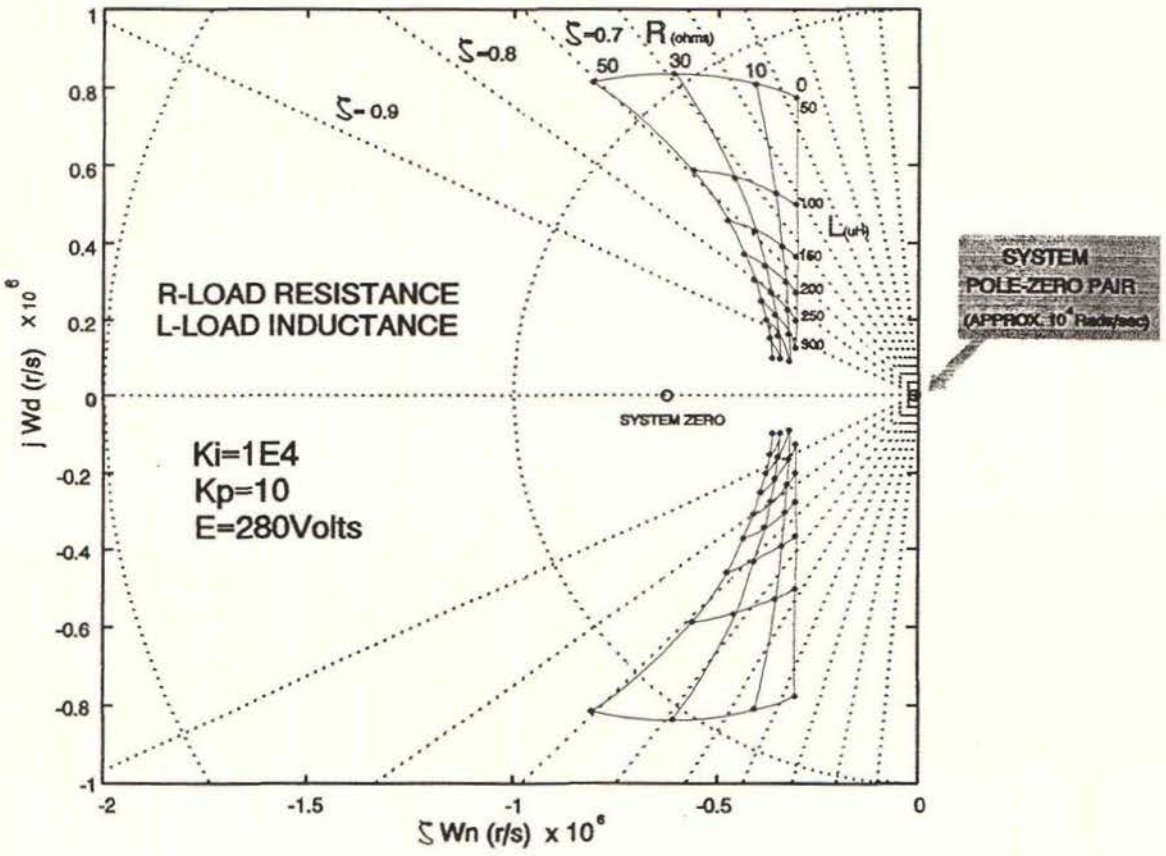


Figure 5.15 Output Current Control Loop Pole/Zero Map, Part "A"

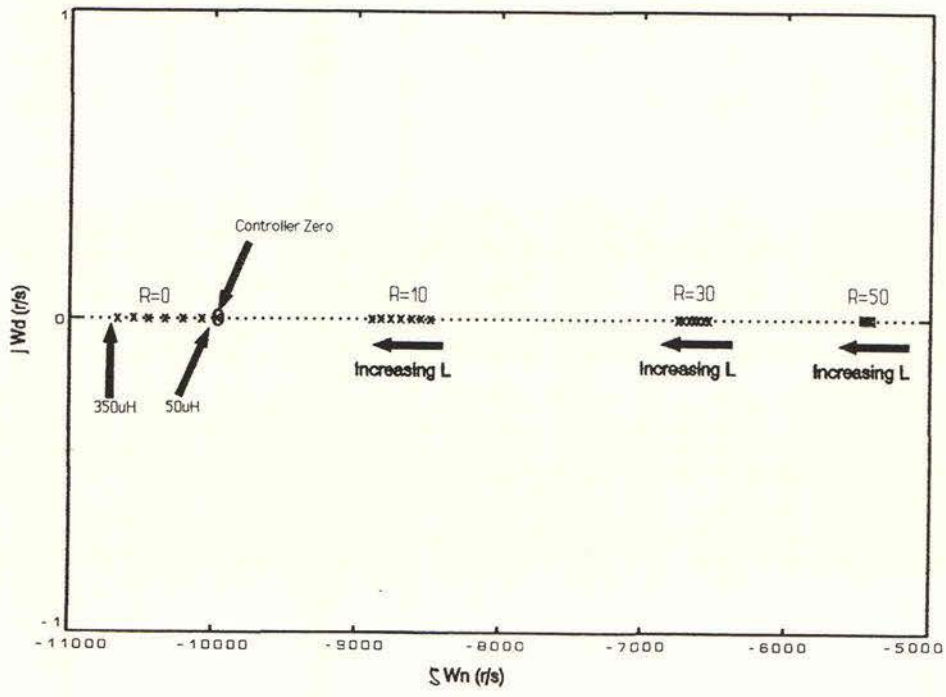


Figure 5.16 Output Current Control Loop Pole/Zero Map , Part "B"

The closed loop zero at 1×10^4 rads/sec originates from the P+I controller and the pole changes position as the load changes. The resistance set to zero ohms is as would be expected the worst case condition from a stability aspect. This corresponds to an output short circuit. The choice of the output inductor dictates the load inductance and hence the relative stability in the short circuit case. The output inductor has been selected to be 250μH which yields a second order system damping ratio of 0.83. The step input overshoot can be calculated for the second order system plus a zero. Curves for such systems are presented in, [45]. The ratio of the zero to the real part of the complex pair is two and for a damping ratio of 0.83 the step input overshoot will be approximately 1.5%.

As previously mentioned this neglects the effect of the closed loop pole/zero pair at 1×10^4 rads/sec. Under short circuit conditions the effect of the pole zero pair should be considered. At R=0Ω and L=250μH the pole frequency is 10480 rads/sec. The time domain unit step input response of the pole/zero pair can be shown to be given by the following, [46]:

$$Y(t) = 1 + (\frac{P}{Z} - 1)\, e^{-pt} \qquad 5.5\text{–}43$$

For P=10480 and Z=10000 the initial value will be:

$$Y(0) = 1 + (\frac{10480}{10000} - 1) = 1.048$$

The output is lifted 4.8% and the decay time constant (1/p) will be 95μS. Compared with the complex pairs time constant of 3.25μS this is very long. The complex pair plus zero and the pole/zero pair can be considered as two cascaded blocks. It can be seen that if a unit step is applied to the pole/zero pair the initial output will step to 1.048 which will decay with a time constant of 95μS back to unity.

Because the time constant of the complex pair is short compared with this the peak overshoot will be lifted by 1.048 times. The resulting peak will therefore be:

$$O.S. \approx 1.048 \times 1.015 = 1.064 \text{ or } 6.4\%$$

This was verified using "MATLAB" to simulate the output response from the system described by equation 5.5–42 for the load of R=0Ω; L=250μH for a unit step input. Loads of R=5Ω; L=250μH and R=5Ω; L=500μH were also simulated and are presented in Figure 5.17. The effect of the low frequency pole/zero pair is clearly evident from the long time constant characteristic response. For the case of R=5; L=250μH because the pole is lower in frequency than the zero the output step undershoots the demand.

From the pole zero map it can also be seen that the system response for purely resistive loads in the expected operating range (0Ω–30Ω) is relatively constant. With increasing load inductance the system becomes more damped as the complex pair of poles migrate towards the real axis. At higher load inductances the system becomes overdamped. The open loop bode plots are presented in Figure 5.18 for loads, R=0Ω, L=250μH; R=0Ω, L=500μH; R=5Ω, L=250μH; R=5Ω, L=500μH. In all cases the phase margin is better than 70° which for a second order dominated system would be equivalent to a damping ratio of approximately 0.7. For the R=5Ω and L=500μH load the bandwidth is 1.2×10^5 rads/sec or 17.5 kHz. This bandwidth is sufficient to give reasonable performance at the maximum modulation frequency of 10 kHz. In fact at 10kHz a greater restriction on the large signal performance is the available voltage for raising the output inductor current. This limits the amplitude that can be reproduced without a slew rate limiting effect occurring.

Lastly the assumption that the modulator functions as a linear amplifier must be checked.

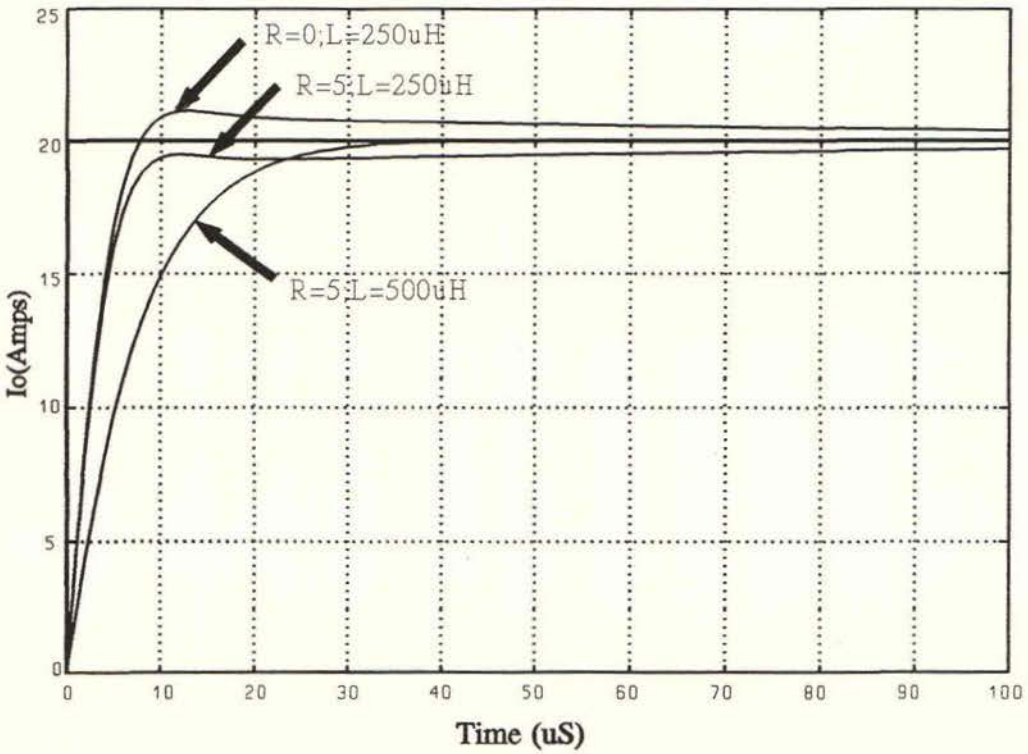


Figure 5.17 Output Current Control Loop Step Response

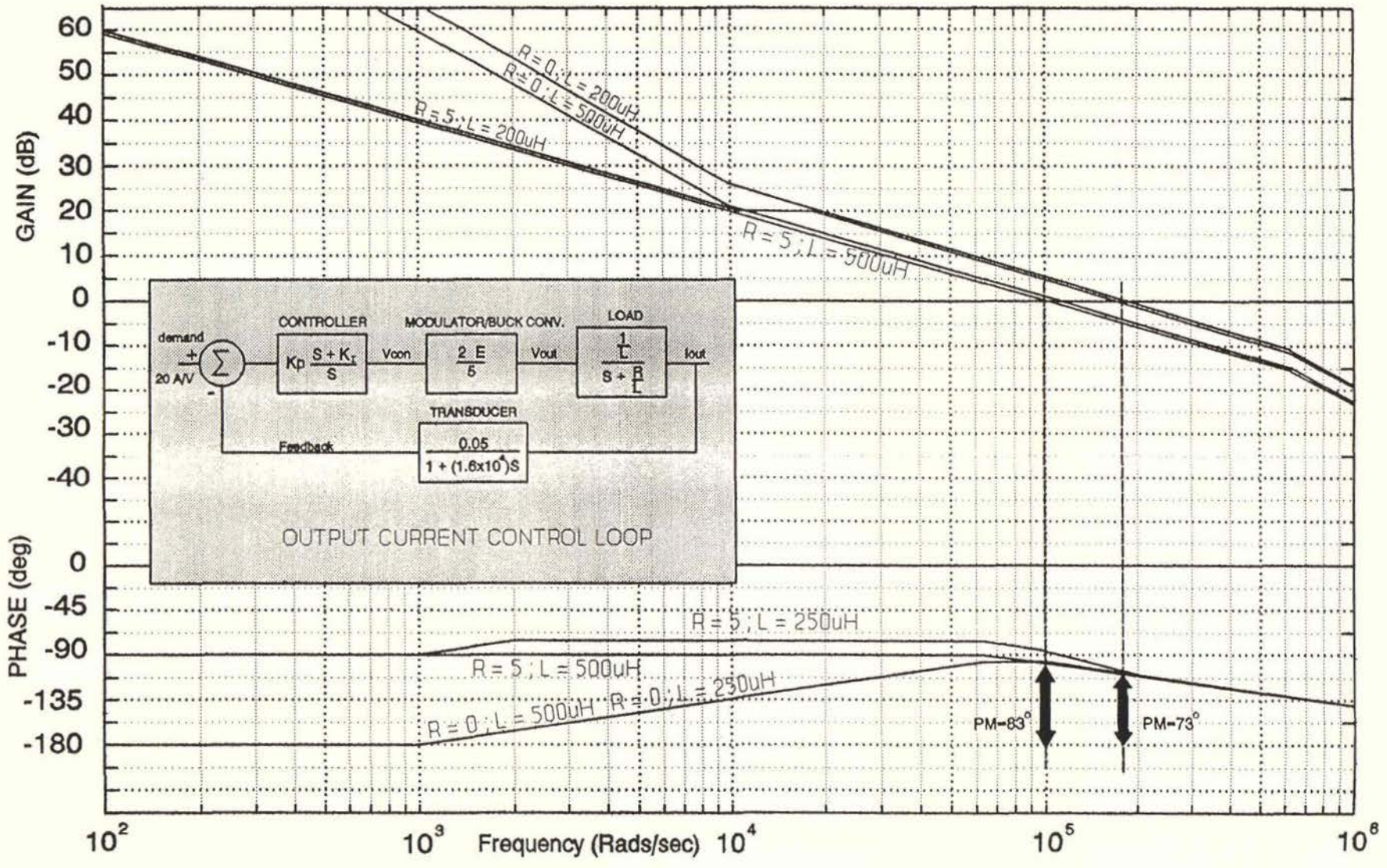


Figure 5.18 Output Current Control Open Loop Bode Plots for Three Typical Loads

From Chapter Two the maximum ripple for the five level modulation scheme was found to be(equation 2.2–3):

$$\Delta I = \frac{E}{16Lf_s}$$

This assumes that the ripple voltage across the resistance is low. This is guaranteed if a capacitor of sufficient size is placed across it. However if the inductance is sufficiently large to make the ripple current low the equation is still valid without the necessity for the capacitor. The output inductor chosen is 250μH and for E=280V the peak to peak ripple will be:

$$\Delta I = \frac{E}{16Lf_s} = \frac{280}{16 \times 250\times10^{-6} \times 50000} = 1.4\ A_{p\text{-}p}$$

This ripple signal is at a frequency 200kHz. The objective is to calculate the ripple signal level at the modulator input. More specifically the rate of rise of the ripple signal should significantly less than the ramp slope (> 10 times will be used) to ensure chatter free linear operation, [1]. The 200kHz (1.25×10^6rads/sec) ripple signal is first attenuated by the transducer since its bandwidth is 100kHz:

$$G(\omega j)_{trans} = \frac{0.05}{1 + 1.6\times10^{-6}\omega j}$$

$$|G(1.25\times10^6)| = 0.05\times\frac{1}{\sqrt{1 + (1.6\times10^{-6} \times 1.25\times10^6)^2}} = 0.0224$$

This ripple signal is passed to the controller. The P+I controllers gain at this frequency is essentially given by the proportional component ($K_p = 10$) since the integral sections attenuation is very high.

The ripple signal at the input to the modulator will therefore be:

$$\Delta V = 10 \times 0.0224 \times 1.4 = 0.314 \ V_{p\text{-}p}$$

The average dV/dt would be given by:

$$\frac{dV}{dt} = \frac{0.314}{2.5} = 125 mV/\mu S$$

The ramp slope is $1V/\mu S$ and so therefore the ripple slope is eight times less than the ramp slope. No chatter problems are encountered on the scale model. It must be remembered that the peak ripple was used for the calculation and that the average is 63.7% of this.

6. SIMULATION AND SCALE MODEL TEST RESULTS

With large converters it is not advisable to carry out debugging using the full power unit with untested control circuitry. The only practical approach is to divide the task into manageable steps. In this project the overall control and converter topology was proven by simulation. A controller design was directly based on the simulation model. This controller was constructed and debugged using a tenth scale power circuit. A prototype buck converter was designed constructed and tested with any necessary modifications being carried out. The final step is to implement the tested controller with the proven set of buck converters to form the final amplifier.

This chapter is devoted to the presentation and discussion of the simulation model and the tenth scale model results. Although the construction of the amplifier is not yet complete the presented results are thought to be representative of the final unit.

Particular attention is drawn to the accuracy which the simulation model predicts the performance of the tenth scale model.

6.1 Simulation Technique

The entire amplifier was modeled in the control systems simulation package "TUTSIM". This package is very useful for this application since it combines standard logic as well as analog functions. The block diagrams of Figure 5.5 A and B were essentially duplicated in the "TUTSIM" model. All the major signals that are available in the controller hardware are also available in the simulation. Using this approach major control system problems could be resolved before any hardware was designed and built.

This saved expensive hardware redesign which more than likely would be necessary in this complex system.

The power circuit was modeled at a systems level. For example the buck converters are modeled using relays that produce the two voltage levels. Special logic is used to mimic the unipolar current behavior and therefore discontinuous conduction. The power circuit is only modeled such that it behaves accurately from the control systems point of view. There is no attempt to model the power circuit devices accurately since this would add little if anything to the validity of the control systems model. The entire model is very large, approximately 400 "TUTSIM" blocks, and is beyond the scope of this report. However the analog control section and the power converter section are presented since they are relevant to the results which are presented and serve to demonstrate the general techniques involved.

Shown in Figure 6.1 is a drawing of the power circuit "TUTSIM" model. For an explanation of the blocks the "TUTSIM" Control Systems Simulation Manual should be consulted, [18]. The bridge is modeled by four relays supplying $\pm$ 280V on command from a logic signal. Each relay represents the output voltage from a converter. The outputs from the "AP" and "AN" converters are subtracted and passed through an integrator, (Block 281). This represents the differential voltage being applied across the coupling transformers magnetising inductance. The output of block 281 is the magnetising current I_{ma}. The outputs of the "AP" and "AN" converters are also added and divided by two (Block 285), to produce the voltage at the coupling transformer center tap V_a. The same applies to the "B" leg which has an output voltage of V_b and a magnetising current of I_{mb}. The voltages V_a and V_b are subtracted (Block 286),to produce the voltage V_{out} which appears across the R–L load (Block 288). The output of block 288 is the load current which is measured by a transducer (Block 290). The output current is also divided by two and summed and subtracted from the I_{ma} to produce I_{ap} and I_{an} respectively (Blocks 317 and 277).

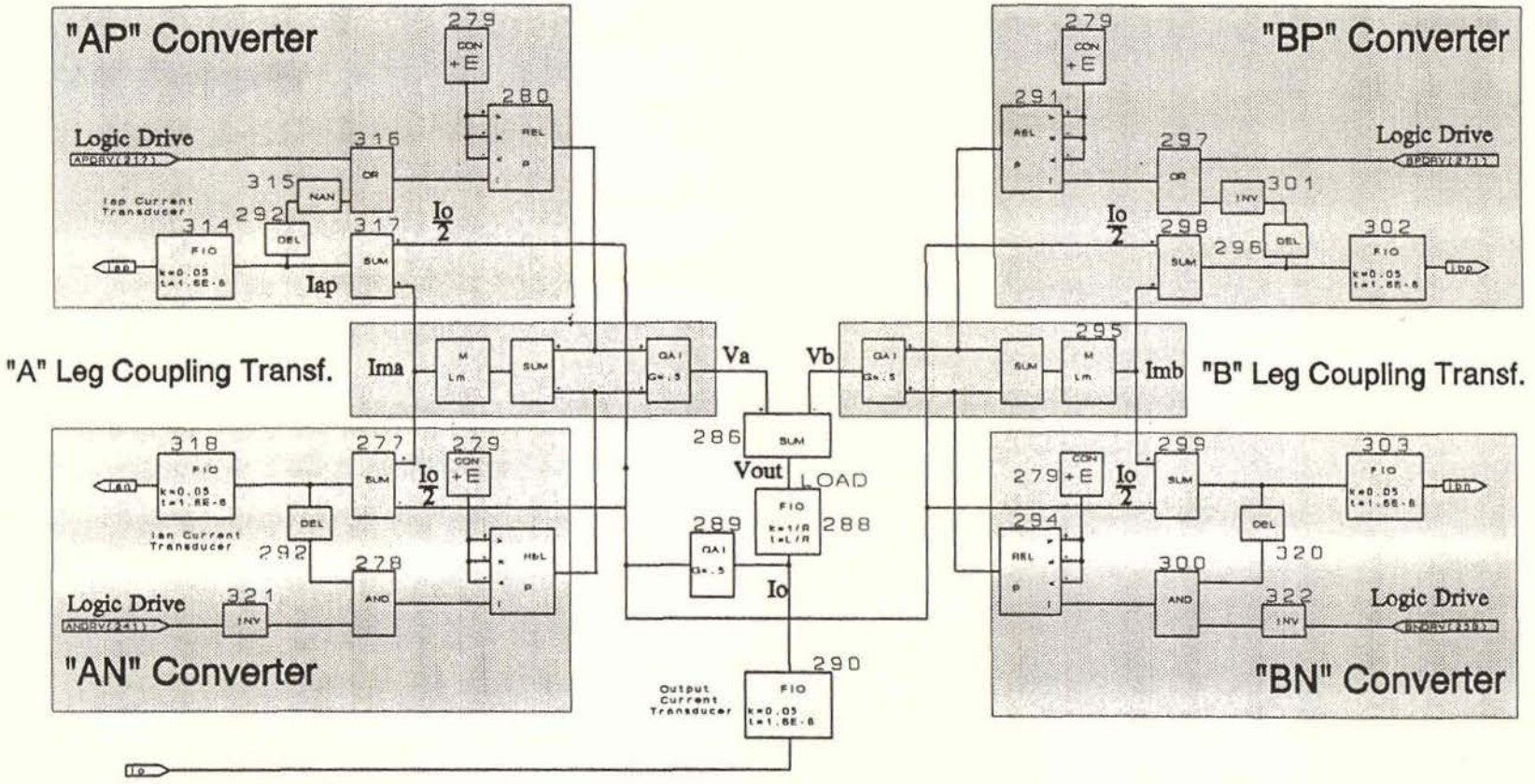


Figure 6.1 "TUTSIM" Model of the Bridge Inverter

The same occurs in the "B" leg (Blocks 298 and 299). Four transducers feedback the four converter currents (Blocks 314, 318, 302 and 303). In reference to the "AP" converter I_{ap} is monitored by a comparator in the form of an NAND gate (Block 315). Once the current reaches zero a logic "1" is supplied to the relay control input by the OR function, (Block 316). This forces the "AP" converter output voltage to +280V. This mimics the behavior of the real converter in that if the current were to reverse it would flow by the IGBT's inverse diode to the positive rail. The power circuit model gives access to the major switching waveforms plus the four converter currents and the output current.

Figure 6.2 shows a block diagram of the analog control section of the controller. This is essentially based on Figure 5.4, the operation of which has previously been explained. Again all the analog signals are available for observation as they would be in the hardware implementation.

6.2 Small Scale Model and Simulation Results

A one tenth scale model (1/10th bus voltage; 1/10th output current) of the power circuit was constructed to test the controller operation. This was essential since it would be impractical if not dangerous to try and debug the controller using the full power amplifier. The switching devices used, were power mosfets gated by pulse transformer coupled drivers. In order to rescale the feedback levels the hall effect current transducers had their gain lifted by ten times by placing ten turns through their magnetic window rather than one. Other than this the power circuit is the same as presented in Figure 5.2.

The major power circuit waveforms and amplifier performance results predicted by simulation and those obtained with the scale model are now compared.

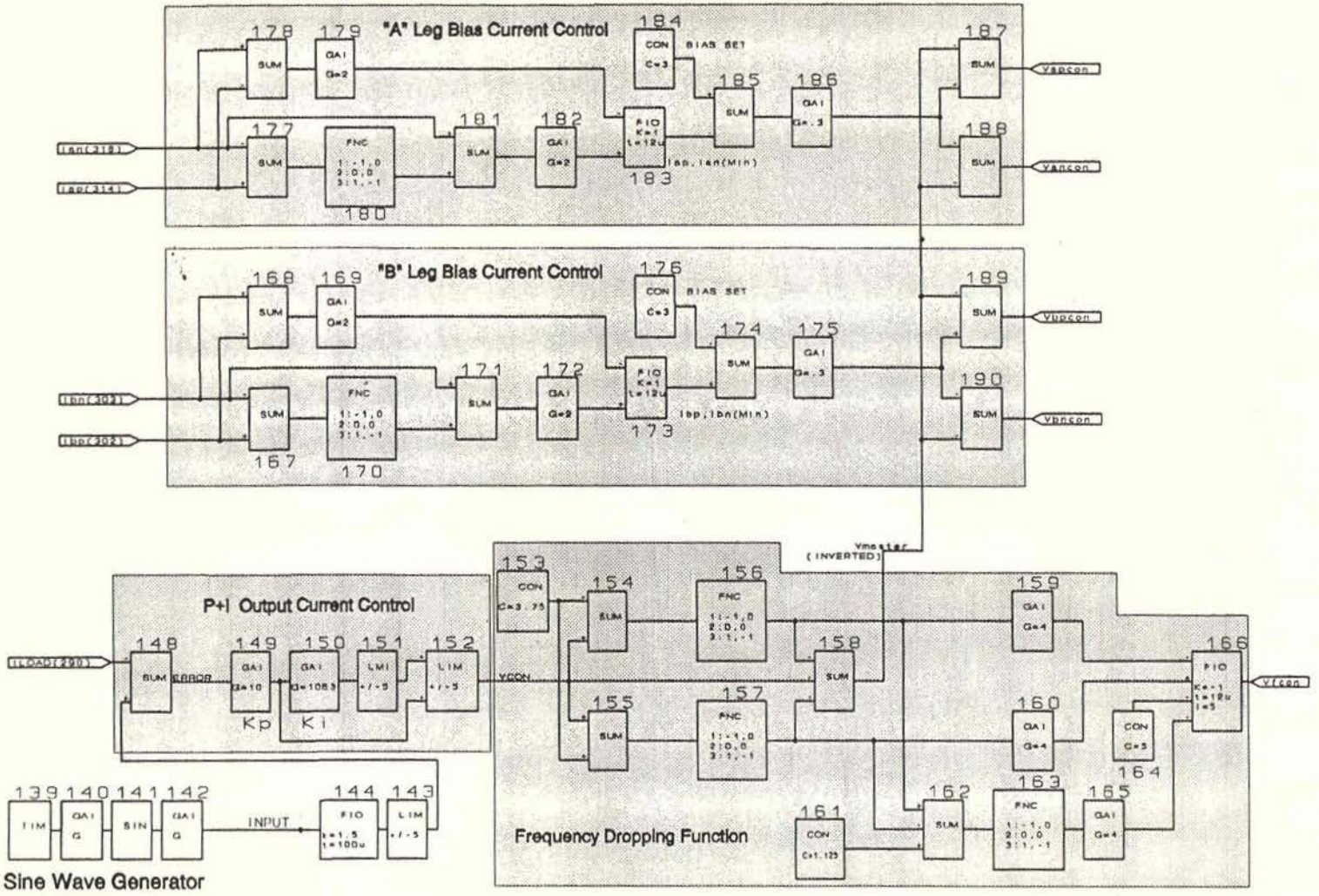


Figure 6.2 "TUTSIM" Model of the Analog Control Section

Figure 6.3 (A) shows the simulated and the scale model output voltage for a 10kHz modulating frequency. The integrity of the five level modulation in both the simulation and the scale model compare well with the open loop ideal simulation presented in Figure 2.10. This means that for the parameter settings used the non–ideal aspects of the practical implementation do not seriously impair the performance. This is enforced by Table 6.1 which shows the output voltage frequency components found in the tenth scale model output. As with the ideal open loop simulation the spectrum consists of sideband components spaced at increments of the modulation frequency around a 200kHz suppressed carrier. Most of the spectral content due to switching is above 150kHz and therefore is ordinarily attenuated strongly by the load transfer function, the output current therefore has only low levels of these components.

The spectral purity is demonstrated in the high quality of the output current waveshape. The scale model output current and the current produced by converter "AP" for 10kHz operation are shown in Figure 6.4. The spectrum presented in Table 6.1 shows a 50kHz component approximately 25dB below the fundamental. The load current was 1.4 A_{rms} through a 1+23jΩ at 10kHz load, therefore the RMS output voltage is 32.2 V_{rms}. The 50kHz component would therefore be 25dB down on this or 1.8 V_{rms}. This would be attenuated by the 1+23jΩ load by a further 23 times. The output current component at 50kHz will hence be 0.08 A_{rms}, which rides on top of the 1.4 A_{rms} modulating signal. As discussed in Chapters Two and Five the action of the bias current controller is mainly responsible for the production of the 50kHz component. The parameter settings used represent an acceptable compromise between the the 50 kHz level and the bias current control loop bandwidth.

Shown in Figure 6.5 parts (A) and (B) are the simulated and the scale model output current plus the "AP" converter current for an $8A_{peak}$ 1kHz modulation.

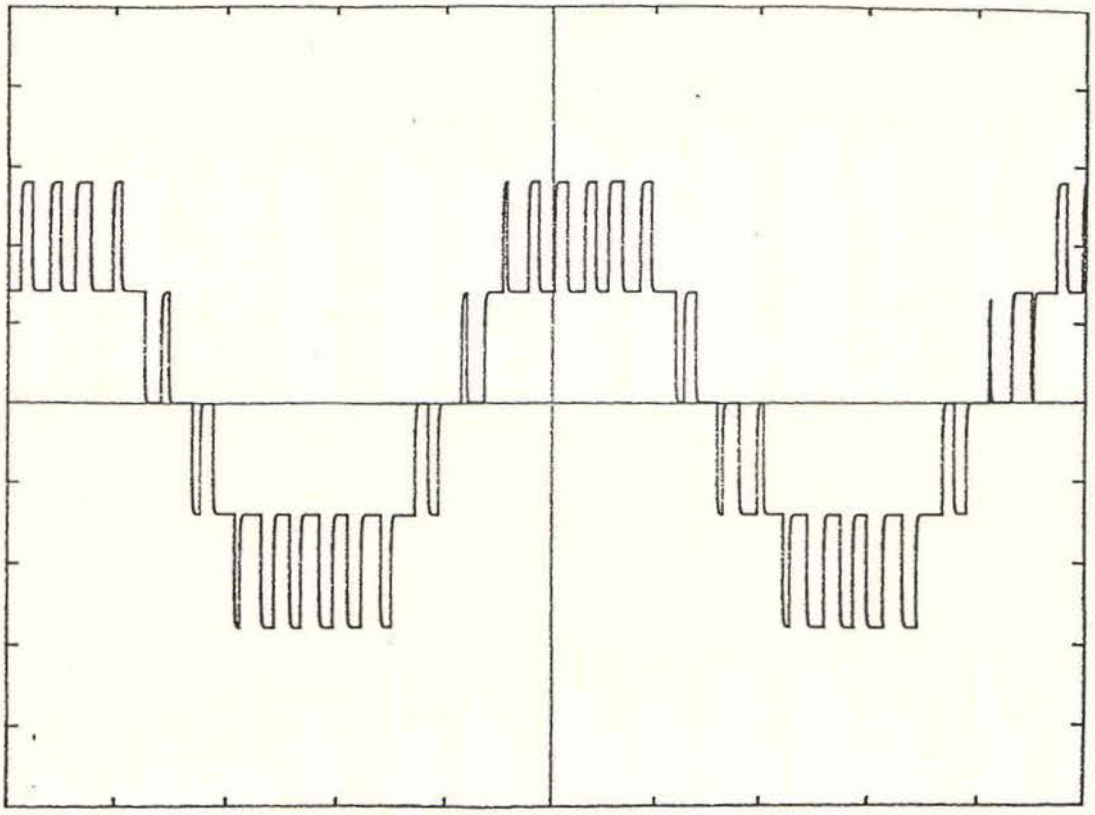


Figure 6.3(a) Simulated Output Voltage for 10kHz Modulation

Vertical Scale - 200V/div

Time Base - 20uS/div

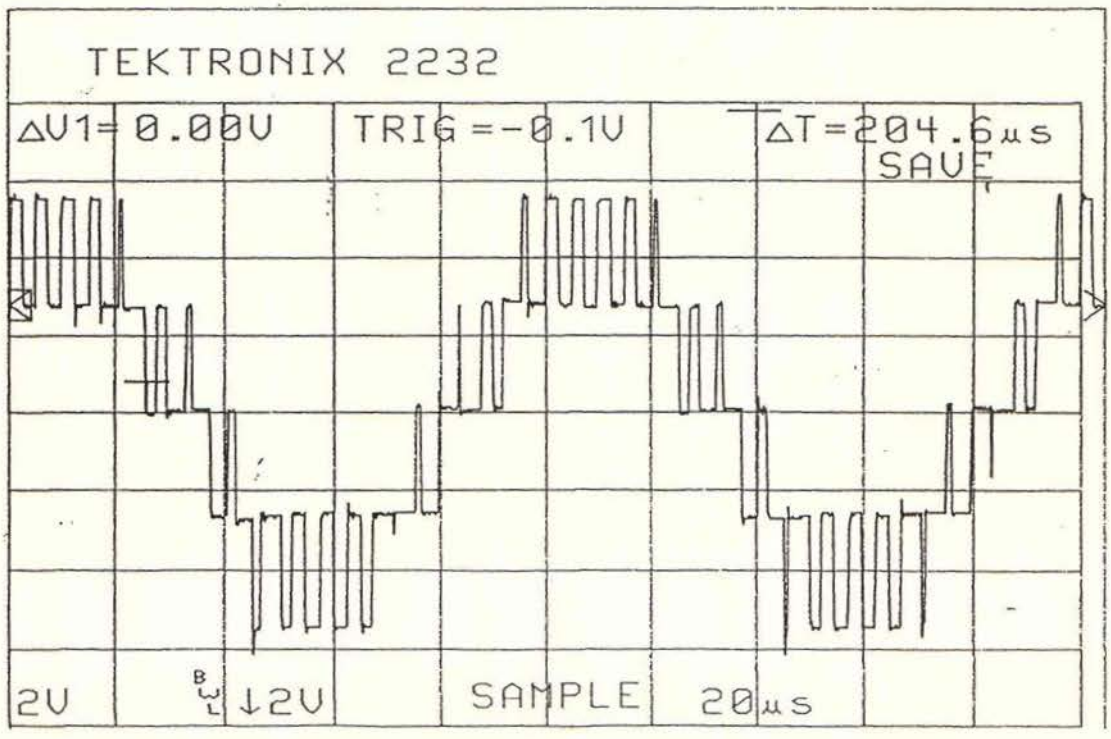


Figure 6.3(b) Scale Model Output Voltage for 10kHz Modulation

Vertical Scale - 200V/div

Time Base - 20uS/div

Frequency	Amplitude	dB
10kHz	32.2Vrms	0.0dB
50kHz	1.45Vrms	-27.0dB
75kHz	1.45Vrms	-27.0dB
100kHz	1.61Vrms	-26.0dB
150kHz	1.36Vrms	-27.5dB
170kHz	5.11Vrms	-16.0dB
190kHz	3.22Vrms	-20.0dB
200kHz	0.00Vrms	——
210kHz	2.55Vrms	-22.0dB
230kHz	4.83Vrms	-16.5dB
250kHz	1.45Vrms	-27.0dB

Table 6.1 Output Voltage Spectrum
Modulation - 10kHz
Output Current - 1.4Arms
Load - 1+23j ohms

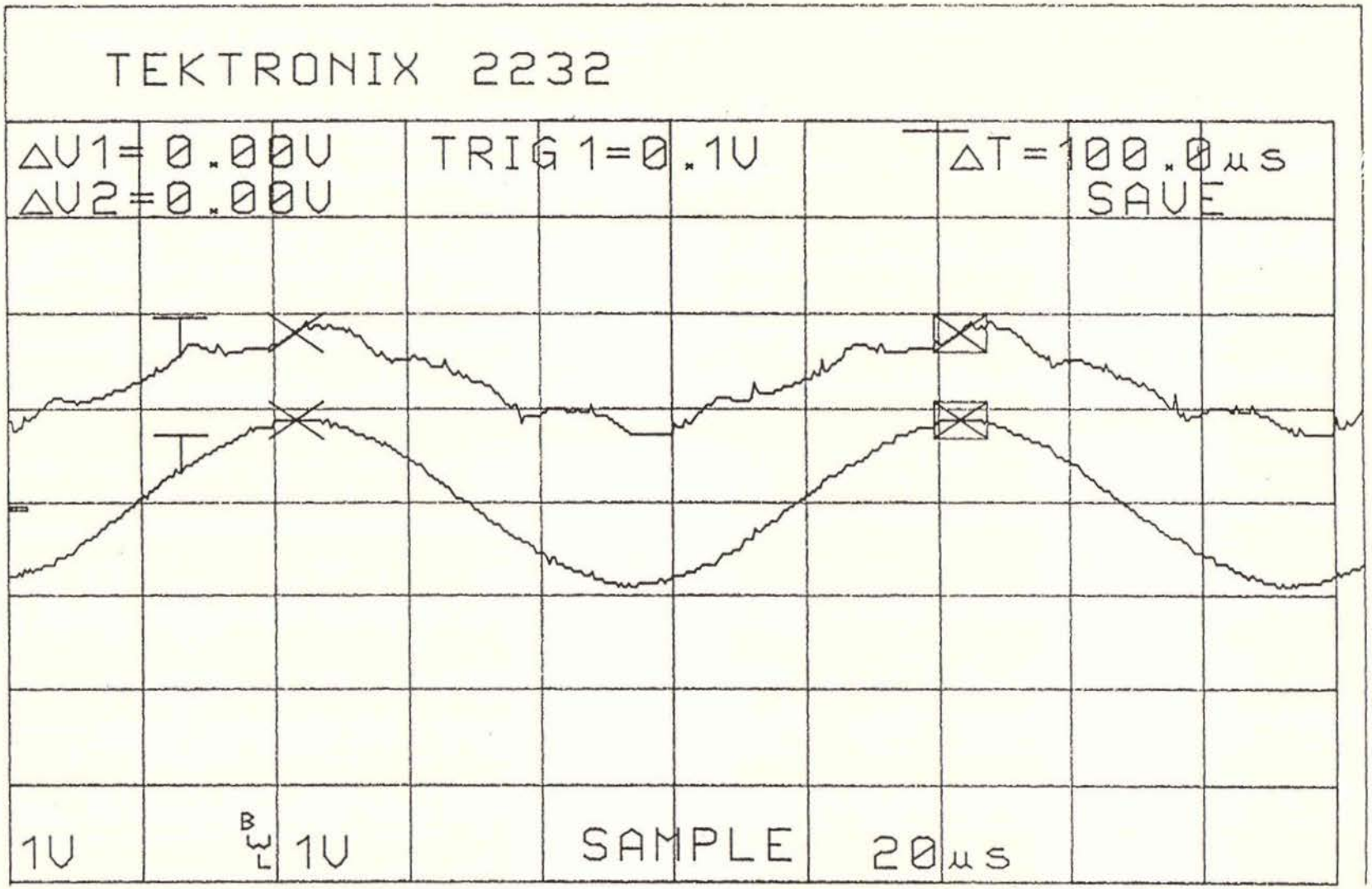


Figure 6.4 Scale Model Output Current for 10kHz Modulation

Top Trace - "AP" Buck Converter Current

Bottom Trace - Output Current

Vertical Scale - 2A/div

Time Base - 20uS/div

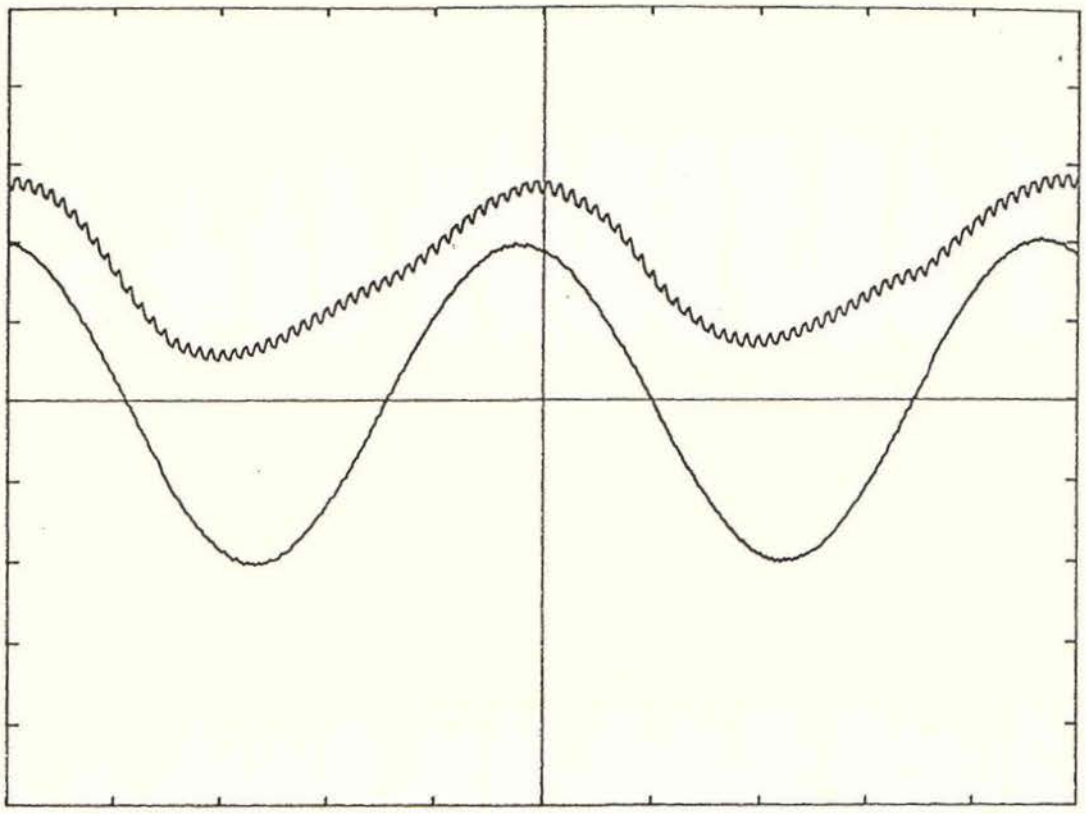


Figure 6.5(a) Simulated Operation; 1kHz, 56Arms, 1.5+2j load

Top Trace - Buck Converter Current

Bottom Trace - Output Current

Vertical Scale - 40A/div

Time Base - 0.2mS/div

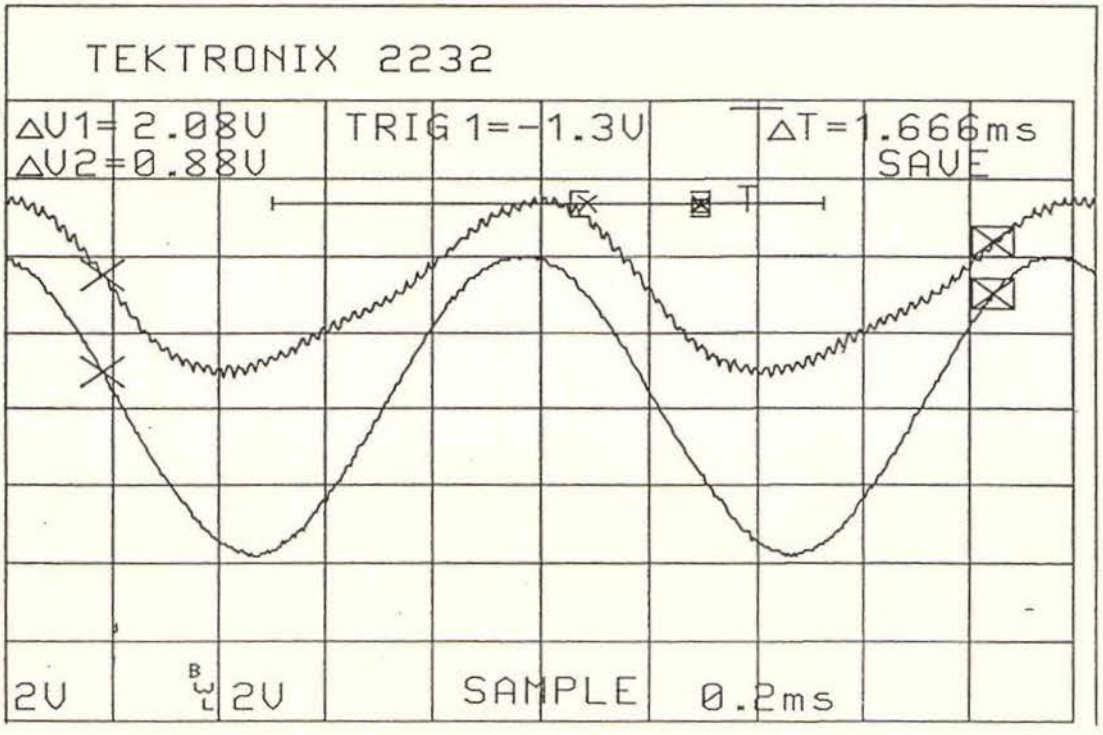


Figure 6.5(b) Scale Model Operation; 1kHz, 5.6Arms, 1.5+2j load

Top Trace - Buck Converter Current

Bottom Trace - Output Current

Vertical Scale - 4A/div

Time Base - 0.2mS/div

In this case the bias current setpoint was set such that the peak converter current is 11A which would correspond to 110A in the full scale unit. The minimum converter current is approximately 2.5A which would correspond to 25A in the full scale unit. This gives the scope to reduce the bias setpoint to bring the peak current down to 90A without discontinuous conduction occurring. The minimum current would then be approximately 5.9A as predicted by eq. 5.5–34. This would imply a setpoint current of 20A and therefore at low modulating frequencies the peak converter current would rise to 100A. The very modest 50 kHz ripple can be seen on top of the converter current, its $10A_{p\text{-}p}$ level, as calculated from eq. 2.4–4, being confirmed.

Figure 6.6 parts (A) and (B) show the output current and the "AP" converter output voltage for a 1kHz modulation as predicted by simulation and as obtained from the scale model. The load impedance has been raised to $3+3j\Omega$ so that the control system is forced into frequency dropping. The pulse stretching is clearly evident. As mentioned in Chapter Five the frequency is reduced to 5 kHz at the peak output voltage.

The closed loop frequency response measured using a Hewlett Packard Dynamic signal analyser is presented in Figure 6.7. The analyzer's periodic random noise source was injected into the amplifier input and the output current was measured at the output of the current transducer. For the load of $R=5\Omega$; $L=500\mu H$ the closed loop bandwidth was found to be approximately 20 kHz which is consistent with the calculations of Chapter Five.

Lastly the output current spectrum for a 1 kHz 7 Amp peak modulation signal was measured to gauge the linearity of the closed loop system. The harmonics up to 10 kHz are shown in Figure 6.8. The major harmonics are the 2nd,3rd and 7th harmonics. The Total Harmonic Distortion (THD) was measured as 0.34%. This is more than adequate for the application.

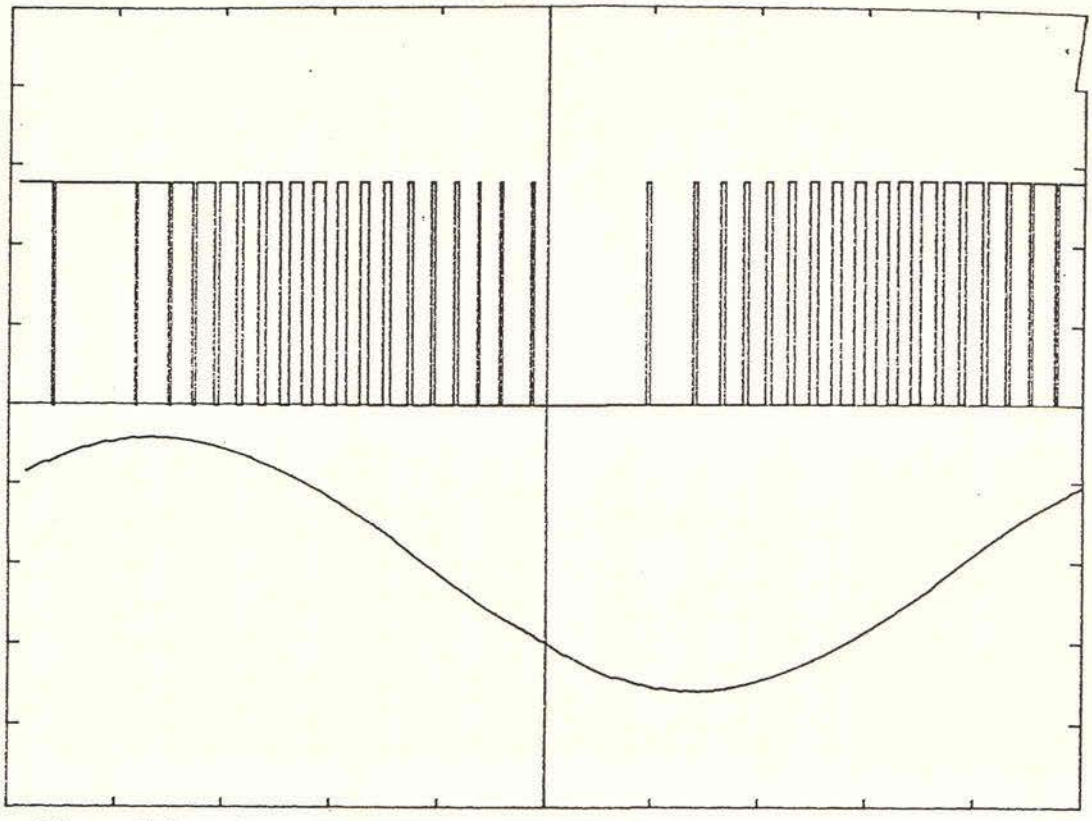


Figure 6.6(a) Simulated Frequency Dropping Mode; 1kHz, 40Arms, 3+3j load

Top Trace - Buck Converter Output Voltage 200V/div

Bottom Trace - Output Current (40A/div)

Time Base - 0.1mS/div

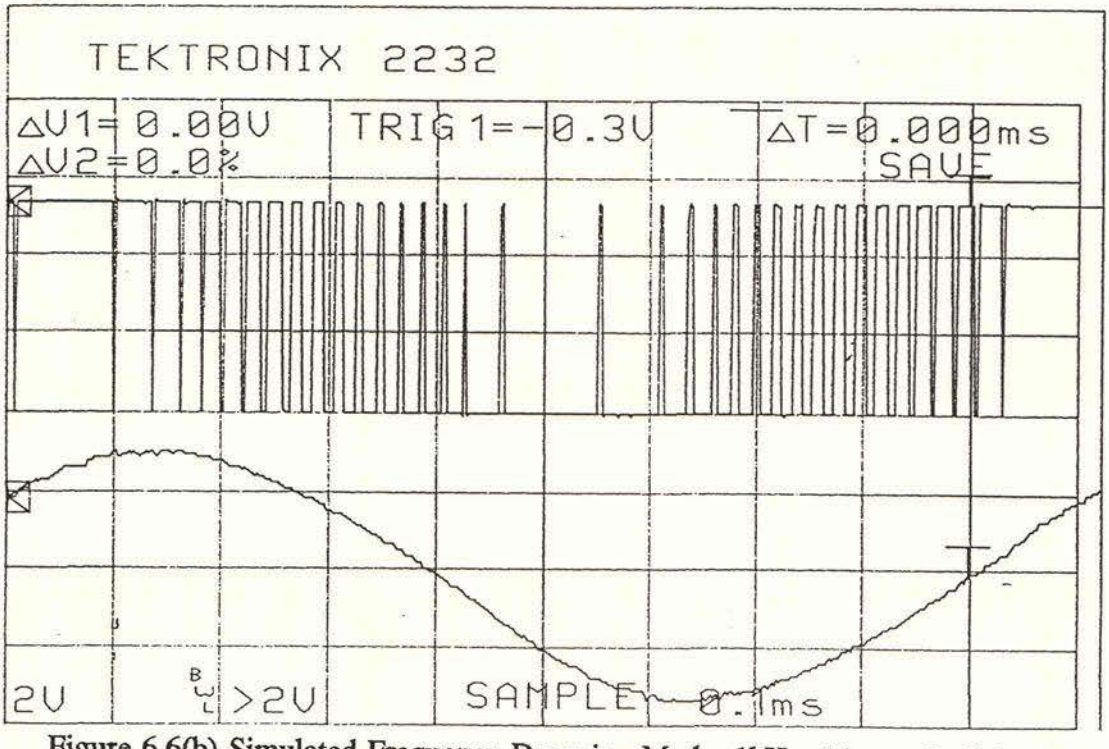


Figure 6.6(b) Simulated Frequency Dropping Mode; 1kHz, 4Arms, 3+3j load

Top Trace - Buck Converter Output Voltage (20 V/div)

Bottom Trace - Output Current (4A/div)

Time Base - 0.1mS/div

It is thought that the origin of the distortion is mainly from two sources:

(a) The modulator output pulsewidth jump during the change in the polarity signal "P" as already explained in Chapter Five.

(b) Slight non–linearity in the ramps due to the voltage dependant properties of the dielectric constant of the integration capacitors.

The simulation results adequately predicted the model responses. Great value was found from the simulation in the design of and evaluating the performance of the control system before any hardware was designed and constructed. This meant there was minimal requirement for hardware changes. The tenth scale model is a necessary intermediate step to provide a test bed for the controller, rather than trying to commission it on the final unit. The tenth scale model confirmed the theoretical calculations and the simulation results.

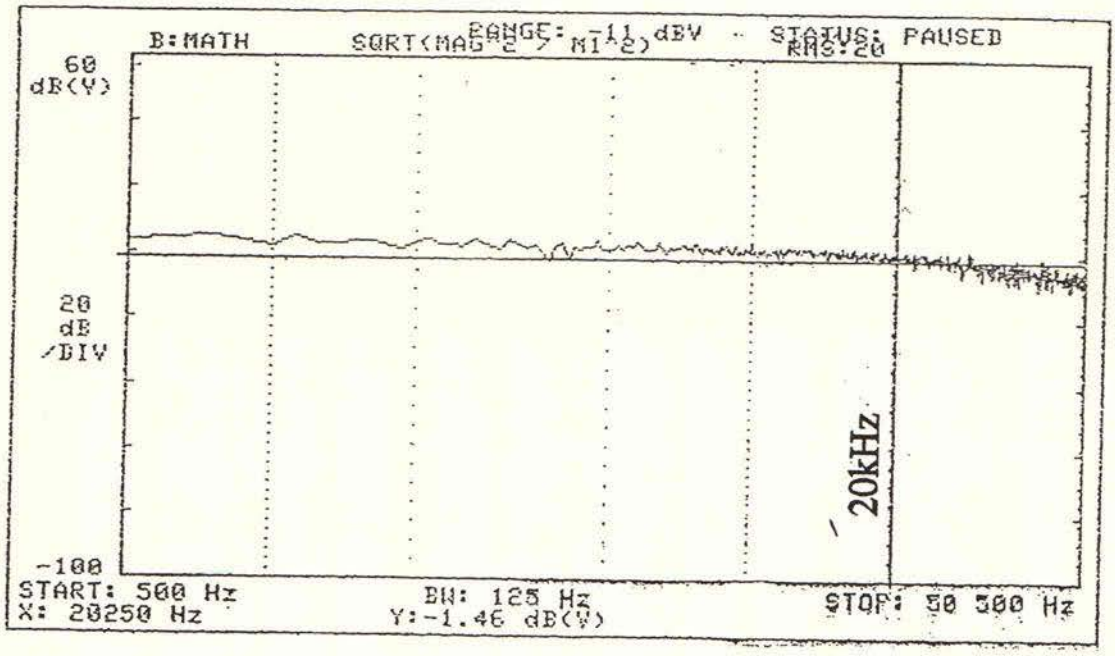


Figure 6.7 Scale Model Closed Loop Response; 5ohm, 500uH Load

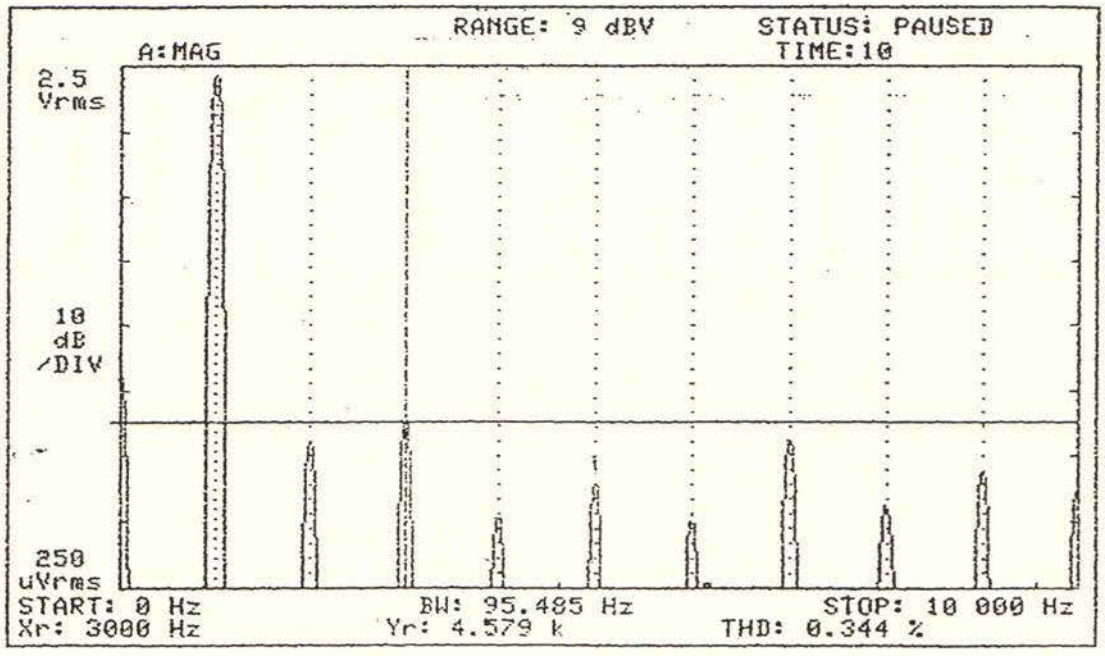


Figure 6.8 Scale Model Output current Spectrum; 1kHz, 5Arms, 3+3j load

7. CONCLUSIONS

A new five level inverter topology suitable for switching amplifier application has been developed. The topology requires just four power switches as compared to previous systems which use eight devices. The new converter consists of four independent buck converters coupled by transformers. Five level modulation allows extension of the amplifiers bandwidth and improvement in the output quality without increase in the switch frequency. In a tenth scale model and computer simulations a bandwidth of 20kHz was easily achieved.

Each buck converter consists of a Insulated Gate Bipolar Transistor with associated snubbing/clamping system and freewheel diode. The converter is capable of supplying 100A maximum from a 560V nominal bus. The innovative regenerative snubbing/clamping system allows the buck conveter to switch at 50kHz with a loss of only 741watts at rated load and 50% duty ratio. The negative buck converter cell has been thoroughly tested to a load of 75A, 50% duty ratio. Loading beyond this has not been carried out due to the lack of availability of loading banks. However the results obtained at 75A indicate that thermally the converter will carry the 100A rated load. Semiconductor voltage stress levels were also shown to be well within device ratings at the 75A load. These would also not be expected to be violated at the 100A load.

A thorough understanding of semiconductor device characteristics is essential to successful converter design at high powers and high switch frequencies. A major contribution of this thesis has been the development of methods of predicting diode reverse recovery behaviour from limited manufacturer's data. This was necessary to accurately determine diode switching loss which is very significant at the 50kHz switching frequency.

Failure to address diode switching loss in high frequency, high power converters often results in unworkable designs. A detailed procedure has been developed to predict power diode reverse recovery performance under any operating condition. It is believed that this procedure will be an important design aid for power electronic engineers.

Specialised control techniques applicable to the new topology have been developed and proven. These include a four phase modulation system which uses frequency dropping to obtain extended dynamic range beyond the normal pulse dropping or saturation range and a leg bias current control system. The leg bias system controls the current flowing in the coupling transformer. This bias current is necessary to maintain conduction in all buck converters and hence the five level modulation capability. Expressions have been established which allow the setting of bias current control parameters. The combined topology and control system effectively eliminates the possibility of a leg shoot through fault which often occurs in conventional bridge inverters.

Extensive use of computer simulation tools was made during the buck converter and control system design process. In addition to this a tenth scale model was constructed to prove the control system hardware and the topology converter topology operation. This allowed debugging and performance tuning to be conducted in stages prior to implementation of the final amplifier. This approach though time consuming is considered essential in high power converter designs. As a result of this technique the amount of redesign and modifications required to either the control hardware or the buck converter has been minimal. The tenth scale model results and the corresponding computer simulation results are both presented. In every case the the hardware model performs almost identically to the computer model.

Although the final full power amplifier is not yet completely constructed it is expected that commissioning will be straight forward. The detailed design verification approach used throughout this project allows this statement to be made with confidence.

Additionally the design is very decoupled in its nature. Each buck converter works semi–independently. Their operation is not greatly changed when they form part of the amplifier converter. The individual buck converter operation has been proven and therefore should perform equally well in the complete inverter. The control system and topology implementation have been shown to be viable by both simulation and a tenth scale model. Debugging and tuning of the control hardware has been done and only minor adjustments if any will be necessary on the final unit.

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APPENDIX A

Self Oscillating Inverter Spice Model Listing

```
R1 1 2 68
VZ1 7 2 12v
VZ2 8 0 12v
D1 0 7 DFR104
D2 2 8 DFR104
VZ3 9 5 12v
VZ4 10 0 12v
D3 0 9 DFR104
D4 5 10 DFR104
R2 3 0 15
R3 4 0 15
R4 6 5 68
L6 2 3 10
L7 4 5 10
Kf L6 L7 .99999 KRM7_N30
R5 3 11 56
R6 4 12 56
D5 0 11 DFR104
D6 0 12 DFR104
D100 11 15 DFR104
D101 12 16 DFR104
Q1 15 11 13 QBC639
Q2 15 13 0 QBC639
R7 11 13 10K
R8 13 0 100
Q3 16 12 14 QBC639
Q4 16 14 0 QBC639
R9 12 14 10K
R10 14 0 100
R11 1 15 470
R12 16 6 470
R13 1 17 68
C1 17 15 .022uf
R14 6 22 68
C2 22 16 0.022uf
D7 0 15 DFR104
D8 15 18 DFR104
R17 18 19 5
VZ5 19 0 12v
D9 0 16 DFR104
VZ6 20 0 12v
R18 20 21 5
D10 16 21 DFR104
R15 15 23 15
R16 16 24 15
M1 25 23 0 0 MIRF451
M2 26 24 0 0 MIRF451
D11 25 27 DBY329
D12 26 27 DBY329
R19 27 28 56
VZ7 28 0 312v
C3 35 0 5uf IC=130v
L1 32 35 35
L2 35 34 35
Lc 25 31 0.05uH
Ra 31 32 0.1
Ld 26 33 0.05uH
Rb 33 34 0.1
```

```
L4 29 0 5
L5 0 30 5
Kx L1 L2 L3 L4 L5 .99999 KEC70_N27
La 6 29 .1uH
Lb 1 30 .1uH
L3 36 37 75
Rc 36 38 0.3
Le 38 39 .5uH
R20 39 40 33
C4 40 37 .001uf
D13 0 39 DBY329
D14 0 37 DBY329
D15 39 41 DBY329
D16 37 41 DBY329
R21 35 15 12K
VL 41 0 280v
Is 0 100 PULSE(0 100A .1u .1u 1.5u .01u 20u)
Cx 100 0 10uf IC=130v
Rd 100 35 3.3
Lx 100 35 50uH
*
.OPTIONS VNTOL=1mV ABSTOL=1mA CHGTOL=.1pC ITL4=100 RELTOL=.01 ITL5=1
*
.MODEL DBY329 D(Is=.1mA N=2 RS=6m CJO=100pF VJ=.7 M=.3 FC=.1 TT=.02u
+           BV=1000V IBV=1mA EG=1.11 XTI=3.0)
*
.MODEL KEC70_N27 CORE(MS=500E+3 ALPHA=2E-5 A=26 K=18 C=1.05
+                AREA=2.79 PATH=14.4 GAP=.008)
*
.MODEL KRM7_N30 CORE(MS=250E+3 ALPHA=.5E-5 A=20 K=30 C=1.5
+                AREA=.4 PATH=2.98)
*
.model MIRF451 NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vm
+    Tox=100n Uo=600 Phi=.6 Rs=32.16m Kp=20.69u W=2.1 L=2u
+    Vto=3.415 Rd=.2606 Rds=1.44MEG Cbd=1.732n Pb=.8 Mj=.5 Fc=.5
+    Cgso=4.12n Cgdo=56.28p Rg=4.086 Is=1E-30)
*
.MODEL DFR104 D(IS=100E-15 RS=.16 CJO=2PF TT=12NS BV=100 IBV=100E-15
*
.model QBC640 PNP(Is=9.913f Xti=3 Eg=1.11 Vaf=90.7 Bf=197.8 Ne=2.264
+          Ise=6.191p Ikf=.7322 Xtb=1.5 Br=3.369 Nc=2 Isc=0 Ikr=0 Rc
+          Cjc=14.57p Vjc=.75 Mjc=.3333 Fc=.5 Cje=20.16p Vje=.75
+          Mje=.3333 Tr=29.17n Tf=405.6p Itf=.4 Vtf=10 Xtf=2)
*
.model QBC639  NPN(Is=3.108f Xti=3 Eg=1.11 Vaf=131.5 Bf=217.5 Ne=1.5
+          Ise=190.7f Ikf=1.296 Xtb=1.5 Br=6.18 Nc=2 Isc=0 Ikr=0 Rc=
+          Cjc=14.57p Vjc=.75 Mjc=.3333 Fc=.5 Cje=26.08p Vje=.75
+          Mje=.3333 Tr=51.35n Tf=451p Itf=.1 Vtf=10 Xtf=2)
*
.PROBE
.TRAN .1u 200u UIC
.END
```

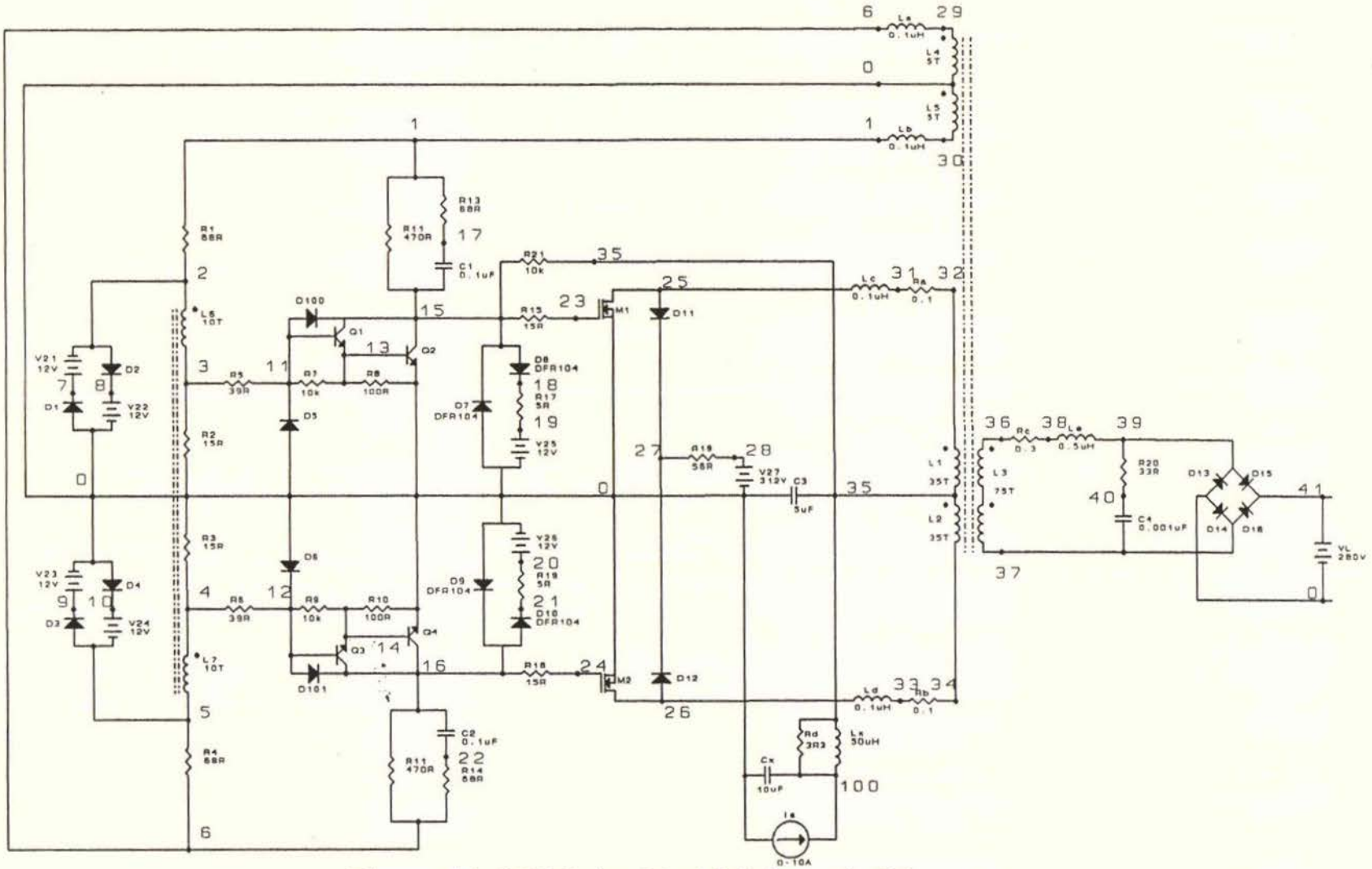


Figure A1 SOI Spice Model Schematic Diagram

APPENDIX B

Selection of Resistor R_f

The diode forward resistance can be neglected since it is assumed that the added series Resistance is much larger. The following variable definitions and reference to Figure B1 will be used:

I_i – Forward current for the ith diode (i= 1 to n)

V_i – Forward voltage for the ith diode (i= 1 to n)

V_T – Total voltage drop across resistor diode pair

$\overline{V}$ – Mean diode forward voltage

$\overline{I}$ – Mean diode forward current

σ_v – Standard deviation for V_{to}

σ_i – Standard Deviation for I

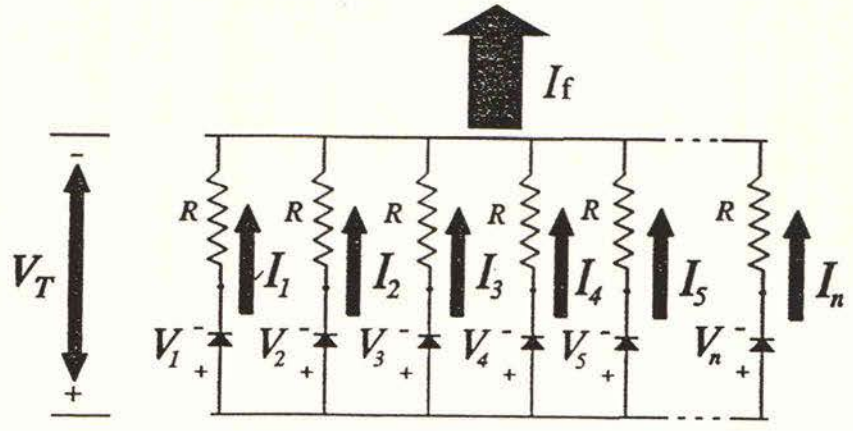


FIGURE PARALLEL DIODE CURRENT BALANCE

For the ith series path:

$$R\,I_i + V_i = V_T \qquad B1$$

Therefore:

$$\sum_{i=1}^{n} [R\,I_i + V_i] = n\,V_T \qquad B2$$

Which can be re–written as:

$$R\sum_{i=1}^{n} I_i + \sum_{i=1}^{n} V_i = n\,V_T \qquad B3$$

Re–arranging and using equation 4.5–1 gives:

$$R\,\overline{I} + \overline{V} = R\,I_i + V_i$$

Further re–arrangement yields:

$$R(I_i - \overline{I}) + (V_i - \overline{V}) = 0 \qquad B4$$

Therefore the following equation is valid:

$$\sum_{i=1}^{n} [R(I_i - \overline{I}) + (V_i - \overline{V})]^2 = 0 \qquad B5$$

Expanding this gives:

$$\sum_{i\ 1}^{n}\{\ [R(I_i-\overline{I})]^2+(V_i-\overline{V})^2+2R(I_i-\overline{I})(V_i-\overline{V})\}=0 \qquad \text{B6}$$

Using equation 4.5–2 results in:

$$\sum_{i}^{n}\{[R(I_i-\overline{I})]^2+(V_i-\overline{V})^2-2R^2(I_i-\overline{I})^2\}=0 \qquad \text{B7}$$

Grouping terms gives:

$$\sum_{i=\ 1}^{n}\{\ (V_i-\overline{V})^2-[R\ (I_i-\overline{I})]^2\}=0 \qquad \text{B8}$$

It therefore can be shown that the following is true:

$$\sqrt{\frac{\sum_{i=1}^{n}(V_i-\overline{V})^2}{n-1}}=R\sqrt{\frac{\sum_{i=1}^{n}(I_i-\overline{I})^2}{n-1}} \qquad \text{B9}$$

Which is an expression relating the standard deviations:

$$\sigma_v=R\ \sigma_i \qquad \text{B10}$$

APPENDIX C.

Freewheel Diode Reverse Maximum Current Calculations

Using the method outlined in Chapter Three. From the DSE1 60–10A data sheet ,[19]:

$$I_{rm} = 32A \text{ @ } m = 480A/\mu S,\ I_f = 60A,\ T_j = 100^oC$$

A junction temperature of 125^oC will be assumed. The maximum bus voltage(672V) will also be used since this represents the worst case. From equation 3–41

$$I_{rm}(T_{j2}) = I_{rm}(T_{j1}) \left[1 + \frac{T_{j2} - T_{j2}}{100} \right]$$

$$I_{rm}(125) = I_{rm}(100) \left[1 + \frac{125 - 100}{100} \right] = 32 \times 1.25 = 40A$$

$$T_x = \frac{I_f + I_{rm}}{m} = \frac{40 + 60}{480} = 0.208\mu S$$

$$\frac{T_m}{T_x} = \frac{I_{rm}}{I_f + I_{rm}} = \frac{40}{40 + 60} = 0.4$$

From Table 3.1:

$$\frac{T_x}{T_t} = 1.6$$

$$T_t = \frac{T_x}{1.6} = \frac{0.208}{1.6} = 0.13\mu S$$

The actual operating conditions for each diode is as follows:

$$I_f = 16.7A$$

$$m = \frac{2\ E}{6L_f} = \frac{672}{6\times 2} = 56.0A/\mu S \text{(note: 6 parallel diodes)}$$

$$V_{rm} = E = 336 \text{ volts (dynamic sharing is assumed)}$$

Using the method outlined in section 3.12:

$$T_o = \frac{I_f}{m} = \frac{16.7}{56.0} = 0.3\mu S$$

$$\frac{T_o}{T_t} = \frac{0.30}{0.13} = 2.3$$

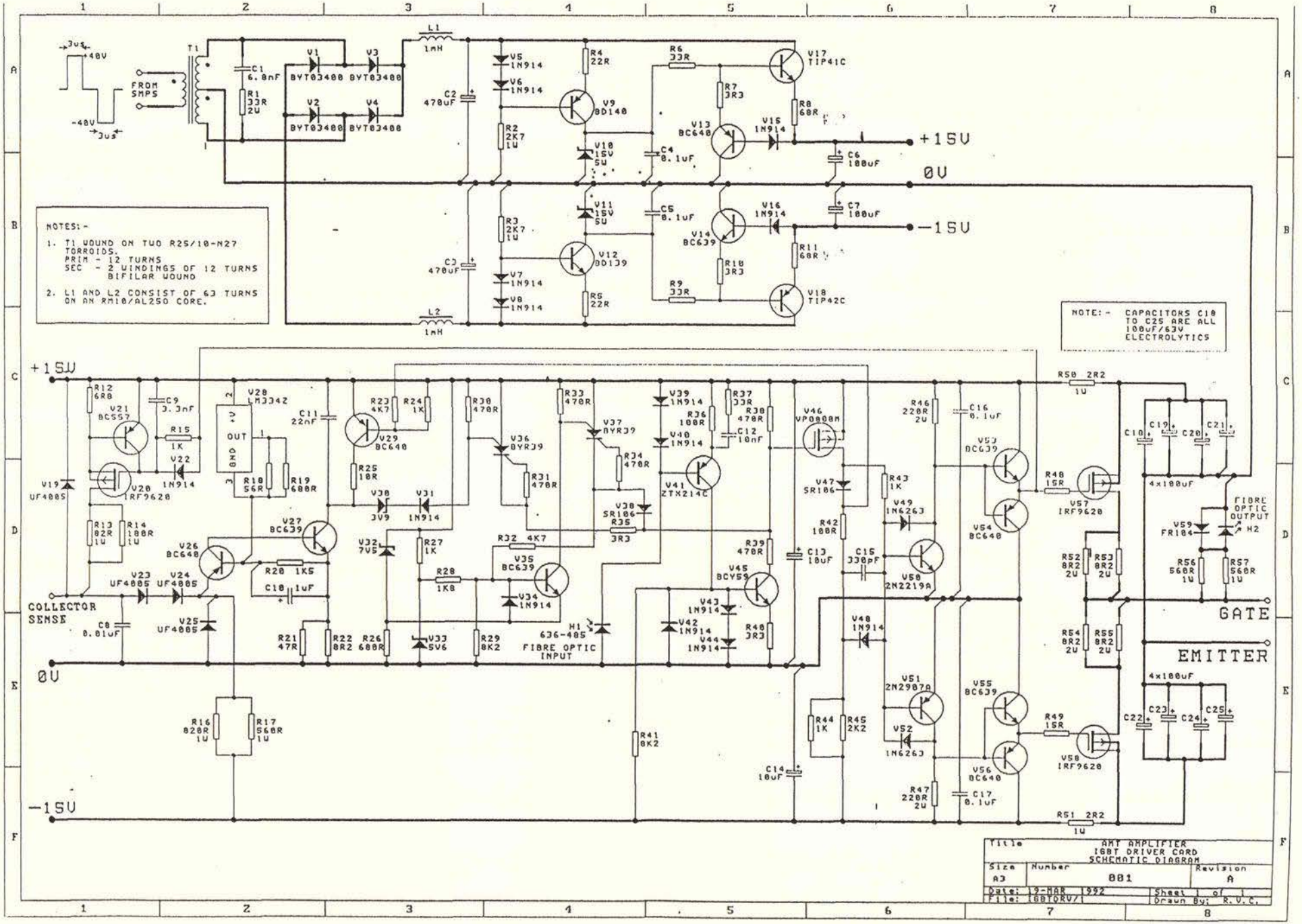
From Table 3.1:

$$\frac{T_x}{T_t} = 3.1$$

$$T_x = 3.1\ T_T = 3.1 \times .130 = 0.403\mu S$$

$$I_{rm} = m\ T_x - I_f = 56.0 \times 0.403 - 16.7 = 5.87A$$

The total freewheel diode reverse current would then be 35.2A.


NOTES:-
1. T1 WOUND ON TWO R25/10-N27 TORROIDS.
PRIM - 12 TURNS
SEC - 2 WINDINGS OF 12 TURNS BIFILAR WOUND
2. L1 AND L2 CONSIST OF 63 TURNS ON AN RM10/AL250 CORE.
NOTE:- CAPACITORS C10 TO C25 ARE ALL 100uF/63V ELECTROLYTICS
+15V
0V
-15V
COLLECTOR SENSE
GATE
EMITTER
FIBRE OPTIC INPUT
FIBRE OPTIC OUTPUT
FROM SMPS
Title
AMT AMPLIFIER
IGBT DRIVER CARD
SCHEMATIC DIAGRAM
Size A3
Number 881
Revision A
Date: 13-MAR 992
Sheet 1 of 1
File: 881DRV1
Drawn By: R.V.C.

APPENDIX E

IGBT Driver Spice Model Listing

```
Vp 1 0 pulse(0 15V 0 5uS 5uS 1S 1S)
Vm 0 2 PULSE(0 15V 0 5uS 5uS 1S 1S)
Id 3 0 PULSE(0 50uA 5uS 0.01uS 0.01uS 2uS 20uS)
R1 1 3 39K
Q1 4 3 16 BC560
Ra 1 16 10
D5 0 4 D1N914
D6 4 104 D1N914
D7 104 0 D1N914
Rn 4 2 8K2
D1 4 5 D1N914
Q2 5 4 6 BC550
R2 1 5 1K
R3 6 0 27
M4 107 5 1 1 VN2222
Rz 107 7 100
R4 7 2 680
D2 21 7 D1N914
Cx 7 21 330pF
R10 107 21 1K
Q5 8 21 0 BC337
D3 21 8 D1N914
Q6 9 21 0 BC327
D4 9 21 D1N914
R5 1 8 220
R6 9 2 220
Q7 1 8 10 BC637
Q8 0 8 10 BC638
Q9 0 9 11 BC637
Q10 2 9 11 BC638
R7 10 12 15
R8 11 13 15
M11 19 12 1 1 IRFD9020
M12 20 13 2 2 IRDF010
Rb 19 14 3.3
Rc 14 20 3.3
Ciss 14 0 .1uF
*
.model BC550  NPN(Is=3.108f Xti=3 Eg=1.11 Vaf=131.5 Bf=325 Ne=1.541
+          Ise=190.7f Ikf=50mA Xtb=1.5 Br=6.18 Nc=2 Isc=0 Ikr=0 Rc=1
+          Cjc=6p Vjc=.75 Mjc=.3333 Fc=.5 Cje=12p Vje=.75
+          Mje=.3333 Tr=51.35n Tf=0.5nS Itf=27mA Vtf=10 Xtf=.7)
*
.model BC560  PNP(Is=3.108f Xti=3 Eg=1.11 Vaf=131.5 Bf=300 Ne=1.541
+          Ise=190.7f Ikf=10mA Xtb=1.5 Br=6.18 Nc=2 Isc=0 Ikr=0 Rc=1
+          Cjc=4.5p Vjc=.75 Mjc=.3333 Fc=.5 Cje=6.0p Vje=.75
+          Mje=.3333 Tr=20n Tf=0.3nS Itf=7.4mA Vtf=10 Xtf=.72)
*
*
.model BC337  NPN(Is=3.108f Xti=3 Eg=1.11 Vaf=131.5 Bf=217.5 Ne=1.54
+          Ise=190.7f Ikf=1.296 Xtb=1.5 Br=6.18 Nc=2 Isc=0 Ikr=0 Rc=
+          Cjc=14.57p Vjc=.75 Mjc=.3333 Fc=.5 Cje=26.08p Vje=.75
+          Mje=.3333 Tr=51.35n Tf=451p Itf=.1 Vtf=10 Xtf=2)
*
.model BC327  PNP(Is=9.913f Xti=3 Eg=1.11 Vaf=90.7 Bf=197.8 Ne=2.264
+          Ise=6.191p Ikf=.7322 Xtb=1.5 Br=3.369 Nc=2 Isc=0 Ikr=0 Rc
+          Cjc=14.57p Vjc=.75 Mjc=.3333 Fc=.5 Cje=20.16p Vje=.75
+          Mje=.3333 Tr=29.17n Tf=405.6p Itf=.4 Vtf=10 Xtf=2)
```

```
*
.model BC637  NPN(Is=3.108f Xti=3 Eg=1.11 Vaf=131.5 Bf=217.5 Ne=1.541
+          Ise=190.7f Ikf=1.296 Xtb=1.5 Br=6.18 Nc=2 Isc=0 Ikr=0 Rc=1
+          Cjc=14.57p Vjc=.75 Mjc=.3333 Fc=.5 Cje=26.08p Vje=.75
+          Mje=.3333 Tr=51.35n Tf=451p Itf=.1 Vtf=10 Xtf=2)
*
.model BC638 PNP(Is=9.913f Xti=3 Eg=1.11 Vaf=90.7 Bf=197.8 Ne=2.264
+          Ise=6.191p Ikf=.7322 Xtb=1.5 Br=3.369 Nc=2 Isc=0 Ikr=0 Rc=1
+          Cjc=14.57p Vjc=.75 Mjc=.3333 Fc=.5 Cje=20.16p Vje=.75
+          Mje=.3333 Tr=29.17n Tf=405.6p Itf=.4 Vtf=10 Xtf=2)
*
.model VN2222 PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+          Tox=100n Uo=600 Phi=.6 Rs=5.724m Kp=.6u W=.015 L=.1u
+          Vto=-2.5 Rd=364m Rds=500K Cbd=.08n Pb=.8 Mj=.5 Fc=.5
+          Cgso=.18n Cgdo=.032n Rg=18.6 Is=648.2E-18)
*
.model IRDF010  NMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+          Tox=100n Uo=600 Phi=.6 Rs=5.724m Kp=20.76u W=.31 L=2u
+          Vto=2.75 Rd=2.6m Rds=400K Cbd=.4n Pb=.8 Mj=.5 Fc=.5
+          Cgso=.9n Cgdo=.15n Rg=5 Is=648.2E-18)
*
.model IRFD9020  PMOS(Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0

+          Tox=100n Uo=300 Phi=.6 Rs=.1429 Kp=9.899u W=1.1 L=2u
+          Vto=-2.75 Rd=74.02m Rds=400K Cbd=.4n Pb=.8 Mj=.5 Fc=.5
+          Cgso=.9n Cgdo=.15n Rg=5 Is=1E-30)
*
.MODEL D1N914 D(IS=100E-15 RS=16 CJO=2PF TT=12NS BV=100 IBV=100E-15)
*
*
.TRAN 0.01U 10u UIC
.PROBE
.END
```

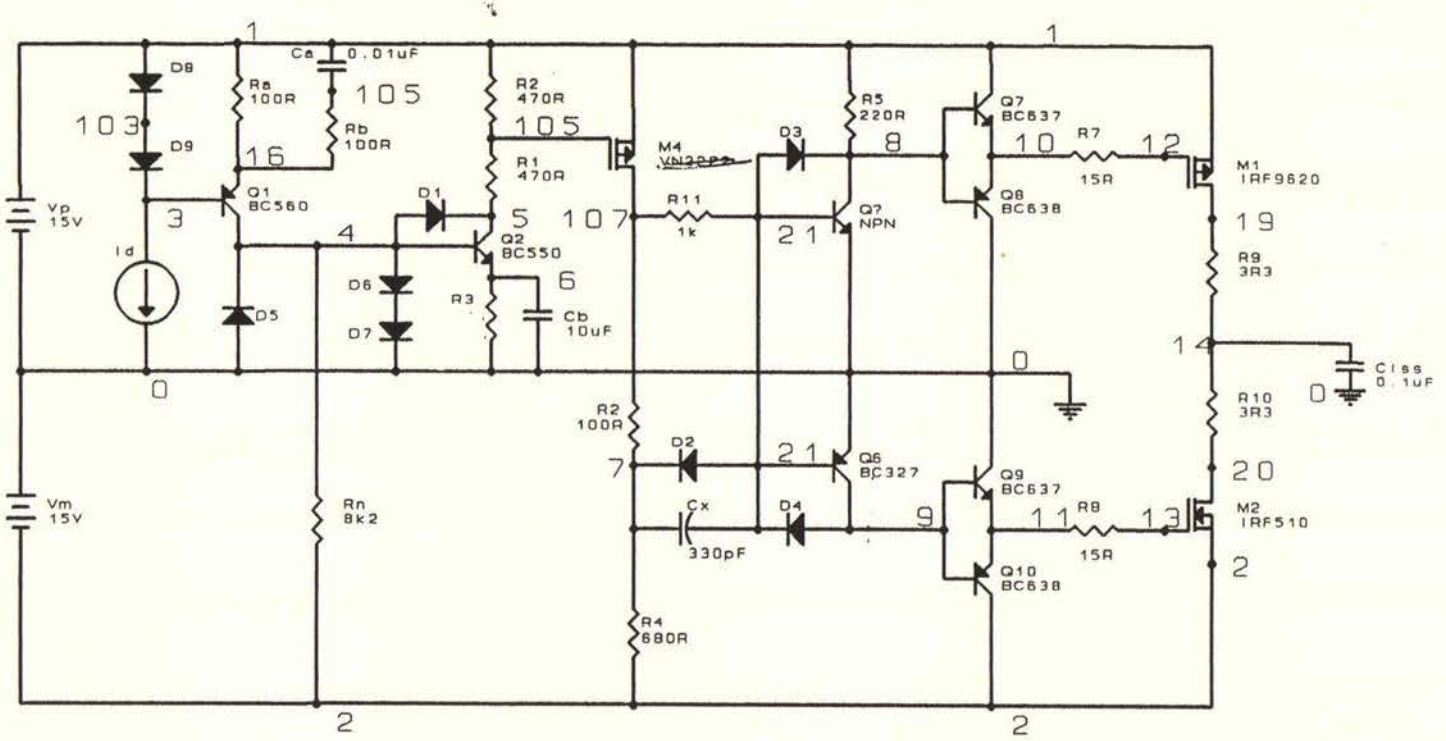


Figure E1 IGBT Drive Module Spice Model Schematic Diagram

APPENDIX F

Diode D_c Reverse Recovery Calculation

If the diode D_c carriers a forward current of 25A and the commutation dI/dt is 39A/μS the reverse maximum current is calculated as follows using the methods of Chapter three:

$$T_o = \frac{I_f}{m} = \frac{25}{39} = 0.64\mu S$$

$$T_t = 0.13\mu S \ @125^oC$$

$$\frac{T_o}{T_t} = \frac{0.64}{0.13} = 4.9$$

From table 3.1:

$$\frac{T_x}{T_t} = 5.7$$

$$T_x = 5.7 \times 0.13 = 0.741\mu S$$

$$I_{rm} = m\ T_x - I_f$$

$$= 39 \times 0.741 - 25 = 3.9A$$

APPENDIX G

Amplifier Photographs

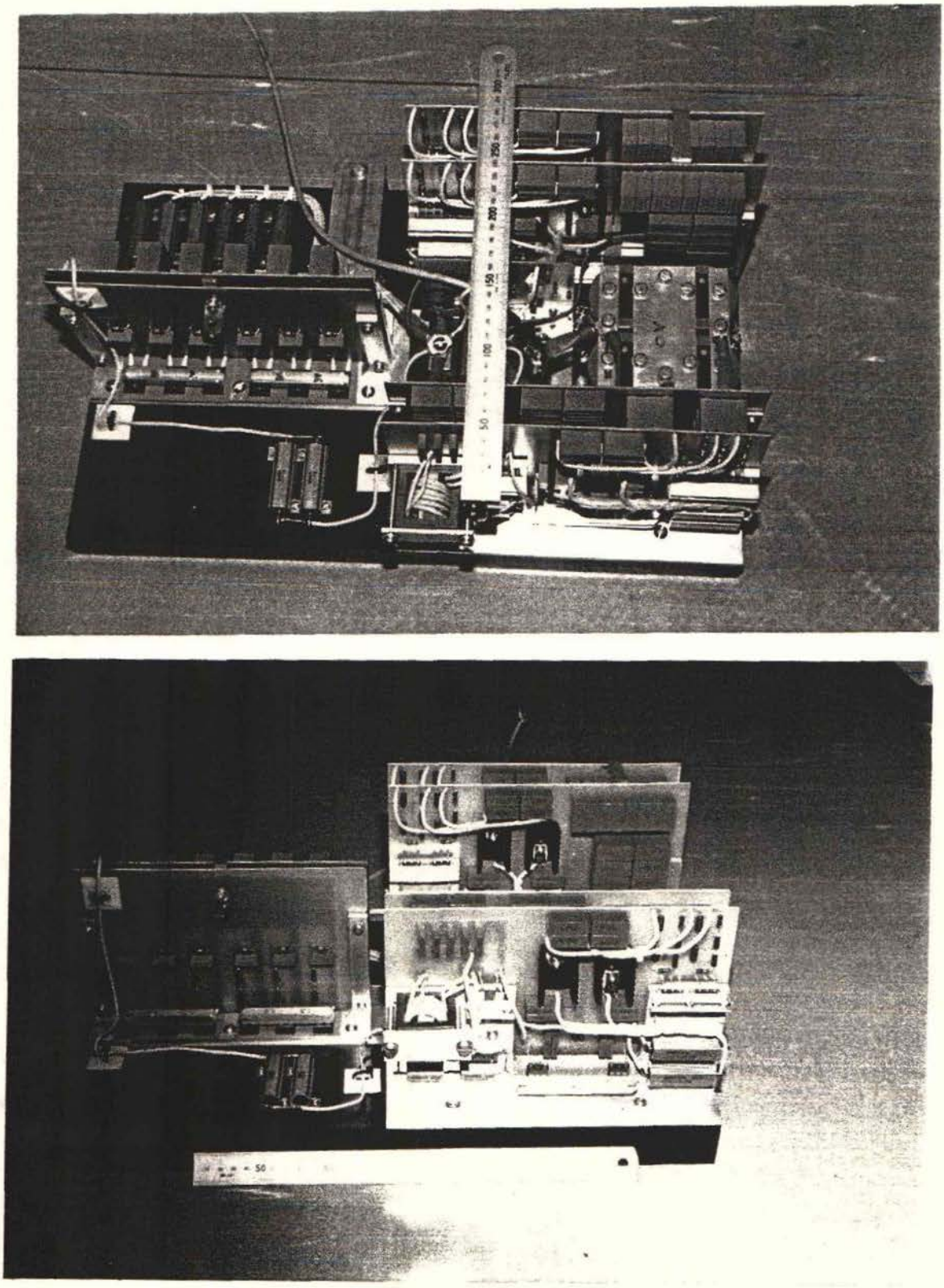


Figure G1 Positive Buck Converter Module

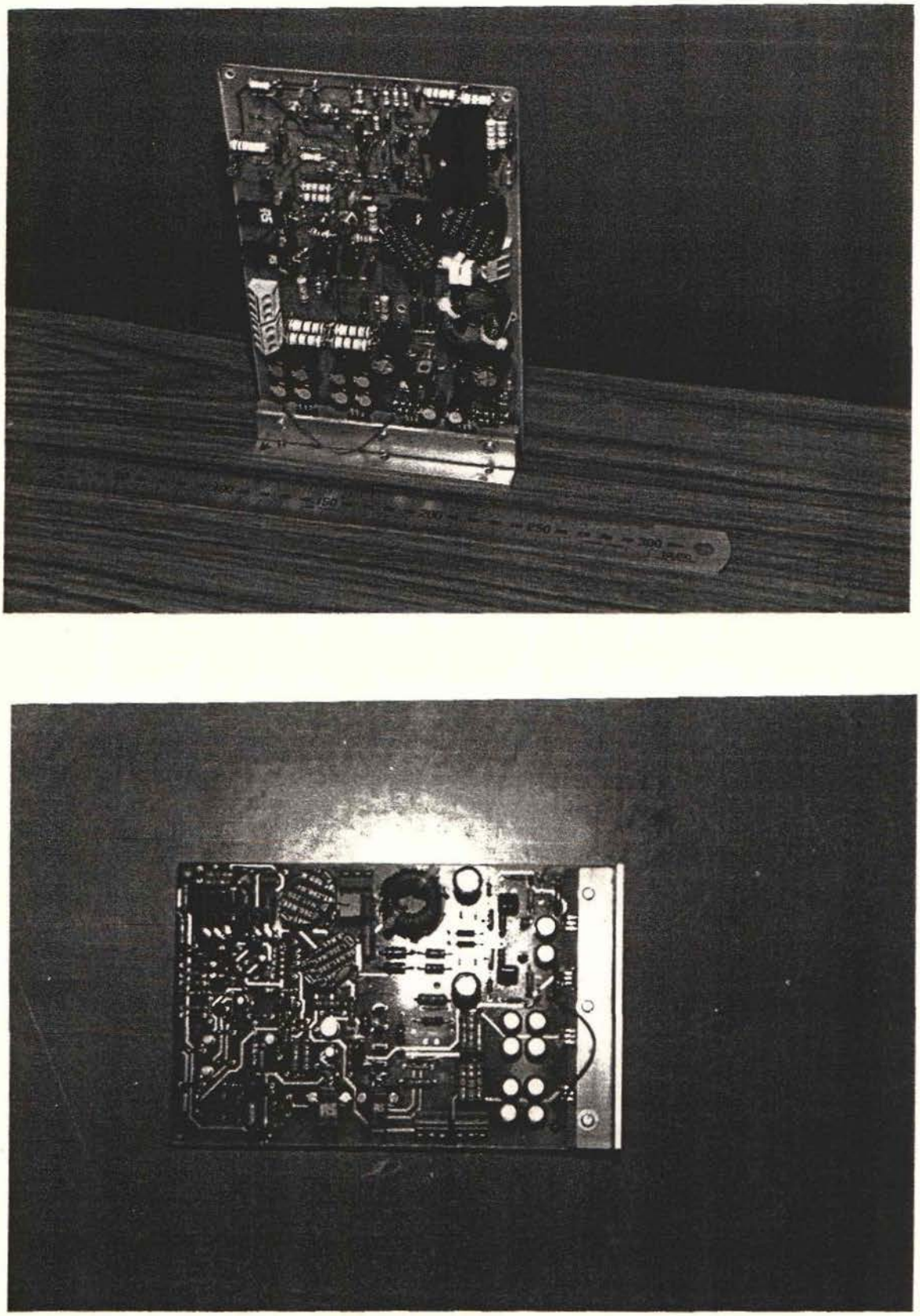
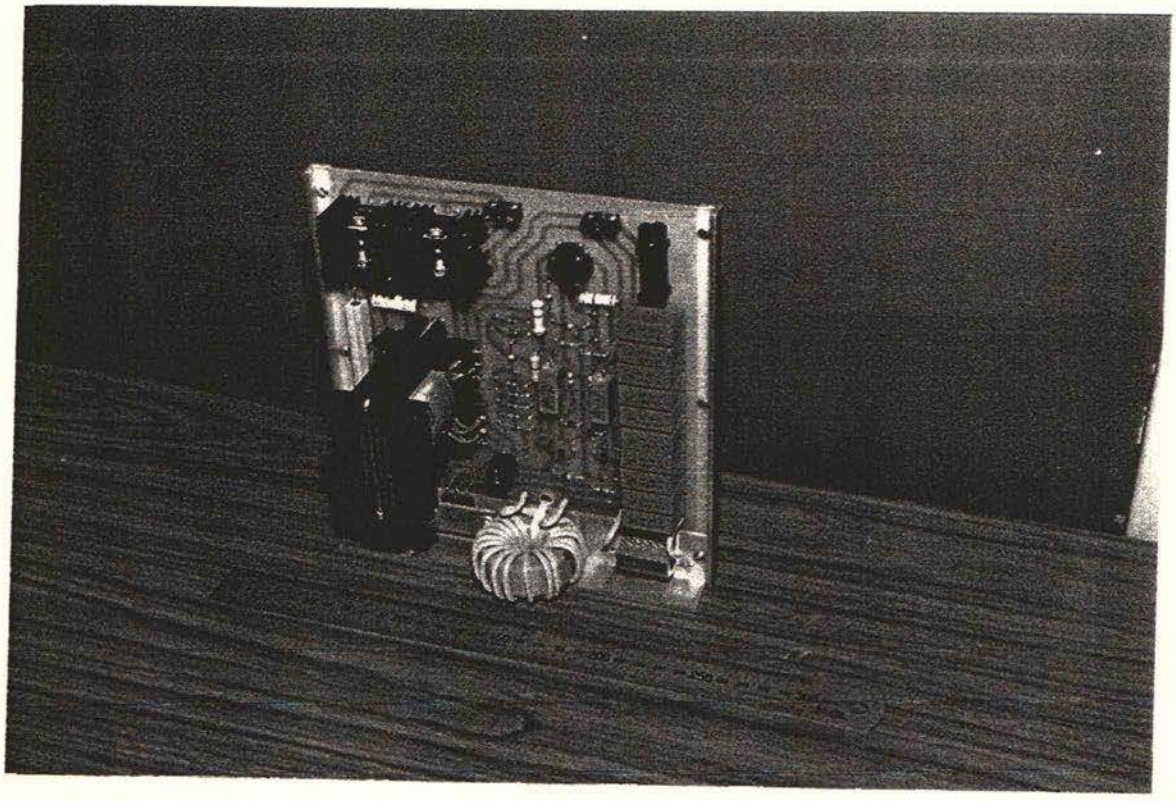


Figure G2 IGBT Gate Drive Module



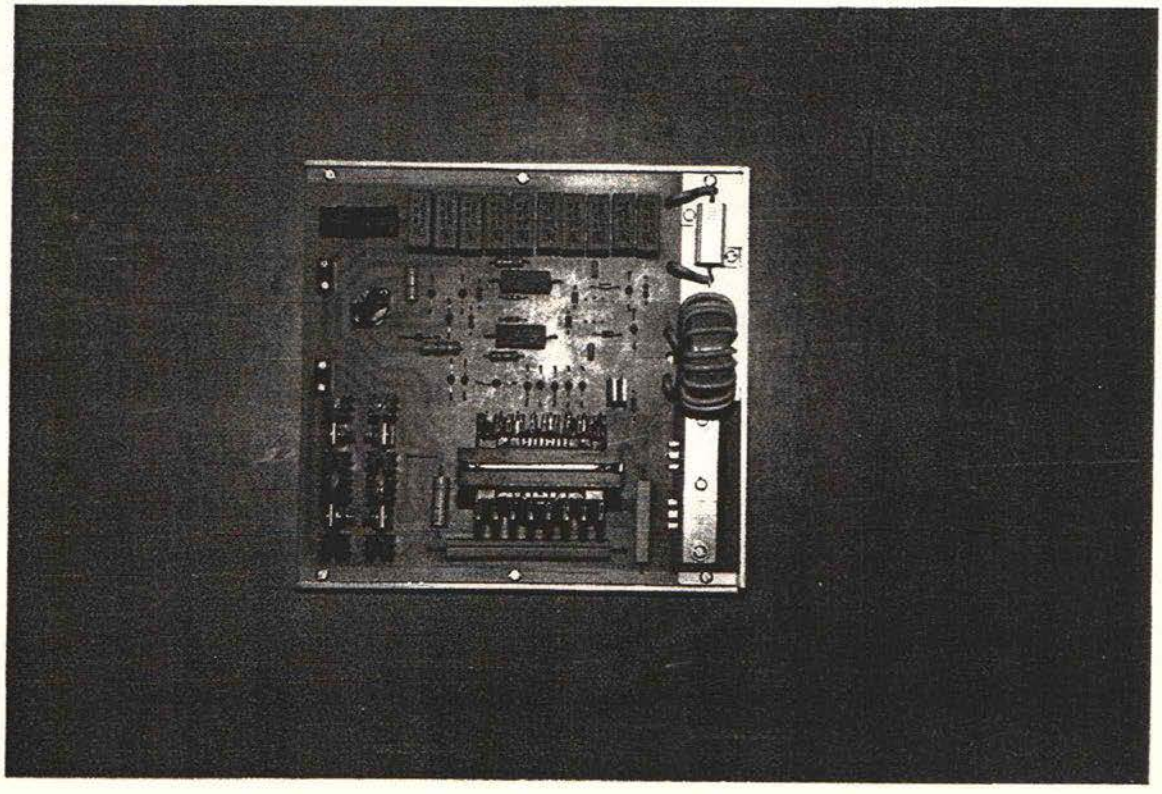


Figure G3 Self Oscillating Converter Module

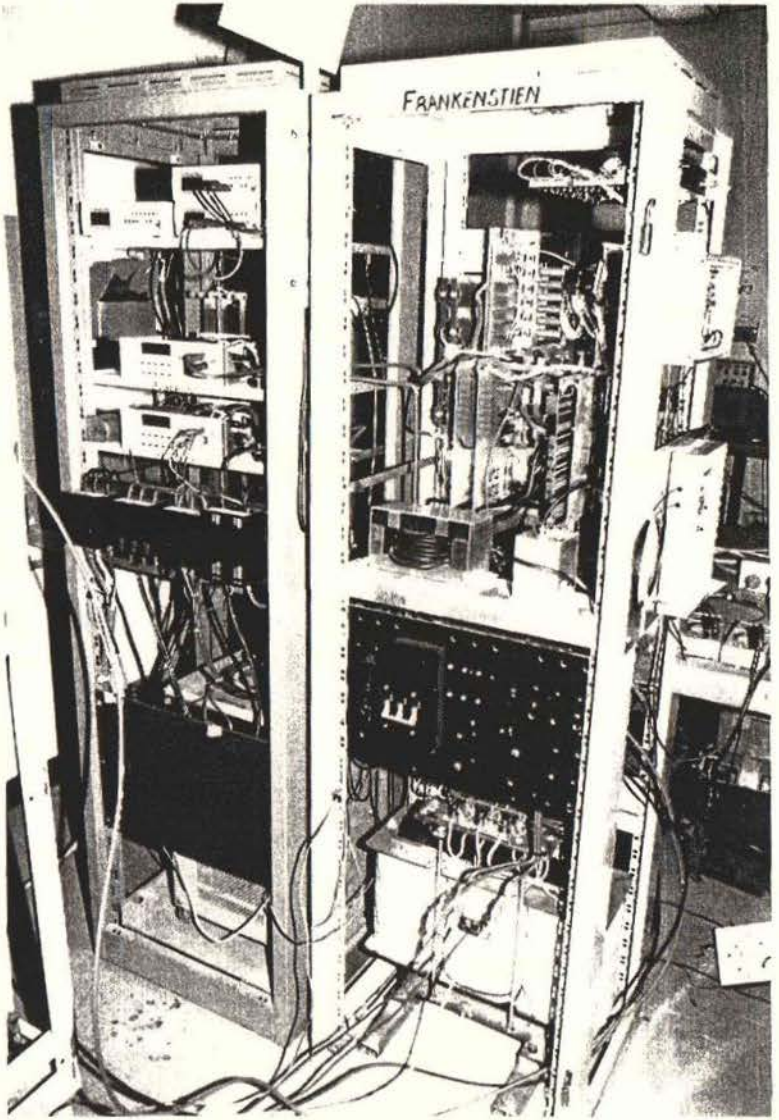
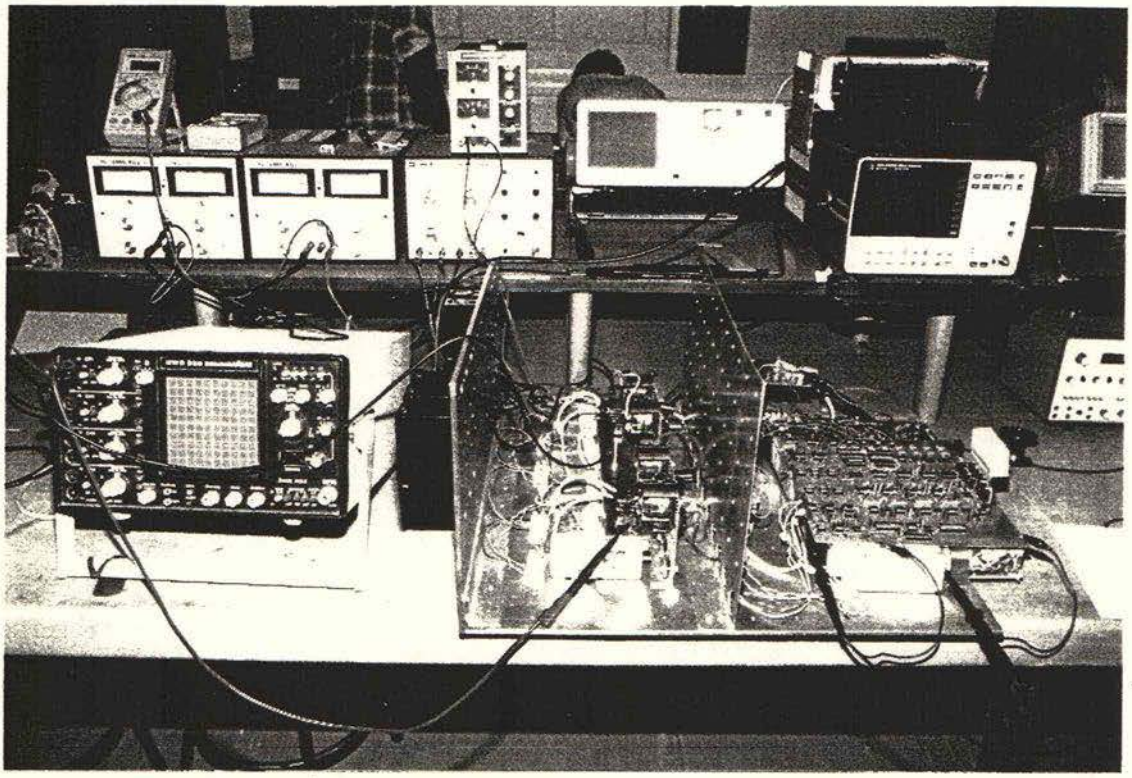


Figure G4 Buck Converter Test Installation and Loading Banks



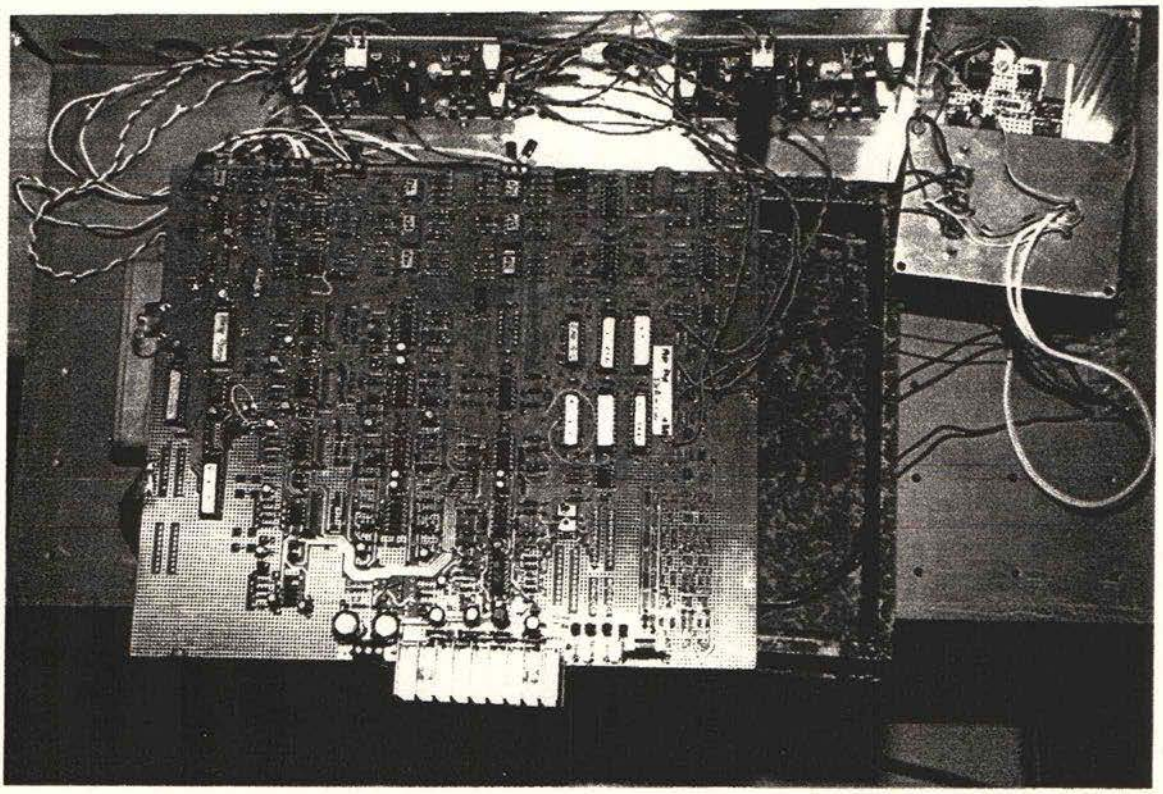


Figure G5 Scale Model Test Installation and Controller PCB

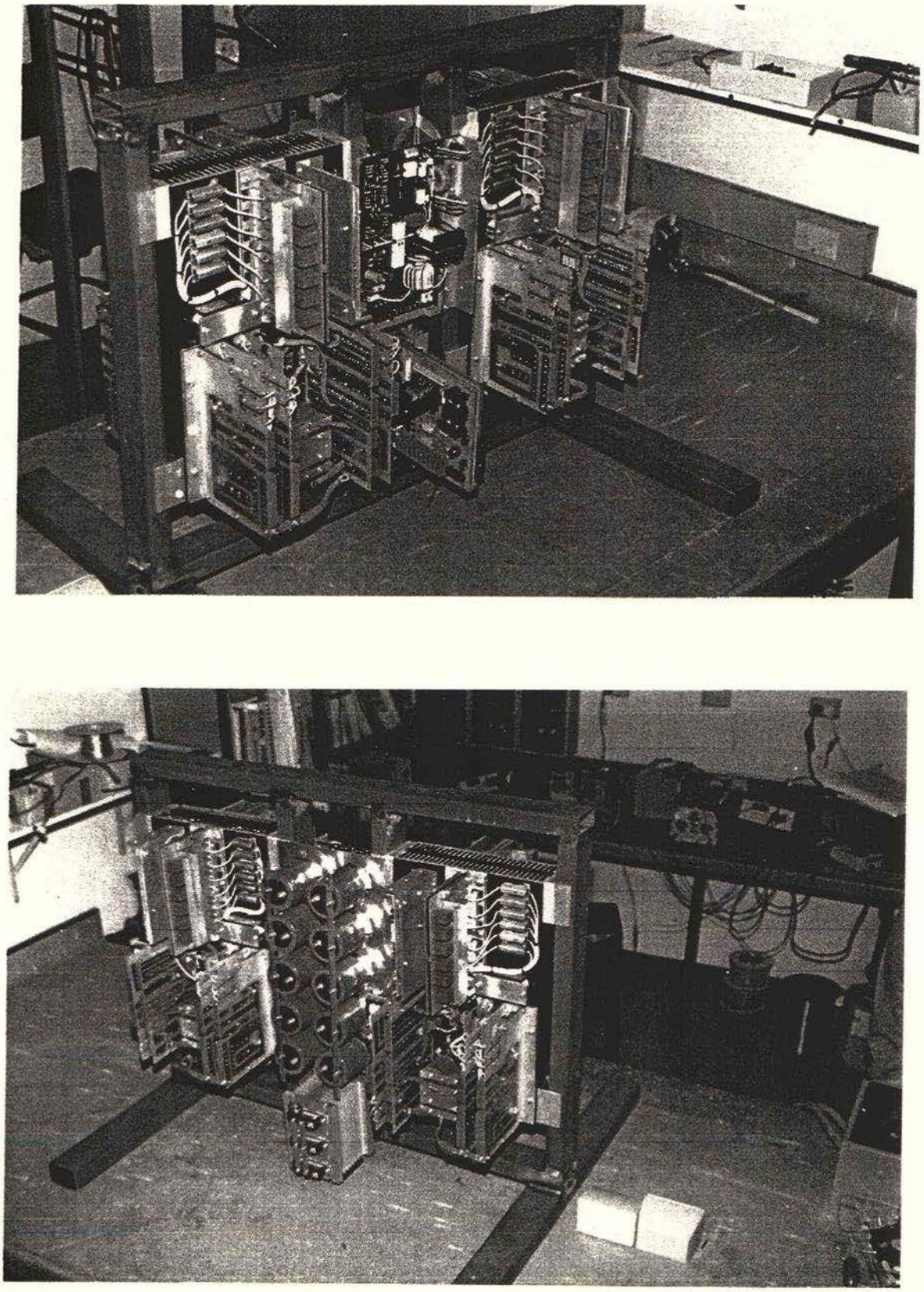


Figure G6 The Amplifier during the Construction Phase

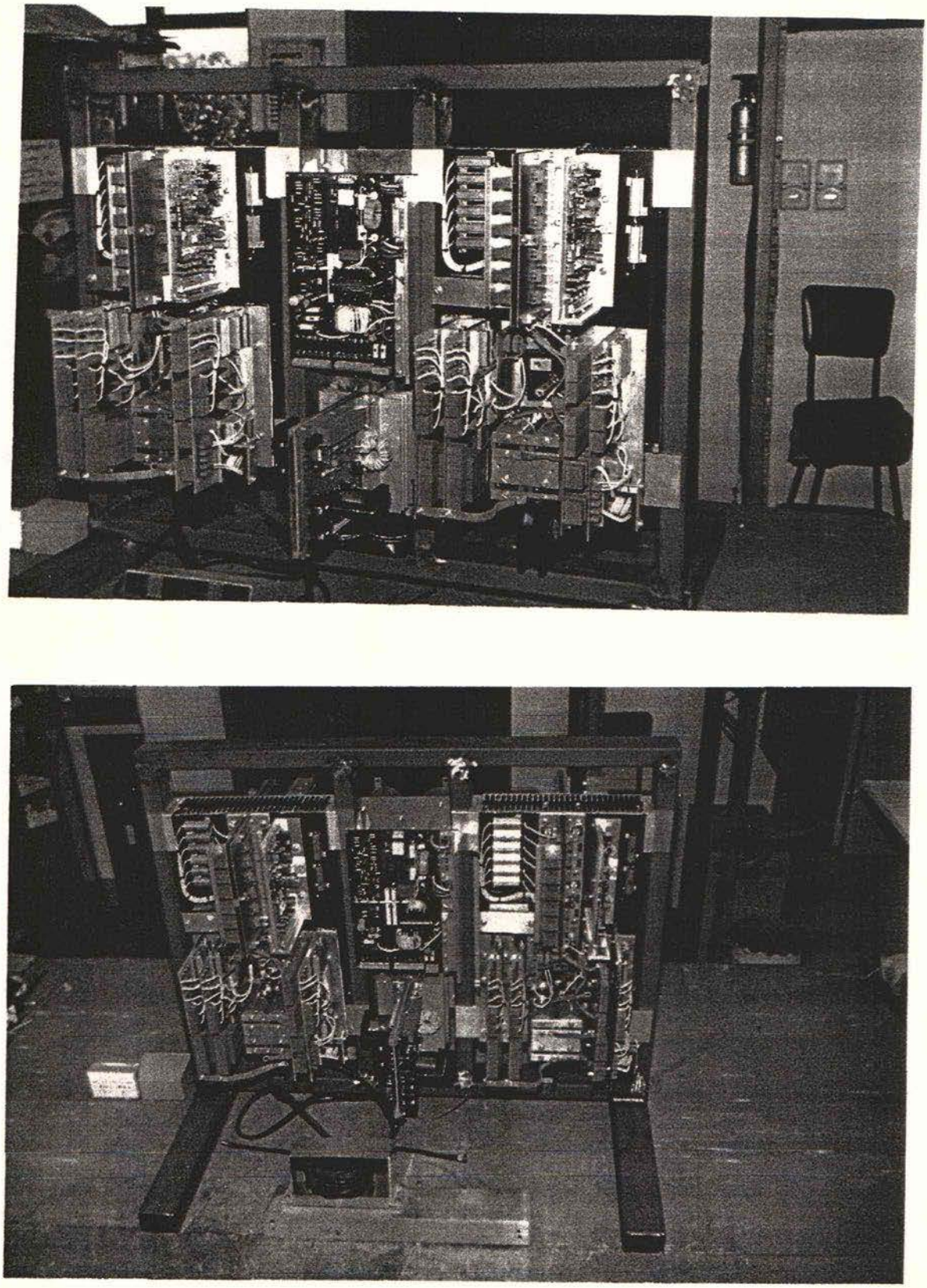


Figure G7 The Amplifier during the Construction Phase

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