A UPFC WITH REDUCED DC BUS CAPACITANCE FOR VOLTAGE REGULATION AND PHASE BALANCING IN LV DISTRIBUTION NETWORKS WITH HIGH PV PENETRATIONS

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ABSTRACT

The penetration level of photovoltaic (PV) power in the low voltage (LV) distribution networks is rapidly increasing. The European Photovoltaic Industry Association reported the installed capacity of PV systems globally reached 177GW at the end of 2014. The annual rate of installations, 38.7GW in 2014, continues to increase. A large part of this is installed as residential systems connected to LV networks. The Australian Clean Energy Regulator has published a report showing the total installed capacity of PV in Australia exceeded 4.5GW in 2015. The impacts of high PV penetrations in LV residential distribution networks include voltage rise, voltage unbalance, and reverse power flow which may limit the level of photovoltaic penetration within the LV distribution networks. A four-leg compensator based on a unified power flow controller (UPFC) concept is proposed for simultaneous voltage and current compensation in LV distribution systems. As a voltage compensator, this compensation device is shown to be capable of regulating the positive, negative and zero sequence voltage in LV distribution networks under high PV penetrations. At the same time, as a current compensator, the device is capable of power factor correction, zero sequence or neutral current compensation, harmonic current compensation and a degree of negative sequence current compensation.

Instantaneous reactive power theory shows that DC-bus capacitor power will fluctuate at twice mains frequency during any unbalanced operation of the regulator. Real and instantaneous power balance of the UPFC can be maintained by allowing the input shunt converter to draw a small positive and negative sequence current respectively. Instantaneous power balance with negative sequence current makes it possible to reduce the DC bus capacitance which allows long life ceramic or polypropylene capacitors to replace electrolytic capacitors.

The operation of the proposed UPFC based four-leg compensator has been demonstrated by extensive simulation studies. These confirm that the device can perform the full range of series and parallel compensation duties for the compensation of voltage and current respectively. It has also been demonstrated that the DC bus voltage can be controlled using relatively small DC bus capacitors. The simulation work is further confirmed by experimental work with a small scale laboratory model. The laboratory system used commercial inverter modules rated at 600V and 15A per phase to construct two inverters with four phase legs. These were configured as a parallel connected inverter and a series inverter with series voltage injection transformers. The four-leg inverters shared a common DC bus and were equipped with voltage and current transformers and controlled using a Texas Instruments Delfino processor.

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LIST OF SYMBOLS

i_s	Source currents
i_C	Compensating currents
v_C	Compensating voltages
C_{DC}	DC bus capacitance
V_{dc}	Average DC bus capacitor voltage
Z	Feeder impedance
R	Feeder resistance
X	Feeder reactance
V_1	Transformer primary voltage
V_2	Transformer secondary voltage
I_1	Transformer primary current
I_2	Transformer secondary current
SW	Switch
V_G	Grid voltages
P_G	Generator real power
Q_G	Generator reactive power
P_L	Load real power
Q_L	Load reactive power
EPT	Electronic power transformer
P_{pv}	Real power supplied by PV
S	Apparent power
Q_{limt}	Reactive power limit
V_{bus}	Bus voltage
V_{pcc}	Voltage at point of common coupling
L_{fin}	Input filter inductance
L_{fout}	Output filter inductance
C_{fin}	Input filter capacitance
C_{fout}	Output filter capacitance
$i_a(t)$	Line a current
$i_b(t)$	Line b current

$i_c(t)$	Line c current
$i_{Ap}(t)$	Shunt converter phase a input current
$i_{Bp}(t)$	Shunt converter phase b input current
$i_{Cp}(t)$	Shunt converter phase c input current
$v_{Aa}(t)$	Series injection voltage at phase a
$v_{Bb}(t)$	Series injection voltage at phase b
$v_{Cc}(t)$	Series injection voltage at phase c
$i_s(t)$	Series converter instantaneous power
$p_p(t)$	Shunt converter instantaneous power
$p_{dc}(t)$	Instantaneous power at DC bus
$i_{dc}(t)$	DC bus capacitor instantaneous current
$v_{dc}(t)$	DC bus capacitor instantaneous voltage
$\overline{p_s}$	Average component of series converter instantaneous power
$\widetilde{p_s}$	Oscillatory component of series converter instantaneous power
$\overline{p_p}$	Average component of shunt converter instantaneous power
$\widetilde{p_p}$	Oscillatory component of shunt converter instantaneous power
V_{s+}	Positive sequence component of series injected voltage
V_{s-}	Negative sequence component of series injected voltage
V_{s0}	Zero sequence component of series injected voltage
I_{s+}	Positive sequence component of line current
I_{s-}	Negative sequence component of line current
I_{s0}	Zero sequence component of line current
φ_{vs+}	Phase angle of positive sequence component of series injection voltage
φ_{vs-}	Phase angle of negative sequence component of series injection voltage
φ_{vs0}	Phase angle of zero sequence component of series injection voltage
φ_{is+}	Phase angle of positive sequence component of line current
φ_{is-}	Phase angle of negative sequence component of line current
φ_{is0}	Phase angle of zero sequence component of line current
$v_{AN}(t)$	Shunt converter input voltage at phase A to N
$v_{BN}(t)$	Shunt converter input voltage at phase B to N
$v_{CN}(t)$	Shunt converter input voltage at phase C to N
V_{p+}	Positive sequence component of shunt converter input voltage

V_{p-}	Negative sequence component of shunt converter input voltage
V_{p0}	Zero sequence component of shunt converter input voltage
I_{p+}	Positive sequence component of shunt converter input current
I_{p-}	Negative sequence component of shunt converter input current
I_{p0}	Zero sequence component of shunt converter input current
φ_{vp+}	Phase angle of positive sequence component of shunt converter input voltage
φ_{vp-}	Phase angle of negative sequence component of shunt converter input voltage
φ_{vp0}	Phase angle of zero sequence component of shunt converter input voltage
φ_{ip+}	Phase angle of positive sequence component of shunt converter input current
φ_{ip-}	Phase angle of negative sequence component of shunt converter input current
φ_{ip0}	Phase angle of zero sequence component of shunt converter input current
E_c	Energy stored at DC bus capacitor
V_U	Upper limit of voltage at DC bus capacitor
V_L	Lower limit of voltage at DC bus capacitor
$i_{Ah}(t)$	Instantaneous value of 5th harmonic current through phase A
$i_{Bh}(t)$	Instantaneous value of 5th harmonic current through phase B
$i_{Ch}(t)$	Instantaneous value of 5th harmonic current through phase C
$i_{nhABC}(t)$	Instantaneous value of three phase harmonic current demand signal
I_{h-}	Peak value of 5th harmonic current
φ_{ih-}	Phase angle of the 5th harmonic current
$p_h(t)$	5th harmonic instantaneous power
$\widetilde{p_h}$	5th harmonic average power
$\overline{p_h}$	5th harmonic oscillatory power
τ	Time period of a cosine waveform for half cycle
T	Time period of a cosine waveform for full cycle
ω	Angular frequency in rad/s
$v_{ar+}(t)$	Positive sequence instantaneous voltage reference for phase A
$v_{br+}(t)$	Positive sequence instantaneous voltage reference for phase B
$v_{cr+}(t)$	Positive sequence instantaneous voltage reference for phase C
$v_{an}(t)$	Instantaneous output voltage reference at phase A
$v_{bn}(t)$	Instantaneous output voltage reference at phase B
$v_{cn}(t)$	Instantaneous output voltage reference at phase C

$v_{abc}(t)$	Three phase instantaneous output voltage
$v_{ABC}(t)$	Three phase instantaneous input voltage
V_{d+}	Positive sequence d-axis voltage component
V_{q+}	Positive sequence q-axis voltage component
V_0	Positive sequence 0-axis voltage component
V_{d-}	Negative sequence d-axis voltage component
V_{q-}	Negative sequence q-axis voltage component
R_{vd+}	Reference real voltage set point for d-axis
$G_{d+}(s)$	PI type positive sequence voltage compensator for d-axis
$G_{q+}(s)$	PI type negative sequence voltage compensator for q-axis
$G_0(s)$	PI type zero sequence voltage compensator for 0-axis
$G_{d-}(s)$	PI type positive sequence voltage compensator for d-axis
$G_{q-}(s)$	PI type negative sequence voltage compensator for q-axis
$G_{cdc}(s)$	PI type DC bus voltage compensator
$G_{cinst}(s)$	P type instantaneous capacitor voltage restraint signal
$G_{c2\omega}(s)$	PI type 2ω oscillatory power compensator
$G_{crc}(s)$	PI type reactive current compensator
$G_{chABC}(s)$	PI type three phase harmonic current compensators
$R_a\,C$	Cosine reference signal for phase A
$R_b\,C$	Cosine reference signal for phase B
$R_c\,C$	Cosine reference signal for phase C
$R_a\,S$	Sine reference signal for phase A
$R_a\,S$	Sine reference signal for phase B
$R_a\,S$	Sine reference signal for phase C
v_{ab}	Line voltage between phase a and b
v_{cb}	Line voltage between phase c and b
φ_e	Phase error
K_p	Proportional gain of PI controller
K_i	Integral gain of PI controller
s_f	Switching states for the phase leg f
s_a	Switching states for the phase leg a
s_b	Switching states for the phase leg b
s_c	Switching states for the phase leg c

v_{af}	Four-leg inverter phase a to neutral voltage
v_{bf}	Four-leg inverter phase b to neutral voltage
v_{cf}	Four-leg inverter phase c to neutral voltage
v_{a_ref}	Reference voltage vectors normalised with V_{dc} at phase a
v_{b_ref}	Reference voltage vectors normalised with V_{dc} at phase b
v_{c_ref}	Reference voltage vectors normalised with V_{dc} at phase c
V_1 *to* V_{16}	Switching vectors for different switching states
RP	Range pointer
d_i	Duty cycle
R_A	Resistor connected with phase A at the grid side
R_a	Load resistor connected with phase A
R_b	Load resistor connected with phase B
R_c	Load resistor connected with phase C
R_f	Filter resistance
L_f	Filter inductance
C_{1f} and C_{2f}	Filter capacitance
V_{gA}	Grid voltage at phase A
V_{gB}	Grid voltage at phase B
V_{gC}	Grid voltage at phase C
V_{AN}	Input terminal voltage at phase A to N
V_{BN}	Input terminal voltage at phase B to N
V_{CN}	Input terminal voltage at phase C to N
V_{an}	Output load voltage at phase a to n
V_{bn}	Output load voltage at phase b to n
V_{cn}	Output load voltage at phase c to n
I_{real}	Shunt converter real current
$I_{reactive}$	Shunt converter reactive current
I_{a_demand}	Phase a current demand for shunt converter
I_{b_demand}	Phase b current demand for shunt converter
I_{c_demand}	Phase c current demand for shunt converter

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DECLARATION

The research and discussion presented in this thesis are the original work of the author and has not been submitted at any tertiary institute or University for any other award. Any material with has been presented by any person or institute is duly referenced, and a complete list of all references is presented in the bibliography.

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Md. Mejbaul Haque

PUBLICATIONS

The following publications have been produced during the course of this thesis:

[1] M. Mejbaul Haque and P. Wolfs, "A four-wire reduced bus capacitance UPFC for LV distribution networks with high PV penetrations," in *2014 Australasian Universities Power Engineering Conference (AUPEC),* Perth, Australia, 28 September - 1 October 2014, pp. 1-7.

Statement of Author Contribution:

In this work, the capability of four-wire UPFC with reduced DC bus capacitance for voltage regulation and neutral current compensation in LV distribution networks is explored. As an author, I developed the modeling and instantaneous power flow equations for four-leg UPFC in continuous domain. I designed the control methodologies for the series and shunt converter equipped zero sequence current compensator. I built and simulated the model using Matlab Simulink software. The simulation data was recorded and plotted using Matlab programming.

[2] M. Mejbaul Haque and P. Wolfs, "A Reduced Capacitance UPFC with Active Filtering Capability for High PV Penetration Applications," in *IEEE PES Asia-Pacific Power and Energy Engineering Conference 2015 (IEEE PES APPEEC 2015)*, Brisbane, Australia, 15 - 18 November 2015 (Accepted).

Statement of Author Contribution:

In this work, the active filtering capability of a reduced bus capacitance unified power flow controller (UPFC) is explored. In addition, I demonstrated the other capabilities such as voltage regulation and reactive current compensation. As an author, I developed the control models for UPFC based active filter. I was responsible for the control designs, simulation results and the discussions of the results. The simulation studies are carried out using Matlab Simulink.

Chapter 1 INTRODUCTION

1.1. Distributed generation and growth of PV

Distributed generators are smaller and numerous sources of electrical power connected either directly to the distribution network or on the customer side of the meter [1]. Distributed generation generally tends to provide small scale power generation, while large centralised power plants supply the majority of the nation's power. Distributed energy systems are capable of generating electricity on or close to the site where that energy will be used. The global demand for electrical energy is constantly growing. While there is no shortage of fossil fuels, environmental concerns are a strong driver for the uptake of renewable sources. Among a variety of renewable energy sources, PV is one of the major sources of distributed renewable energy [1] and is predicted to become the biggest contributor to electricity generation among all renewable energy candidates by 2040 [2] . It is also environmentally friendly and produces electricity with no harmful emissions. The use of distributed PV is growing across the world as an alternative. Energy storage is sometimes integrated to improve availability. Residential customers are showing great interest in integration of distributed PV generation in the form of roof-top domestic systems. The total solar power installations in the world exceeded 177GW at the end of 2014 [3]. A large part of this total PV is installed as single phase rooftop PV by the customers at their premises in LV distribution networks. Over 30 countries are currently participating in PV installation, and 20 countries had already passed their 1GW mark at the end of 2014. The International Energy Agency (IEA) has estimated that the world's PV capacity will increase up to 308GW by 2018. In Australia, PV installations are mostly residential in the form of rooftop solar PV, but there are also a growing number of commercial rooftop systems. The growth in solar PV installations is significant and still

continues strongly as new generations of households are looking forward to solar to limit the rising cost of existing grid-based electricity. Rooftop solar PV installations in Australia reached a capacity of more than 4.5 GW in 2015 as reported in [4].

1.2. Integration of distributed PV generation in LV distribution network

The adoption of PV energy globally is growing and part of this PV generation is being integrated into LV distribution networks. The existing distribution networks were primarily constructed without considering the possibility of large scale PV penetration into the LV distribution networks. Most of the existing distribution networks are of the radial type where the power flows from upstream transformers on the medium voltage networks to downstream LV networks. The usual behaviour of LV distribution networks may change depending upon the level of PV penetration. For example, the voltage profile of any distribution network is directly impacted by the level of PV penetration on it. Due to the increased level of PV penetration into LV distribution networks, the loads generally consume a significant portion of power locally from the installed PV while consuming reduced power from the distribution networks. This causes significant voltage variation in the LV distribution networks which is not desirable and should be managed so as to remain within acceptable limits. In some cases, the direction of power flow may become reversed in parts of the distribution network when the solar generation by the PV modules exceeds the feeder load demand [5]. Change of network voltage profile and reversal of power flow direction are the most significant power quality issues that may appear in LV distribution networks with the inclusion of distributed generation [6]. In addition, unbalanced variation in voltage may also occur due to the unbalanced solar generation or unbalanced loading in four-wire LV distribution networks. This may cause an undesirable low voltage on one phase while increasing the voltage of remaining phases, which is potentially damaging for electric appliances [7]. In addition, over-voltage is a common phenomenon observed in LV

distribution networks with high penetration of residential roof-top PV. For instance, during the middle of any day of a working week, the solar generation may be higher than the load demand. In such cases, high voltages may cause inverter tripping and the subsequent loss of solar generation. In addition, high PV penetrations also causes several other power quality problems including voltage unbalance, voltage drop/rise and voltage flicker etc. which limit the capability of distribution networks to allow a large quantity of PV penetration. All these impacts may limit the level of PV penetration within the LV distribution networks.

1.3. Compensator for LV distribution networks with distributed PV generation: A Unified Power Flow Controller (UPFC) Proposal

To achieve higher penetration of renewable generation within the LV distribution networks while preventing loss of solar generation, the incorporation of intelligent control, storage or regulatory devices are required in the LV distribution networks [8, 9]. The authors of [8] propose a coordinated control of distributed energy storage with tap changing transformers for voltage rise mitigation. Integration of batteries as storage devices with PV systems are proposed in [9] which shows that storage can shift the peak demand by allowing the PV/storage system to charge during high solar generation periods on off-peak and discharge during peak load conditions. An energy storage system (ESS) is proposed as an intelligent active-management solution for mitigating voltage unbalance with high PV penetrations in LV distribution networks [10]. The authors showed that an ESS is capable of reducing the voltage unbalance factor as well as power losses in the networks. Some other methods for improving voltage unbalance are proposed and discussed in [11] where the authors firstly proposed increasing the cross-sectional area of feeders to reduce the voltage drop along the feeder. Since the distribution networks have already been constructed and are in service, it will not be economical to reconstruct the networks by

increasing feeder cross-section. Significant improvement in voltage unbalance can be achieved by the installation of capacitor banks in LV distribution feeders. It is shown that, with the help of proper operational commands for capacitor regulator, the voltage unbalance can be effectively improved by shifting the voltage profiles to within an acceptable range. Finally, the authors proposed to combine two techniques for improving voltage unbalance and found a significant improvement by this method compared applying those techniques separately. Two fundamental methods, namely on-load tap-changing (OLTC) and capacitor installation (either fixed or switched) are discussed for voltage regulation in LV distribution networks under high PV penetrations [12]. OLTCs are typically constructed as autotransformers with automatically adjusting taps and used to increase the voltage along the feeder under load. The permissible voltage increase provided by the OLTC for voltage regulation along the feeders is limited by the presence of loads (customers) near the OLTC. If there is a load near the OLTC, then first house protection is required to protect this customer from overvoltage [12]. On the other hand, due to the continuously varying nature of loads and PV penetration, fixed capacitors are not suitable for supplying the reactive power demanded by the load. OLTCs and switched capacitors are not suitable for voltage regulation along the feeder for such varying loads and variable PV penetration because they may not respond quickly enough to voltage variation. The possibility of inverters to support the necessary reactive power for voltage regulation is described in [12]. However, the IEEE 1547 standard, which is a guideline for interconnecting distributed resources with electric power systems, does not currently permit the PV inverter to actively regulate the voltage at the point of common coupling (PCC) [13]. Moreover, [12] also mentioned that the UL 1741 standard does not allow the inverter's participation in voltage regulation. The Australian PV Association has recently published a report [14] indicating that the AS4777 standard for grid connection of energy

systems via inverters recommends that inverters be set to operate at unity power factor. Due to the limitations imposed by AS4777, IEEE 1547 and UL 1741, PV systems are only designed to operate at unity power factor at present. At this point, researchers should look for intelligent controls for meeting the challenges of voltage regulation, voltage unbalance, overvoltage and phase balancing which occurs in LV distribution networks due to high PV penetrations.

Flexible AC Transmission System (FACTS) devices employing solid state electronics can respond almost instantaneously to manage voltage variation within the LV distribution networks. Specific FACTS devices include the Static Compensator (STATCOM), Dynamic Voltage Restorer (DVR) and UPFC. Recent research in LV distribution networks with PV are mainly focused on voltage regulation, voltage balancing, line loss minimisation, voltage profile correction and active filtering. The use of FACTS devices to mitigate those problems is being extensively studied. For example, the effectiveness of Distribution Static Compensator (DSTATCOM) and DVR devices are investigated for voltage unbalance reduction and voltage profile correction within LV distribution networks with high PV penetrations [15]. A UPFC is used as a centralised control device for simultaneously controlling all node voltages and line losses in a loop distribution system to ensure better service quality [16] where an electrolytic capacitor of about 3000 μF is used as a DC bus. These electrolytic capacitors are quite costly, large in size and often determine the working temperature of the converters. In addition, the failure rate of such capacitors is significant [17, 18].

Current research with UPFC is focused on the reduction of DC bus capacitance value to optimize its size, cost and lifetime. A UPFC with a three-leg parallel converter and a four-leg series converter, (3+4 leg UPFC) is proposed for LV distribution networks in [19]; this

work was based on simulations only conducted in Matlab Simulink which covered the following:

- A 3+4 leg UPFC was developed with a three-leg series converter and four-leg shunt converter which shared a common DC bus. This DC capacitor was proposed to be polypropylene or ceramic.
- Control strategies for voltage regulation and DC bus voltage control were developed.
- A degree of negative sequence current compensation was provided to remove 2ω oscillations from the DC bus.

This thesis is a systematic exploration and expansion of capabilities of an extended UPFC based compensator. A UPFC based on a four-leg shunt converter and a four-leg series converter, (4+4 leg UPFC), with reduced DC bus capacitance is introduced. This has a full range of series and parallel compensation duties and is a significant extension of the previous work [19]. This thesis includes results from a laboratory scale prototype for experimental verification. This thesis introduces new control features for series and parallel compensation using the UPFC based compensators. The addition of a fourth leg in the shunt converter provides an additional degree of freedom. The additional features covered in this thesis are:

- The sequence based synchronously rotating frame method is established to regulate the load voltages through a four-leg series converter and a series injection transformer.
- The zero sequence voltage compensation technique is established to remove the zero sequence voltage which appears at the output terminal during any unbalanced operation of the system.
- Active filtering capability of the UPFC shunt converter is explored to provide harmonic compensation.

- Zero sequence current compensation is established with the addition of a fourth leg in shunt converter.
- Reactive current compensation is provided which allows the power factor correction of the system.
- DC bus voltage control strategies are extended to cover the cases when the shunt converter is able to provide zero sequence, reactive current and harmonic current compensation.
- The instantaneous power flow analysis of UPFC are derived and presented for the 4+4 leg case.
- An equation is provided to calculate the DC bus capacitor size if the shunt converter is controlled to provide harmonic current compensation.

As the electrolytic capacitor of several thousands of microfarads is now replaced by a ceramic capacitor of tens of microfarads, the major research challenge is to control the 4+4 leg compensator and the DC capacitor voltage by ensuring instantaneous power balance for the input and output converters [20]. Figure 1.1 represents the basic schematic of a typical UPFC as presented in [21] redrawn with some modifications. It consists of a combination of two switching converters, i.e., series and shunt converters and the DC terminals of which are connected to a common DC bus capacitor. This UPFC arrangement can function as an AC to AC power converter where real power can freely flow in either direction between the AC terminals of the two inverters. Moreover, each inverter can independently generate or absorb reactive power at its own AC output terminal. The series converter performs voltage compensation duties by injecting AC voltage (v_C) with controllable magnitude and phase angle in series with the distribution feeders by means of a series transformer. The shunt converter provides the current compensation through the common

DC link to meet the power requirement by the series converter. It also regulates the DC bus voltage.

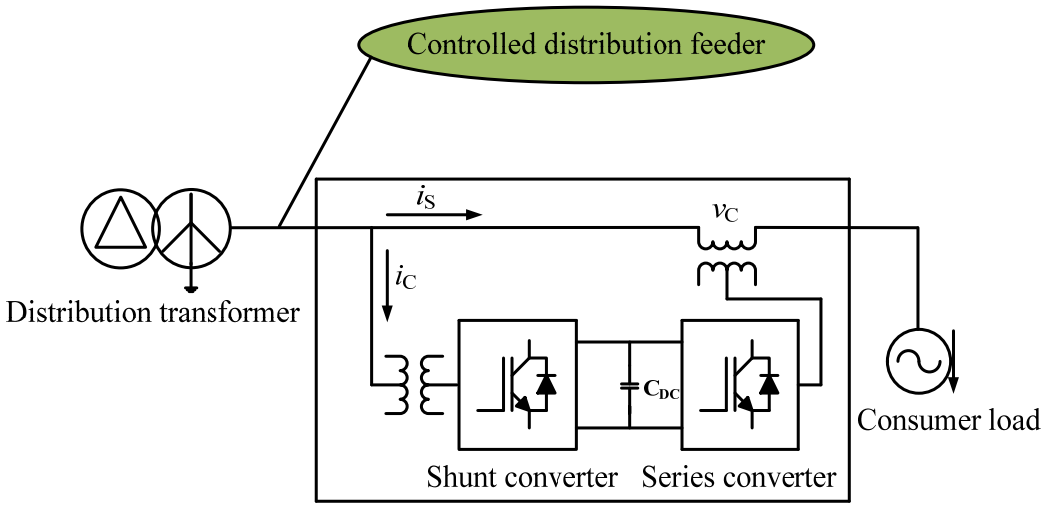

Figure 1.1 Schematic of unified power flow controller (UPFC) [21]

1.4. Aims and objectives of the research

The research program has the following central challenges:

- To develop control models based on averaged representations of the UPFC converters.
- To extend the instantaneous power balance analysis of UPFC with a view to controlling the DC bus voltages for the cases where the DC bus capacitors are small.
- To simulate suitable control models for the converters in the Matlab Simulink environment.
- To confirm the capability of a 4+4 leg UPFC based compensator to simultaneously provide voltage and current compensation for LV distribution networks with high PV penetrations by simulation.

- To build a laboratory scale 4+4 leg UPFC based compensator prototype for experimental works using commercial inverter module (STGIPL14K60).
- To develop the control software for the experimental tests of the 4+4 leg UPFC based compensator.
- To perform the experimental verification of the UPFC and its control algorithms on a laboratory scale prototype.

1.5. Organisation of the thesis

This thesis is organised into seven chapters. **Chapter 1** covers the general background, objectives and motivation of the research work. The potential contribution of this research is also discussed in this chapter. **Chapter 2** discusses the literature review which included the recent PV scenarios globally and in Australia, the benefits and impacts of high PV penetration in LV distribution networks and mitigation techniques. The research gap is also discussed in this chapter. In **Chapter 3**, modelling and control strategies of the proposed 4+4 leg UPFC are developed in the continuous time domain. The instantaneous power flow equation is also developed for three cases i.e., voltage regulation, active filtering and ancillary services. The simulation results are presented in **Chapter 4** and are divided into two sections. Section 4.3 discusses the results when the UPFC based compensator is applied in the LV distribution feeder for voltage regulation with only zero sequence current compensator. The simulation results are also shown when the UPFC is configured for voltage regulation with both zero sequence and reactive current compensator. Section 4.4 discusses the simulation results when the UPFC based compensator is applied in LV distribution networks for active filtering. **Chapter 5** describes the hardware design and construction for the project, the experimental system architecture and the filter design considerations for damping, the phase locked loop arrangement and the algorithm used for the 4+4 leg converter for modulation. The current, voltage and the DC bus voltage

regulation system architecture and their control systems are presented. The experimental results are also presented and discussed in this chapter. An overview discussion, conclusions and the directions of future work are presented in **Chapter 6**. Appendix A which records the details of the development boards including the experimental circuit board, schematic diagrams and the PCB layout of the development board is presented in **Chapter 7**.

1.6. Conclusion

This chapter covers the general background of distributed renewable energy systems and the potential contribution of PV energy in power generation. This chapter also discusses the challenges and probable implications for integration of high PV generation within LV distribution networks. A brief discussion is carried out into the merits and demerits of the possible solutions available for voltage management with distributed PV generation. A UPFC is proposed as a compensation device for mitigating potential complications faced by LV distribution systems having to cope with high PV integration. The major aims and objectives of the research are also presented in this chapter.

Chapter 2 LITERATURE REVIEW

2.1. Introduction

The installed capacity of PV systems globally reached 177GW at the end of 2014. The annual rate of installations, 38.7GW in 2014, continues to increase. A large part of this is installed as residential systems connected to LV networks. The majority of the LV distribution networks are radial, unbalanced with respect to loads and feeder structures and have high feeder line resistance to reactance R/X ratios. The large scale deployment of PV within the LV distribution networks is limited by voltage quality problems, particularly over voltages and unbalance. Development of proper mitigation techniques is essential to effectively and efficiently manage high penetration of PV within the LV distribution networks. A number of techniques have already been developed and implemented in LV distribution networks to alleviate those problems. This chapter provides an extensive review of the present status, impacts and technical challenges of PV penetration in LV distribution networks. In addition, the review comprehensively examines the commercially available and emerging mitigation methods and provides a framework that systematically explores the full range of technical methods and limitations for PV impact mitigation.

2.2. Recent historical advancement of cumulative PV installation

2.2.1. Global PV scenario

The global PV market has grown rapidly over the past decade at a steadily increasing rate which will lead to PV becoming one of the major sources of power generation for the entire world [22]. The global PV market had a record year in 2014, installing more capacity than any other renewables after hydropower while exceeding wind power [23]. Figure 2.1 shows the progress of cumulative installed PV capacity in the world over the period 2000-2014. A major portion of the total PV capacity is integrated with LV distribution networks in the form of rooftop domestic systems. According to the European

Photovoltaic Industry Association (EPIA) report, rooftop PV installations were more than 23GW in 2013 which exceeded the utility scale installations significantly [22].

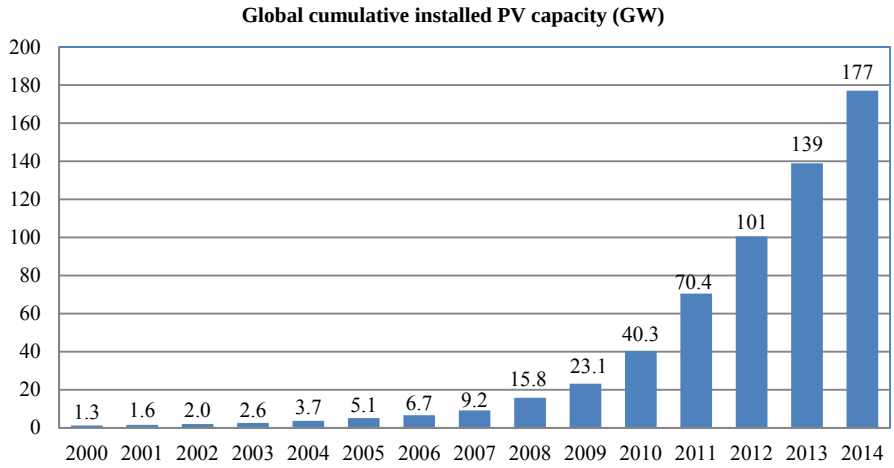

Figure 2.1 Progress of total global cumulative installed PV capacity (2000-2014) [3, 22]

Table 2.1 presents numerical data for actual cumulative PV installed capacity by region with global market share in 2013, and forecasts of those numbers for 2018. Europe is the world's leading region in terms of cumulative installed capacity with 81.5GW as of 2013 that represent about 59% of the world's cumulative PV capacity. However, the global market share of PV capacity in Europe is slightly down in 2013 from 70% in 2012 and about 75% of the world's capacity in 2011. Asia Pacific countries are also still growing fast, having about 21.9GW of cumulative PV installed capacity representing 16% of the world's capacity in 2013. China is in the top rank within the Asia Pacific countries, recording 18.6GW of cumulative installed capacity with 13% of market share in 2013. The Americas is improving its position compared to other countries in respect of cumulative installed capacity. The Americas achieved 13.7GW cumulative installed PV in 2013 which was a global market share of 10%. Several countries from large Sunbelt regions like Africa, the Middle East, South East Asia and Latin America are on the brink of starting their development. For example, the cumulative installed capacity outside Europe was 30GW in

2012, but doubled during 2013 to reach 60GW. This indicates the ongoing rebalancing between Europe and the rest of the world and closely reflects changing patterns in electricity consumption [22]. The share of PV installations outside Europe can only increase, ensuring the ongoing development of the PV market globally.

Table 2.1 Global PV cumulative installed capacity and market share per region in 2013 and forward forecasts

Region	2013		2014		2018	
	Installed capacity (GW)	Market share (%)	Installed capacity (GW)	Market share (%)	Installed capacity (GW)	Market share (%)
Americas	13.7	10	22	11	64.5	15
Asia Pacific	21.9	16	34	18	82	19
China	18.6	13	34	18	103	24
Middle East and Africa	0.9	0.6	3.8	2	21.5	5
Rest of World	2.0	1.4	1.90	1	4.3	1
Europe	81.4	59	95.3	50	155	36
Total	138.5	100	191	100	430.3	100

The data for 2014 and 2018 is based on EPIA's "high scenario" [22]

The combination of declining European markets and the possibility of establishing durable new markets in developing countries could cause this market to boom. As a result, the Asia-Pacific region, including China, should represent a major share of PV installations in the coming years under the EPIA's high scenario [22]. There is a possibility of reaching up to 430.3GW of PV systems within five years from 2013 for the best cases as compared to 138.9GW at the end of 2013.

2.2.2. Australian PV scenario

The Australian Renewable Energy Target (RET) has been established with the mandate of generating 20% or 45TWh of Australia's electricity supply from renewable energy sources by 2020 while reducing greenhouse gas emissions [24, 25]. A wide range of initiatives have been taken by several state governments to promote the installation of small scale PV in Australia. Feed-in tariffs (FIT) existed in the early stages of the development of the residential PV market. The RET currently provides installation rebates and encourages

investment in small scale installations, especially for solar PV and hot water systems in households [25]. The continuous rise in grid electricity prices and the various incentives provided by the state governments make PV a cost effective option for homeowners, as well as of increasing interest to the commercial sector across Australia [26]. Module prices continued to drop from 1.3 AUD/W in 2012 to around 0.75 AUD/W in 2013, and installed prices for small residential systems dropped from an average of around 3 AUD/W to around 2.50 AUD/W [26]. Over 1 million Australian homes now have a PV system, and residential penetration levels average 15% and are over 30% in some areas. The Australian Photovoltaic Institute (APVI) has recently reported that the small scale cumulative PV installed capacity has reached more than 4.5 GW in 2015 [4, 27] as shown in Figure 2.2. The growth in solar PV in Australia is quite significant. The cumulative installed capacity was about 1.39 GW in 2011 and reached 2.44 GW during 2012. However, the Australian PV market has contracted in 2013, with installation levels reducing from more than 1 GW installed in 2012 to around 850 MW [26].

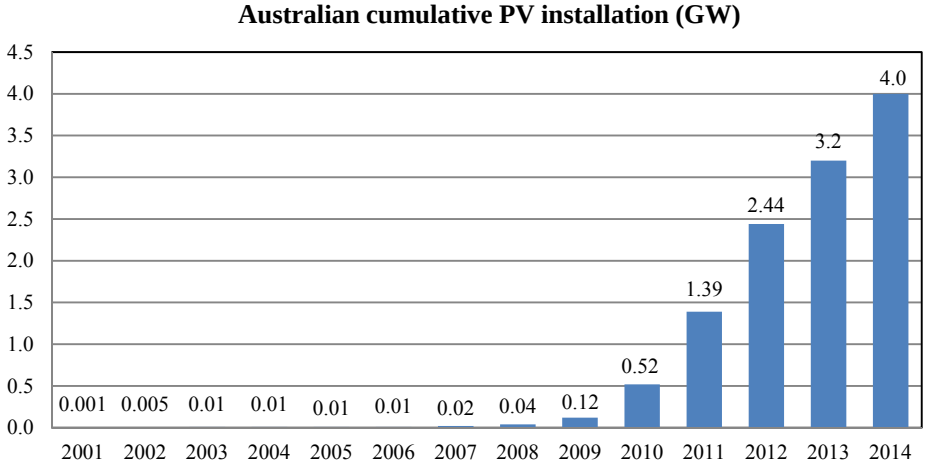

Figure 2.2 Progress of cumulative small scale installed PV capacity in Australia since April 2001 [4, 27]

The probable reason is the withdrawal of FITs by most State Governments. Electricity network operators also impose restrictions on further installations to cope with potential

issues arising from high penetration levels. According to a report of the APVI supported by the Australian Renewable Energy Agency (ARENA), PV system sizes have still continued to increase despite these restrictions on PV power exports to the grid and low or zero rates now paid for exported power [27].

2.3. Benefits of high Solar PV penetrations

The level of solar PV penetration signifies how much power from solar PV generation is contributed locally to meet the total loading of a distribution feeder. It is determined based on the total output from the distributed solar PV divided by the total loads on the feeder and represented as a percentage [28]. For example, the level of PV penetration for a 1.2MW residential rooftop PV would be 57.14% for a total 2.1MW loading system under maximum solar generation of 1.2MW. This means that 57.14% of the load demand is locally supplied by the distributed PV. However, the level of PV penetration may vary due to the variation in feeder loading conditions and the intermittent nature of PV generation throughout the day. It will be high during light load conditions while the solar generation remains high. However, the definition of PV penetration can be presented in some other forms. For instance, PV penetration is calculated based on the ratio of total peak PV power to peak load apparent power on the feeder in [29]. The authors in [30] extensively study the major benefits of PV. They declare solar PV as a clean, pollution free energy source which requires no maintenance other than occasional cleaning of the PV array. The potential benefits of grid-connected PV generation are discussed in [31]. Net load of an overloaded residential distribution feeder and distribution losses can be significantly reduced with PV penetration as reported in [31]. The impact of connecting solar PV generation units to a rural distribution system is studied in terms of voltage support, loss reduction and reduction in peak demand [32]. Simulation results demonstrate that, due to the PV penetration in distribution feeders, the voltage profile is improved and the

distribution losses are also reduced. The authors in [33] show that solar PV can significantly decrease the feeder losses by supplying power to provide some portion of load locally. However, the authors in [34] perform a survey of several aspects regarding both driving and inhibiting the acceptance of distributed generation. They claim that the distribution feeder losses for distributed generation are very time dependent and location specific. They also indicate that the distribution network behaviour completely depends upon the penetration level, and it is possible to accommodate 5% to 10% penetration of distributed generation without significant changes in feeder protection and voltage regulation devices. At a certain level of penetration, the assumption of unidirectional power flow through the network may break and the distribution networks may be reformed. However, the impact of moderate and high levels of PV penetration on a residential distribution feeder for two different loading scenarios has been investigated in [28]. Simulation results reveal that a moderate level of distributed PV penetration, for example, 57.14% and 21.81% for 2.1MW and 5.5MW feeder loadings respectively, gives better voltage regulation and reduces line losses considerably. With the increase of penetration level to 95.2%, the distribution network suffers for overvoltage that causes reverse power flow in the network. In addition, the feeder losses are also increased due to the high current in the feeder. On the other hand, the voltage unbalance factor mostly depends on the loading of different phases and the location of PV generation. Thus, it is obvious that the penetration level of solar PV is influenced by both geographical location of distributed PV and loading of the distribution feeder. There are some benefits with the integration of distributed PV generation in residential distribution feeders, but only up to a certain level of PV penetration. With increasing PV penetration above this level, the presence of distributed PV generation may result in power quality problems including overvoltage, voltage unbalance and reverse power flow which are problematic for the distribution

networks. Therefore, further investigation is required of these technical challenges to determine the acceptable limits of PV penetration within the existing distribution networks.

2.4. Impact of high PV penetrations in LV distribution network

A single line diagram of a typical residential LV distribution network [8] is shown in Figure 2.3. There is a distributed generator connected to the load side. In this figure, V_2 is the substation secondary bus voltage, X and R are the feeder line reactance and resistance respectively. LV distribution networks have some typical characteristics, i.e. high R/X ratio and unbalanced in nature. Due to the high R/X ratio, they are generally designed to have unidirectional power flow from upstream high voltage to downstream low voltage. The unbalance is mainly due to asymmetry in load currents and untransposed feeder impedances. This causes uneven voltage levels in each phase. As a result, LV distribution networks may encounter some technical challenges with high numbers of PV installed as domestic rooftop systems which can degrade the situation, leading to poor power quality.

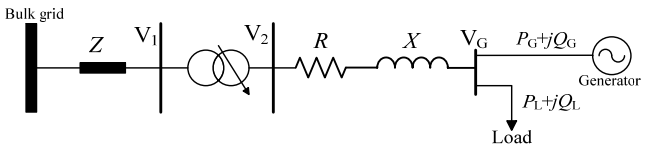

Figure 2.3 Single line diagram of a distribution network

A significant number of research papers have already been published to identify the potential challenges and impacts for integration of distributed generation resources in LV distribution networks [5, 6, 28, 29, 35-41]. Impacts of distributed resources integration to distribution networks were rigorously discussed and summarised accordingly to provide fundamental knowledge regarding voltage issues, protection issues and network issues which were reported as the major impacts [6]. Overvoltage is one of the most serious voltage issues that may occur when distributed resources are connected in small residential areas sharing a distribution transformer. Solar PV impacts on LV distribution networks

were studied and several major issues were identified, namely reverse power flow, voltage rise and voltage fluctuations, frequent operation of voltage regulation devices, reactive power fluctuations and increase in power losses [35]. Solar PV impacts on LV three phase distribution networks were investigated using a comprehensive assessment tool [5]. This investigation revealed that PV output at midday may significantly change the network behaviour in terms of voltage rise, voltage unbalance, reverse power flows and feeder losses. At midday during working days with peak PV output, feeder voltage profiles may improve at heavily loaded phases, but there is still the risk of voltage rise and reverse power flow at lightly loaded phases [5, 36]. Such voltage rise and voltage variation have a direct impact on network equipment. Voltage variations cause frequent operation of load tap changers (LTCs), line voltage regulators (VRs) and voltage-controlled capacitor banks for controlling the feeder voltage. This frequent operation shortens the expected life cycle of these devices and increases maintenance requirements. The voltage unbalance factor depends on how the solar PVs and loads are distributed in different phases of the LV distribution feeder [36]. Several studies were performed to determine factors limiting the level of photovoltaic penetration on distribution feeders and analyse their influence on network behaviour [29, 37, 38]. Voltage rise has been found to be one of the significant factors that limits the integration of high levels of solar generation into radial distribution systems [37]. Voltage variations were observed for different penetration levels and found to increase with the level of PV penetration into distribution networks [38]. Significant measures are required to mitigate such voltage variations. They cannot be mitigated with conventional LTC and capacitor banks. Studies were also carried out on the effects of high PV penetrations on residential distribution networks [28, 40, 41]. The majority of these papers have mentioned voltage regulation, voltage unbalance, reverse power flow and harmonics as the significant problems with high levels of PV penetration into LV

distribution networks. In this review, we will explore more details regarding voltage regulation and voltage unbalance issues because these severely affect the LV distribution networks as reported by much of the relevant literature.

2.4.1. Voltage regulation

Voltage regulation is one of the major concerns in LV distribution networks [42]. It is the utility's responsibility to keep the customers' service voltage within an acceptable range. Figure 2.4 shows an example of voltage limits for the primary circuit, the service entrance, and utilisation based on one utility's guidelines studied in [12]. The ANSI C84.1 standard provides guidelines for the normal and emergency ranges of nominal 120V power systems. The recommended service and utilisation voltage limits according to this standard are shown in Table 2.2. The primary voltage refers to the voltage at the input or primary side of the step down transformer at the customer load. The service voltage means the voltage at the customer's meter or PCC.

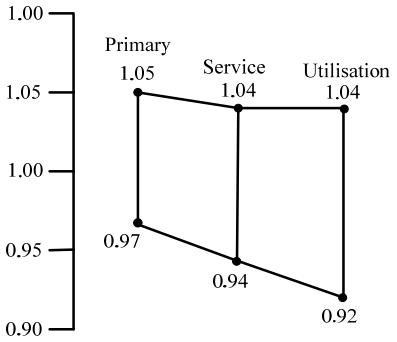

Figure 2.4 The voltage range used in [12]

Table 2.2 ANSI C84.1 Voltage Range for 120V voltage level [8]

	Service		Utilisation	
	Min	Max	Min	Max
Range A (Normal)	-5%	+5%	-8.3%	+4.2%
Range B (Emergency)	-8.3%	+5.8%	-11.7%	+5.8%

The utilisation voltage refers to the voltage at the point of use where the customer equipment is plugged in. According to the IEC 60038 international standard [43], the statutory tolerance range for voltage levels of a 230/400V system is -6% to +10% and the acceptable voltage band becomes 216.2-254V at the PCC. Based on IEC 60038, Australia has published the new AS 60038-2000 standard [33] which defines exactly the same voltage requirements as IEC 60038. In a geographically small area with high PV penetrations, voltage instability may arise from cloud induced voltage fluctuations [34]. This can become severe when cloud induced voltage fluctuations develop faster than the action of voltage regulators, and this may upset the operation of voltage regulation devices [44]. Frequent operation of the LTC reduces its life expectancy due to the significant increase in transformer tap changes. It is reported that distributed solar PV greatly affects the distribution feeder voltage regulation [42, 45-48]. One of the major factors affecting voltage regulation is reverse power flow which may occur more frequently in distribution feeders with the increasing level of PV penetration. This reverse power flow causes voltage rise which might lead to violations of voltage boundaries specified by ANSI C84.1. Moreover, the operation of voltage regulation devices such as on-load tap changers (OLTCs), static voltage regulators (SVRs) and switched capacitors (SCs) is affected by reverse power flow in distribution feeders. In addition, overvoltage limits the amount of active power injected into a LV distribution system [45] and reduces the efficiency of LV distribution networks. PV inverters may be able to provide feeder voltage support even at relatively high penetration levels, thus reducing the need for capacitors. Some technical solutions to mitigate the voltage rise problems include active power curtailment, energy storage to hold surplus power for later use, distributed generator's reactive power support, to reduce the substation tap changer set point, and to install autotransformers and voltage regulators along the line [39]. Active and reactive power controls can be applied for

voltage regulation, but reactive power control would not be as effective as active power curtailment for LV distribution networks due to the larger R/X ratio. For proper voltage regulation, a multi-agent cooperative control structure based on smart grid technologies is proposed [46]; the authors reported that traditional voltage regulation techniques using OLTCs, SVRs and SCs would create conflict among those devices due to the existence of distributed generation, and the multi-agent cooperative control structure would impact most positively with the increase of distributed generation penetration.

2.4.2. Voltage unbalance

Voltage unbalance is defined as the ratio of negative sequence to positive sequence voltage components and is represented in percentage terms as the voltage unbalance factor [49]. Voltage unbalance is regarded as a power quality problem of significant concern in LV distribution networks [50, 51]. Although the voltages are quite well balanced at the generator and transmission levels, the voltages at the utilisation level can be unbalanced due to the unequal system impedances and the unequal distribution of single-phase loads [50]. The increase in voltage unbalance can result in overheating and de-rating of all induction motor types of load and also distribution transformers [50, 52]. Voltage unbalance in LV distribution networks has several causes, including unbalanced loading in different phases, unbalanced solar generation and unequal system impedances, and the intermittent nature of PV [11, 36]. Voltage unbalance also depends on the location and rating of distributed PV. At the beginning of a distribution feeder, voltage unbalance is low and kept within the standard limit regardless of the number, location, and rating of installed rooftop PVs, but might increase at the end of the feeder to more than the standard limit [11]. Voltage unbalance is increased with unequal loading [36], and the worst condition is found for high load with no PV. However, voltage unbalance is improved significantly when equalising the feeder loads with the combination of medium load and medium PV.

Other scenarios such as high load with medium PV and medium load with high PV also encounter voltage unbalance problems. To address the voltage regulation and unbalance problems, traditional and commercially available approaches use network upgrading, OLTCs, fixed or switched capacitors and active power curtailment. Besides these traditional approaches, there are some emerging techniques proposed by researchers which include inverter-based reactive power control, use of energy storage and flexible AC transmission system (FACTS) controllers. Among the emerging methods, FACTS controllers are new technology based on power electronics to enhance power system capability through the provision of high-speed control [53, 54]. The FACTS devices offer fast response characteristics [55] and smooth control [56]. FACTS devices are being extensively studied with a view to deployment at LV distribution networks to achieve fast control of various parameters [15, 51, 57].

2.5. Commercially available mitigation methods

2.5.1. Reconductoring

The existing distribution networks can be reconfigured to improve the voltage profile by increasing the cross-sectional area of the feeders to a bigger size. The feeders with larger cross-sectional area have lower impedances. Figure 2.3 shows that this will reduce the voltage drop along the feeder. Resistance is inversely proportion to the cross section if skin effects are ignored. Reactance reduces, but at a much lower rate and depends on the logarithm of the conductor radius. Larger cross sections have an improved X/R ratio which will make capacitive voltage regulation methods much more effective. A stochastic analysis has been performed to verify the efficacy of this method for a distribution network of two different sizes of LV feeders which has shown that the feeder with the higher cross-sectional area improved the voltage unbalance [11]. Although upgrading the feeders is very effective for reducing the voltage drop and unbalance, it is a very expensive approach which is not usually justified due to low cost benefit ratios [8].

2.5.2. On-load tap changer

An OLTC is an essential part of distribution networks which is typically constructed as an autotransformer. Automatically adjustable OLTCs are commonly used at distribution substation to raise the starting voltage for a feeder under a load so as to keep the desired voltage along the feeder while compensating the feeder voltage drop [12]. The schematic of a common form of on-load tap changing transformer is shown in Figure 2.5. The secondary side voltage magnitude across the load changes depending upon the operation of tap changers. The control circuit measures the voltage and load current to estimate the controlled voltage at remote points. Depending upon the controlled voltage, the control unit initiates a signal to change the tap position of the transformer in order to restore the required voltage level. Each tap position corresponds to a voltage level. Depending upon the construction of the tap changing mechanism, the OLTC can be mainly categorised as conventional or electronic tap changers. In conventional OLTCs, moving mechanical parts are present which make the system more complex [58]. These moving mechanical parts are used for the purpose of changing tap positions.

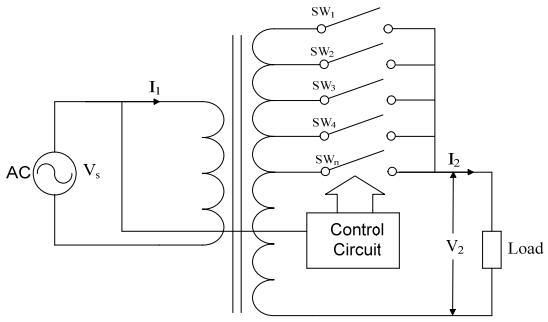

Figure 2.5 Schematic of a typical on-load tap changing transformer construction

The major drawback of these conventional OLTCs is a high response time in the range of 100ms to several seconds. Other disadvantages include arcing in the contacts of the diverter switches during the tap changing process, high maintenance and service costs, and high failure rates of tap-changers during operation [59]. These types of conventional OLTCs are not suitable for applications where quick and successive operations of tap

changers are highly desirable. For example, an OLTC requires fast operation in response to the quick succession of voltage variation that occurs at LV distribution networks with high solar PV penetrations. This frequent operation of the OLTC mechanism puts more stress on this type of voltage regulator and reduces the service life [8].

However, solid state OLTCs offer significant advantages over mechanical ones, namely improved performance and reduced maintenance costs due to the replacement of the mechanical tap changing mechanism with power electronic switches. The solid state OLTCs are built with modern power devices which can operate at high frequencies. Due to their fast response characteristics, OLTCs built with power electronic switches are treated as fast voltage regulators. This allows correcting several problems in the AC mains, such as sags and flicker. The insulated gate bipolar transistor (IGBT) can be a good candidate as a switch in high and medium frequency applications of power devices. In order to circumvent the limitations and drawbacks of conventional OLTCs, the solid state fast on-load tap changing transformer is proposed [60]. This topology is the direct replacement of existing classical OLTCs with an improved control circuit based on digital signal processor (DSP) and the modern power switches such as IGBTs as shown in Figure 2.6.

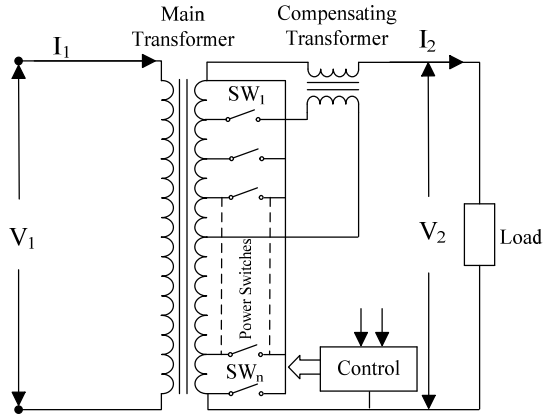

Figure 2.6 Schematic of a fast on-load tap changing transformer construction

This type of regulator provides the advantage of a fast response in order to correct other kinds of problems beside voltage sags in the AC lines. The experimental results revealed

that several disturbances such as sags, swells and flicker could be corrected with less response time than the conventional mechanical OLTC. There is still the need for further studies to allow higher switching frequencies and improve the response time of the regulator even more. Moreover, there are two major problems in solid state OLTCs, namely discontinuity caused by their stepwise controls and the limitation to the amount of switches. Recently, the on-load voltage regulator (OLVR) based on electronic power transformer (EPT) was proposed to achieve fast and continuous voltage regulation. A schematic of this device is shown in Figure 2.7 [59].

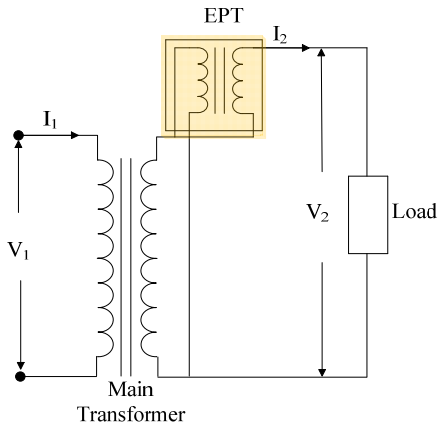

Figure 2.7 Schematic of a fast and continuous on-load voltage regulator based on EPT

This novel on-load voltage regulator based on electronic power transformer (OLVR-EPT) is designed to replace the conventional OLTC transformers and achieve fast and continuous voltage regulation. The resultant load voltage is maintained at the desired value by injecting an appropriate voltage component to traditional power transformer windings through the EPT output stage. The EPT, also called a power electronic transformer or solid state transformer, is a new type of power transformer which utilises the benefits of modern power electronics and the constantly improving high frequency magnetic materials. It is employed to eliminate the drawbacks of conventional copper-and-iron-based transformers such as high weight, sensitivity to harmonics, voltage drop under load, environmental concerns regarding mineral oil etc. The major objective is to replace all the line frequency

transformers. However, in this topology, the main role of an EPT is to serve as an auxiliary voltage regulator for line frequency transformer. This approach eliminates the need of mechanical tap changers and provides fast and continuous voltage regulation. Although this topology seems more attractive for voltage regulation and also power quality improvement, the cost, reliability and availability are expected to be the shortcomings of EPT technology.

2.5.3. Fixed or switched capacitor

Reactive power demand of the load can either be supplied from the substation side or by placing capacitor banks along the feeder. However, the ultimate benefit of supplying the reactive power locally to a consumer's load is the reduction of total current flowing through the feeder. This reduction of current lowers the feeder voltage drop and improves the voltage at the PPC. The capacitor banks may be either fixed or switched to supply variable reactive power according to the load demand. However, both the load pattern of LV distribution networks and the PV power output are variable. Thus, fixed compensation of reactive power is not a viable solution for voltage regulation. On the other hand, it is difficult to supply the exact reactive power demand by use of switched capacitors [12] because the reactive power demand varies continuously while the capacitor banks are only able to be switched in discrete steps. This may lead to overcompensation by the capacitors, causing voltage rise on the feeder. This requires an additional voltage regulator at the substation to lower the voltage to accommodate the voltage rise due to that overcompensation. Moreover, injected reactive power from the capacitor might drop at low voltage levels because it varies with the square of voltage. Due to these shortcomings, capacitor banks may not be a suitable option for voltage regulation in LV distribution networks with PV.

2.6. Emerging mitigation methods

2.6.1. VAR control of PV inverters

Utilisation of the PV inverter's reactive power capability is one of the emerging technologies to address the voltage regulation issue in LV distribution networks with high PV penetrations. The reactive power control capabilities of the PV inverter have been investigated to explore its possibility for participating in active voltage regulation in LV distribution networks [12]. A graphical representation which explains the reactive power control capabilities of grid connected PV inverters is shown in Figure 2.8.

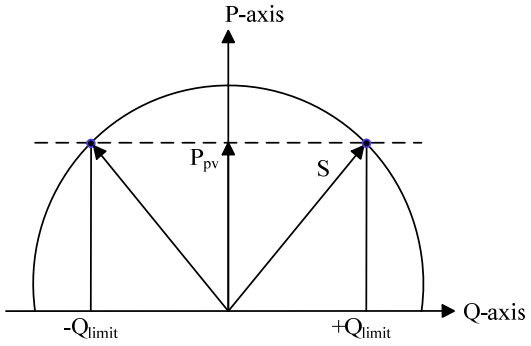

Figure 2.8 Reactive power control capabilities of grid connected PV inverters [61]

The PV inverter's ratings are represented by a vector with magnitude S. The boundary of the PV inverter's operating range is represented by the semicircle with radius S in PQ space. The power generated by the PV array, P_{pv}, is represented by the dotted line with two intersection points with the semicircle. The projection of the segment at both end points down to the Q-axis defines positive and negative reactive power limits as $+Q_{limit}$ and $-Q_{limit}$ which are determined by the inverter's rating, S, and real power, P, supplied by the PV array. There are two possibilities of operation, namely two quadrant operation and full four quadrant operation. For the unidirectional grid connected PV inverter without storage, two quadrant operation is possible and the inverter can utilise its entire rating to supply reactive power when there is no power from the PV array. The inverter will lose its reactive power supply capability when the real power produced by the PV array equals the inverter rating,

S. However, some reactive power capability can be retained by oversizing the inverter to allow more active and reactive power control capability [61]. The effective use of integrated energy storage with the solar PV inverter can allow full four quadrant operation [62]. In this latter article, four quadrant operation of integrated storage with solar PV inverter is discussed in detail. In addition to their continuous and variable reactive power support, inverters can operate quickly.

According to the IEEE 1547 standard which is a guideline for interconnecting distributed resources with electric power systems, PV inverters are not permitted to actively regulate the voltage at the PCC [13]. Moreover, several other standards, i.e. UL 1741 [12] and AS4777 [14], do not allow the inverters to participate in voltage regulation. The National Renewable Energy Laboratory (NREL) [12] reported that this restriction is not a technical one, rather a matter of agreement with the customer not to allow decentralised voltage regulation. In recent times, some literature [61, 63-69] has proposed voltage control in distribution systems by using the reactive power capability of inverter based distributed generators. A comprehensive PV control strategy has been proposed based on the optimal reactive power control and real power curtailment of single-phase inverters to improve the operational performance of significantly unbalanced four-wire LV distribution networks in [61]. Decentralised voltage control for distribution systems with inverter based distributed generators has been proposed in [63] and shown capable of maintaining the voltage within regulatory limits while producing maximum available active power. Those authors also reported that this system can avoid the disconnection of distributed generators due to violations of voltage limits. The effectiveness of distributed generators as a reactive power source has been presented in [64]. This work did not consider the variable nature of load and distributed generation. A reactive power control scheme with inverter reactive power support has been developed in [65]. The authors in [69] proposed a unified VAR controller

for voltage regulation and islanding detection with both functions integrated into a PV inverter based on reactive power control to address system voltage issues. They theoretically showed that these two features, voltage regulation and islanding detection, can be integrated in the PV inverter by means of real and reactive power control. Thus, reactive power control utilising PV inverters can be an attractive means of voltage regulation in LV distribution networks. Many current national standards require changes to allow reactive power control and this is under consideration in many nations.

2.6.2. Distributed energy storage systems

Batteries are often proposed as energy storage systems and will become more widely applied as battery technologies and economics improve [70]. Energy storage allows integration of intermittent renewables generation by smoothing their energy output over time. As a result, utilities can use existing infrastructure and energy resources efficiently to provide a reliable source of high quality electricity to customer premises. Battery energy storage can be applied in various operational modes. In a “load levelling mode”, energy is stored in the battery banks when the grid power exceeds the load demand and this stored energy is supplied when the demand exceeds the grid power. In an “arbitrage mode”, energy is purchased off-peak at lower prices from the grid, stored in the battery banks and then utilised at the peak time or when the grid power is costly. In an “export curtailment mode”, excess solar generation from the solar PV is stored in battery storage at the customer premises and no export to the grid is allowed, preventing voltage rises. In this case, customers may be allowed to fit a much larger solar array if this voltage problem is actively prevented. Apart from batteries, ultracapacitors (U-Cap) can be used to store moderate amounts of energy without chemical reactions during the process. This allows for a very large number of charging/discharging cycles. Ultracapacitors have larger power density compared to batteries. The dominant ultracapacitor technology is the electrochemical double layer capacitor (EDLC), but in many instance costs are prohibitive.

A comparison of ultracapacitors, Li-ion batteries and other battery energy storage devices is shown in Table 2.3. Lead-acid is the most commercially mature rechargeable battery technology in the world and has been used as an energy storage device from the beginning of eighteen century [71]. Although lead acid batteries have comparatively low energy density and a limited life cycle, they are still prevalent in cost-sensitive applications including automotive, marine, telecommunications, and UPS systems [72]. Recent advances aim to replace lead with lighter materials such as carbon to increase power and energy density.

Table 2.3 Comparison between different energy storage devices [70, 73]

Energy storage device	Energy density (Wh/kg)	Power density (W/kg)	Cycle Life
Li-ion	150-250	180	1200
Lead-Acid Battery	30-50	100-200	200-300
NiMH Battery	60-120	250-1000	300-500
Zinc-Bromide Battery	85-90	300-600	2000
Ni-Cd	40-60	150	1500
Na-S	150	-	-
Li-Ion U-Cap	10-20	900-9000	>100000
EDLC	2-8	500-5000	>100000

The high energy density and relatively low weight of lithium ion (Li-ion) systems make them an attractive choice for areas with space and weight constraints. In addition, Li-ion batteries have a low self-discharge and no memory effect. The current applications include portable electronic devices such as laptops, cameras, mobile phones, military equipment, energy reserve, aerospace industry and hybrid electric vehicle technology [74]. Li-ion is being positioned to be the leading technology platform for plug-in hybrid electric vehicles and all-electric vehicles [71, 72]. Due to high conversion efficiency, compactness and attractive cycle life, Li-ion batteries are also being seriously considered for several utility grid-support applications such as community energy storage, transportable systems for grid-support, commercial end-user energy management, home back-up energy management systems, frequency regulation, and wind and photovoltaic smoothing [75].

Advanced wall mounted, rechargeable Li-ion batteries with liquid thermal control are available for daily cycle and back up applications with single and three phase utility grid compatibility [75]. Hydrogen build up in nickel–metal hydride (NiMH) batteries during charging at an excessively high charge rate may cause the cell to rupture. The relatively high self-discharge rate makes NiMH batteries unsuitable for automotive applications [76]. Nickel-cadmium (NiCd) batteries have a higher energy density and longer cycle life than lead acid batteries, but are inferior to other battery chemistries. Other disadvantages of NiCd batteries compared to NiMH include shorter life cycle, memory effect, toxicity of cadmium that requires a complex recycling procedure, lower energy density, flat discharge curve, and negative temperature coefficient that may cause thermal runaway in voltage controlled charging [70]. Sodium-sulphur (NaS) batteries exhibit several advantages such as high power and energy density, good temperature stability, long cycle life, low cost, and good safety [77, 78]. NaS batteries are a commercial energy storage technology finding applications in electric utility distribution grid support, wind power integration, and high-value service applications on islands. The round-trip AC-to-AC efficiency of NaS battery systems is approximately 80% [71]. Battery storage has been proposed to store surplus power during peak solar generation for voltage rise mitigation and evening peak support [62]. A detailed charging and discharging control strategy was developed to effectively utilise the capacity of the battery storage. However, battery storage is still currently very expensive and the cost benefit ratio can be low if they have to be sized to store the PV generation surplus [79].

2.6.3. Coordinated control between utility equipment and PV inverter

A coordinated control between utility equipment such as OLTCs, SVRs and SVCs, or between that utility equipment with PV or energy storage systems (ESSs) can be an option for the mitigation of voltage regulation issues in LV distribution networks. The coordinated control of a distributed energy storage system with OLTCs has been proposed

for voltage rise mitigation under high PV penetrations as shown in Figure 2.9 [8]. The major objective of this coordinated control is to reduce the level of OLTC operational stress, shave the distribution network peak load and decrease the transmission and distribution resistive power losses under high solar power penetration.

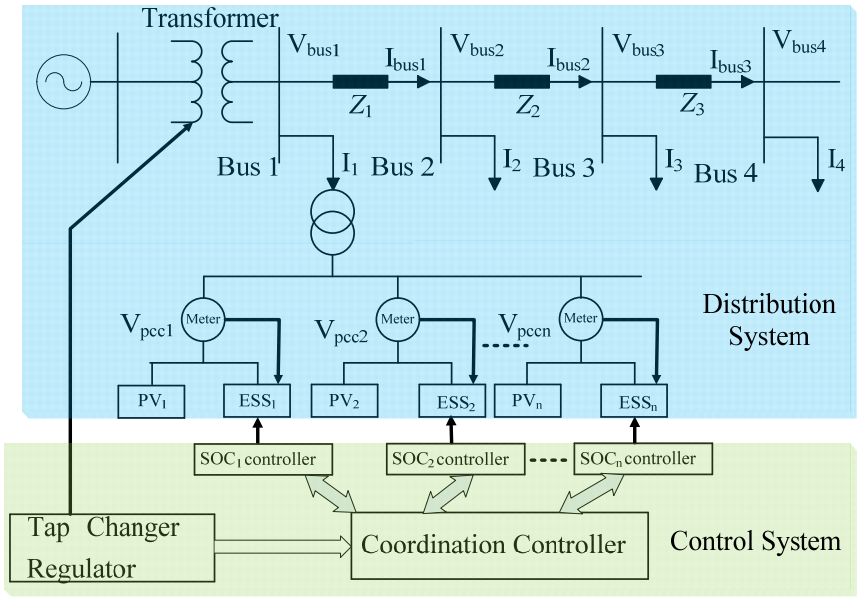

Figure 2.9 Coordinated control of distributed ESS with tap changer transformers for voltage rise mitigation [8]

In this coordinated control strategy, during off-peak hours when voltage rises occur, the centralised coordination controller sends coordination charging signals to the distributed ESS state of charge (SOC) controllers to start charging the battery storage for absorbing the reverse power flow. This will then reduce OLTC operational stress. During the peak hours, the centralised controller sends a coordinated discharge signal to the distributed ESS to start discharging the battery storage to shave the grid peak load. Simulation results revealed that the proposed method can reduce the switching operation times and stress of OLTCs in coordination with ESS. Coordination between OLTCs and SVCs has been proposed for voltage regulation in unbalanced radial distribution systems with PV generation [80]. The network uncertainties regarding network impedance, loads and generation were not taken into consideration. Furthermore, the proposed approach takes

less than 1 minute. Some scenarios were investigated by allowing the PV inverter to control the voltage at PCCs with traditional voltage regulators such as OLTCs and switched capacitors [81]. Voltage regulators could experience more frequent operation if they are not properly designed and coordinated. Effective control requires the development of an appropriate algorithm for the coordinated voltage control in existing LV distribution networks before allowing multiple PV plants to control the voltage at multiple PCC interconnections. Coordinated voltage control approaches have been proposed to regulate voltage in a distribution feeder with the coordination of OLTC, voltage regulator and distributed PV [82, 83]. Simulation was carried out on an Australian distribution feeder [82] and significant improvements achieved in terms of system voltage recovery time and voltage regulator operational stress.

2.6.4. Dynamic voltage restorer

The dynamic voltage restorer (DVR) is a power electronic converter based series compensator that can protect critical/sensitive loads from most common supply side disturbances other than outage [51, 84]. A DVR is realised as a voltage source inverter (VSI) where the output of the VSI is connected in series with a distribution feeder.

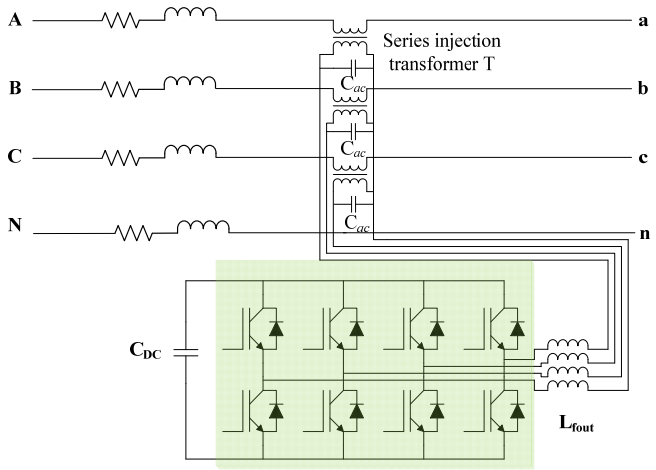

Figure 2.10 Schematic of a DVR connected to a distribution network

The basic function of the DVR is to regulate the voltage at the load terminal irrespective of sag/swell, distortion, or unbalance in the supply voltage by injecting a voltage of the required magnitude and frequency. A DVR can regulate the load voltage at any given magnitude and phase angle, but is subject to any limits in energy storage that are imposed at the DC bus. A real power exchange between the DC source and the AC system through the inverter would be required to, for example, regulate the positive sequence voltage over time. A DVR may be able to eliminate negative sequence voltages and harmonics without exchanging a significant amount of real power. The schematic of a DVR connected to a distribution network is shown in Figure 2.10. It contains a series inverter that is connected to a common DC storage capacitor, C_{DC}. The voltage, V_{dc} across this capacitor is the DC supply voltage input to the inverters. The output of each inverter leg is connected to a single-phase transformer with a secondary connected in series to the three phases of the distribution feeder. A DVR was proposed for the compensation of distribution system voltage in [85]. Simulation results confirmed the operation of the DVR as a voltage regulator, voltage restorer and voltage conditioner. However, the ideal DVR may not be able to suppress the voltage transients for nonlinear loads unless a low impedance path is provided from the PCC to ground [84]. In this latter article, a capacitor supported DVR is proposed for the protection of unbalanced and distorted loads. This capacitor is connected between the load and ground. Hence, the success of the DVR is often limited by the choice of an appropriate filter capacitor. A four-wire dynamic DVR using a three-phase split capacitor VSI was proposed in [86]. A three-dimensional voltage space vector PWM algorithm was used for the control of a three phase four-wire inverter. According to the simulation, a DVR using a three-phase split capacitor VSI was to be shown capable of effectively injecting three independent voltages in series with the line to maintain a desired voltage at the sensitive load. Use of a DVR has also been proposed for the mitigation of

voltage sags [87-90]. A DVR was recently applied in LV residential feeders with rooftop PVs for voltage profile and voltage unbalance improvement [15] with relative comparison made between the performances of the DVR with a distributed static compensator (DSTATCOM) in terms of voltage unbalance reduction capability. A conclusion was made that the DVR is not as successful as the DSTATCOM in terms of unbalance mitigation performance, but requires a much smaller rating than the DSTATCOM.

2.6.5. Distributed static compensator

The DSTATCOM is based on a solid-state voltage source implemented with an inverter and connected in parallel to the PCC of a distribution system for voltage regulation [51]. Usually, this device is supported by energy stored in a DC capacitor. When a DSTATCOM is associated with a particular load, it can inject compensating current so that the total demand meets the specifications for utility connection. The general arrangement is as shown schematically in Figure 2.11. A DSTATCOM has been studied for system voltage control with reactive power compensation during peak solar irradiation in order to increase the PV installation capacity of a distribution feeder [91]. With increasing DSTATCOM size, the PV installation capacity can be significantly increased. DSTATCOMs with reduced DC bus capacitance have been applied to improve the PV penetration limits in LV distribution networks in [92].

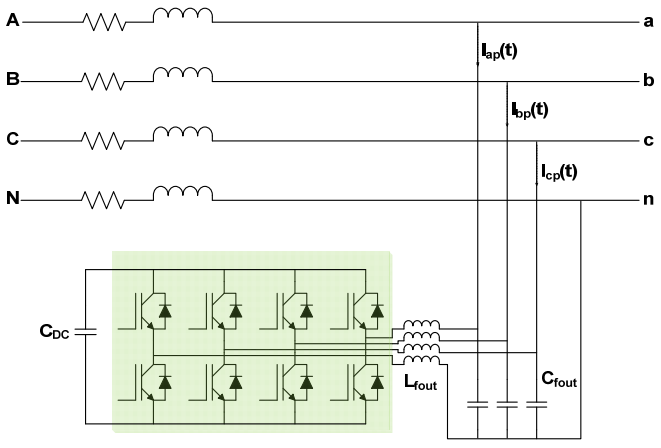

Figure 2.11 Schematic of a DSTATCOM connected to a distribution network

This can be designed with low value DC bus capacitance if appropriate limits are imposed on the negative sequence current. However, a significant portion of zero sequence current still flows through the input terminal. Thus, the DSTATCOM is not able to compensate the zero sequence current from the input terminal. A DSTATCOM was proposed for voltage profile and voltage unbalance improvement in LV residential feeders with unequal distribution of single phase rooftop PVs [15]. The placement of a DSTATCOM along the distribution feeder has a direct impact on the voltage unbalance factor. It was shown that the DSTATCOM has better results for voltage profile improvement and voltage unbalance reduction. A general recommendation is that a DSTATCOM should be installed at the 2/3rd point from the beginning of the feeder to have better results in voltage unbalance reduction along the feeder. In addition to this, some DSTATCOM applications need auxiliary devices, for example a zig-zag transformer for neutral and harmonic current compensation in LV distribution networks [93].

2.6.6. Unified power flow controller

A UPFC consists of two switching converters operated from a common DC link provided by a DC storage capacitor [94, 95]. One connected in series with the line is designated as a series converter, while the other in parallel is called a shunt converter. This arrangement, shown schematically in Figure 2.12, functions as an ideal AC to AC power converter in which the real power can freely flow in either direction between the AC terminals of the two inverters, and each inverter can independently generate or absorb reactive power at its own AC output terminal. The series inverter provides the main function of the UPFC by injecting an AC voltage, v_{Aa}, with controllable magnitude, $v_{Aa}(0 \le v_{Aa} \le v_{Aa\max})$, and phase angle, $\phi(0 \le \phi \le 360^{\circ})$, at the power frequency in series with the line via a series injection transformer.

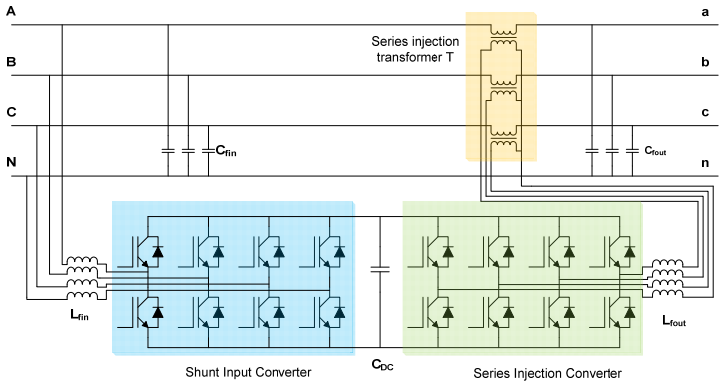

Figure 2.12 Schematic of a UPFC connected to a distribution network

A basic function of a shunt inverter is to supply or absorb the real power demanded by the series inverter at the common DC link. The shunt inverter can also generate or absorb controllable reactive power, and can thereby provide independent shunt reactive compensation for the line. A UPFC has a capability that includes voltage regulation, series compensation, phase angle regulation and multifunction power flow control [94]. A UPFC with reduced DC bus capacitance has been proposed to mitigate voltage regulation and voltage unbalance problems in LV distribution networks with high PV [90]. This proposed UPFC can effectively regulate the output voltage and shows no variation in voltage magnitude between different phases at the output. Such a UPFC has been shown capable of simultaneously regulating all nodes voltage and line losses in loop distribution systems [16]. However, this work was mainly focused on voltage regulation and line loss minimisation in a loop distribution system, and the effect of inclusion of distributed generation in the distribution system was not considered. A linear and sliding mode control strategy for a matrix-converter based UPFC (MC-UPFC) has also been proposed [96]. Simulation results demonstrated that the active and reactive power can be effectively controlled using the MC-UPFC with any one of the following controllers, namely a direct power controller (DPC), a decoupled linear controller, or a simple proportional controller. However, the DPC achieved the best result and showed no steady-state errors, no cross coupling, a fast response time (<1ms) and low third harmonic distortion. A comparison has

been performed between a DSTATCOM and UPFC based on the voltage regulation and location [97]. Optimum voltage regulation is found when the UPFC is connected near the receiving end, and with the DSTATCOM at the middle of transmission lines. Recently, the effects of different types of FACTS devices on the steady-state performance of the Hydro-Québec power system network has been analysed and compared to those of a STATCOM with energy storage (SMES) from the viewpoints of static loadability and losses [98]. In this analysis, it was found that a UPFC is the most effective FACTS device which could simultaneously increase loadability while reducing the losses for power transmission networks. Still, there is a need for investigating the capabilities of a UPFC at the distribution level.

2.7. Converter topologies

FACTS devices such as DVRs, DSTATCOMs and UPFCs are power electronics converters which are generally realised by three phase voltage source converters (VSC). Three-phase VSCs can be connected in two ways to provide a neutral connection for three-phase four-wire systems [99]. One way to do this is to use a four-leg converter topology and tie the neutral point to the mid-point of the fourth neutral leg. The other way is to use split capacitor topology where the DC link capacitor is split into equal halves and the mid-point of the DC link capacitor is tied to the neutral point. These two topologies are shown in Figure 2.13 and Figure 2.14 respectively.

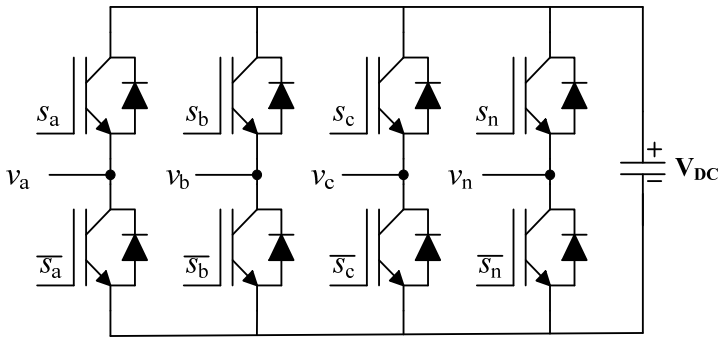

Figure 2.13 Four-wire four-leg topology [100]

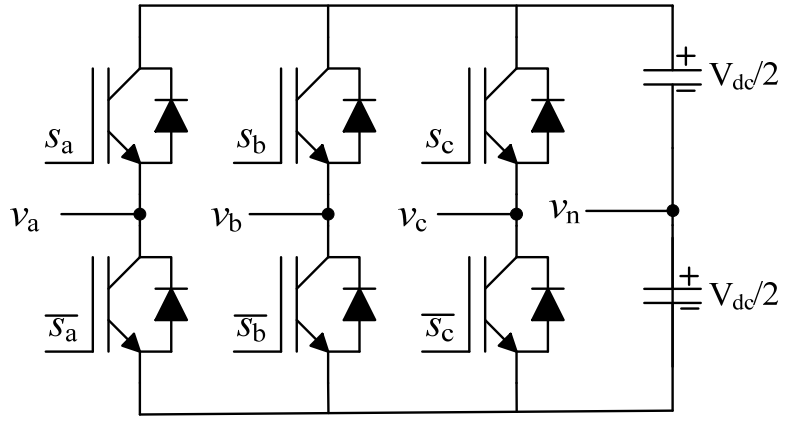

Figure 2.14 Four-wire three-leg with split capacitor topology [100]

However, the split capacitor topology suffers from insufficient utilisation of the DC link voltage. In addition, large and expensive DC link capacitors are needed to maintain an acceptable voltage ripple level across the DC link capacitors in case of a large neutral current due to unbalanced and/or nonlinear load [99, 101, 102]. A three-leg VSC based DSTATCOM with a zig-zag transformer is implemented for reactive power compensation, voltage regulation, neutral current compensation and harmonic current elimination at the PCC [93]. In this case, the zero sequence and harmonic current are compensated at the cost of the zig-zag transformer. As a result, there is a growing interest in four-leg converters for three phase four-wire applications [99-101, 103]. This is finding a wide range of applications in distributed generation, active filtering, common mode noise reduction and three phase PWM rectifiers. In distributed generators, this is very crucial for providing a three-phase output with a neutral connection, and thus neutral current compensation produced by impedances imbalance, unbalanced and/or nonlinear loads [99]. Four-leg converters are used in active filtering for compensating the harmonic current through the neutral point, and in three-phase PWM rectifiers for providing flexibility to deal with line distortion and imbalance, as well as provide fault tolerant capability.

2.8. Inverter with reduced DC bus capacitance

The uses of power electronics in the form of FACTS devices are increasingly common and play a key role in transmission network control while, at the distribution level, these are much more limited [104]. A near-term need for utilities is cost effective distributed voltage control at the grid edge. Among the FACTS devices, UPFCs are shown to be effective in providing several functions such as voltage regulation, voltage unbalance, power factor correction and neutral current compensation [105]. Still, it is an expensive approach because of the large value of DC bus capacitors and high power switches. Normally, three-phase VSIs utilise a DC bus provided by conventional electrolytic capacitors [18]. These electrolytic capacitors are one of the major components affecting the volume and cost of UPFCs [106] . The presence of these large capacitors in the DC bus, although giving better voltage stability, produces harmonic distortion in the input currents and in the line voltage.

These capacitors are bulky and make the inverter less reliable due to their short life expectancy [17]. Electrolytic capacitors occupy approximately 35-40% of the whole inverter volume and weight while contributing 23% to the total inverter cost [107]. One way of reducing the size and cost of UPFCs is reduction of the DC bus capacitance value which can be done by replacing the electrolytic capacitor with polypropylene or ceramic versions. There is an increasing interest in replacing these capacitors with non-polarised capacitors [108-116]. A comparative study of aluminium electrolytic capacitors, multilayer monolithic ceramic capacitors and film capacitors has been presented [117]. The ceramic capacitors provide the best performance due to their lowest equivalent series resistance (ESR), high ripple current capability, high volumetric efficiency and a temperature withstanding capability higher than 150^0C. Although aluminium electrolytic capacitors have higher capacitance per unit volume than ceramic capacitors, they suffer

from the drawbacks of high ESR and low ripple current capability. It is possible to replace the conventional bulky electrolytic capacitors with polypropylene or ceramic capacitors.

However, a small DC-link capacitance leads to large voltage fluctuation. For example, if a non-negligible active power flows into the DC-link capacitor, the DC-link voltage would rapidly rise and overvoltages would appear across the DC-link capacitor. Fast power-flow control in a UPFC causes fluctuation of the DC-link voltage [21]. The required capacitance of the DC-link capacitor should be appropriately designed to avoid overvoltage. If electrolytic capacitors with thousands of microfarads are replaced by ceramic capacitors of tens of microfarads, this will significantly reduce the total cost for UPFCs. In this case, the major research challenge would be to manage the DC capacitor voltage by ensuring instantaneous power balance for the input and output converters of the UPFCs.

2.9. Research gap

In this chapter, voltage management philosophies for distribution networks with PV are divided into two categories, namely commercially available and emerging trends. The commercially available methods for voltage management include reconductoring, OLTCs, fixed or switched capacitors and active power curtailment. Upgrading the feeder size would be a very attractive solution for voltage regulation, but it is a very expensive approach that involves massive labour costs and service disruptions. Several types of OLTCs have been proposed to date, and these are mainly categorised into three major topologies in this paper. The conventional OLTC topology shown in Figure 2.5 that involves the mechanical switches is not a preferable choice for voltage regulation in LV distribution networks for many reasons. For example, the conventional OLTC needs to operate more frequently to correct the load voltage due to the intermittent nature of PV. Such frequent operation would increase the stress and reduce the service life of the OLTC switching mechanism. Additionally, the response time for switching is very slow,

approximately in the range of hundreds of milliseconds or even seconds. The second topology shown in Figure 2.6 is proposed as a fast on load voltage regulator which replaces electromechanical switches with solid state power electronics switches. This topology reduces the response time significantly, but still needs further development for improving switching frequencies and the response time even more. The most recent topology of Figure 2.7 studied in this paper aims to replace OLTCs with an electronic power transformer. As a result, this topology eliminates the need for mechanical switches as well as power electronic switches and is expected to provide very fast and continuous voltage support. This topology becomes more attractive and performs better than the other two topologies, but the cost, reliability and availability seem to be the shortcomings of the EPT.

Another commercially available method for voltage regulation is fixed or switched capacitor banks. The reactive power demand of residential load varies continuously due to the inclusion of PV in LV distribution networks. Attempting to meet such a variable power demand, these capacitors sometimes cause overcompensation and thus lead to overvoltage. On the other hand, active power curtailment is very effective for overvoltage prevention by limiting power export to the grid. But this is not an economically attractive solution and lost revenue leads to dissatisfaction of the customers. The PV inverter's reactive power support is gaining more attention and becoming one of the emerging technologies for overvoltage prevention, voltage regulation and power factor correction. It is well known that grid connected PV inverters have continuous reactive power control capabilities. It is theoretically established that two quadrant operation is fully achievable with PV inverters, while four quadrant operation is possible with energy storage. The current requirements of the IEEE 1547, UL 1741 and AS4777 standards impose restrictions on PV inverters, preventing these from participating in voltage regulation at PCCs. It is expected that the restrictions will be withdrawn or modified over time. The inverters can then become an

effective means for continuous voltage regulation. Use of energy storage is another alternative to emerging technologies for voltage rise mitigation. This can have three different operational modes, namely load levelling, arbitrage mode and export curtailment mode. In arbitrage mode, energy is purchased at off-peak and utilised during peak hours. Different types of battery energy storage are available. The lead acid battery is a mature and still very cost effective technology but suffers from low energy density and limited service life. In contrast, the Li-ion battery is expected to be the most useful for grid connected integrated PV systems due to its high energy density, compactness and attractive life cycle. However, the cost is still a barrier to practically incorporate the energy storage systems with PV. The major challenge of the coordinated control topology of Figure 2.9 is the proper coordination of the PV inverter and traditional voltage regulating devices such as OLTCs, SVCs, SVRs and switching capacitors. Incorrect coordination may lead to an excessive operation of voltage regulators whereas our main objective is to reduce the operational stress of these devices.

Although, the FACTS controllers are already a familiar and mature technology for power system transmission network control, their application at the distribution level is very limited. In addition to this, very little literature exists on FACTS controllers for voltage regulation in radial distribution systems with high PV penetrations. Research is ongoing to incorporate these high speed power electronics based controllers at the distribution level to manage end-user voltage problems. Among the three members of the FACTS family, DSTATCOM is easily installed as a shunt device. There are some functional limitations of three-leg DSTATCOM which requires extra devices to provide harmonic and neutral current compensation. These limitations are removed by four-leg DSTATCOM designs. The UPFC is shown to be effective for achieving several functionalities together. This is shown capable of effectively regulating positive sequence voltage and voltage unbalance

issues, while simultaneously providing neutral current and harmonic current compensation and power factor correction without any ancillary devices.

2.10. Conclusion

PV is one of the favourable renewable energy resources and is becoming increasingly attractive to customers to satisfy their electricity demand in parallel with the grid power. The present status of PV globally and its associated impacts are reviewed. A significant part of the large installed PV capacity is connected to existing distribution networks as residential systems. As a result, existing networks suffer from several technical issues such as reverse power flow, overvoltage, voltage unbalance etc. This requires quick corrective measures to keep the customer supply voltage within acceptable limits. A variety of methods which have been proposed in recent publications for mitigation of voltage problems in LV distribution networks are reviewed in this chapter. Different mitigation methods are categorised into two groups, namely available mitigation methods and emerging mitigation methods. The commercially available mitigation methods are not effective in alleviating those problems due to the inclusion of PV which is naturally intermittent. The emerging mitigation methods mainly include VAR control of PV inverters, distributed batteries and FACTS controllers. Of these, FACTS controllers seem to be more effective, particularly the UPFCs, and a review of the other two methods shows VAR control of PV inverters is restricted by the current practice of the applicable standards and distributed batteries are very expensive.

Chapter 3 MODELLING & CONTROL STRATEGY FOR A UPFC

3.1. Introduction

The modelling and control strategies of the proposed UPFC based 4+4 leg compensator are presented in this chapter. In the proposed compensator, the DC bus capacitor sizes are reduced to allow the application of a non-polarised ceramic or polypropylene capacitor in place of the conventional electrolytic capacitor. The proposed UPFC based compensator is designed to provide voltage and current compensation for voltage regulation, voltage unbalance correction, neutral and reactive current compensation and active filtering in LV distribution networks. A continuous time domain simulation model is developed to confirm the operation of the proposed UPFC based compensator. Voltage control and power control schemes for both series and shunt converters are separately addressed and discussed.

3.2. Four-leg reduced DC bus capacitance UPFC

The four-leg distribution level 4+4 leg UPFC based compensator with reduced DC bus capacitance is shown in Figure 3.1. The UPFC consists of two four-leg switching converters i.e. a shunt converter and series injection converter operated from a common DC bus. This DC bus is provided by a DC storage capacitor which has a reduced value in this case. The series injection transformer is connected in series with the distribution feeder. The series injection transformer provides an AC voltage, v_s with controllable magnitude and phase angle in series with the line to allow voltage regulation and balancing by the action of voltage compensation. A shunt input converter supplies or absorbs the real power demanded by the series converter at the common DC bus. The shunt input converter can generate or absorb controllable reactive power, and thus can provide independent shunt reactive current compensation for the distribution feeders. Thus, the shunt converter can be

operated either at a unity power factor or be controlled to have a reactive power exchange with the line independently of the reactive power exchanged by the series converter [94]. The four-leg shunt converter can also draw zero sequence current, harmonics current for zero sequence and harmonic current compensation.

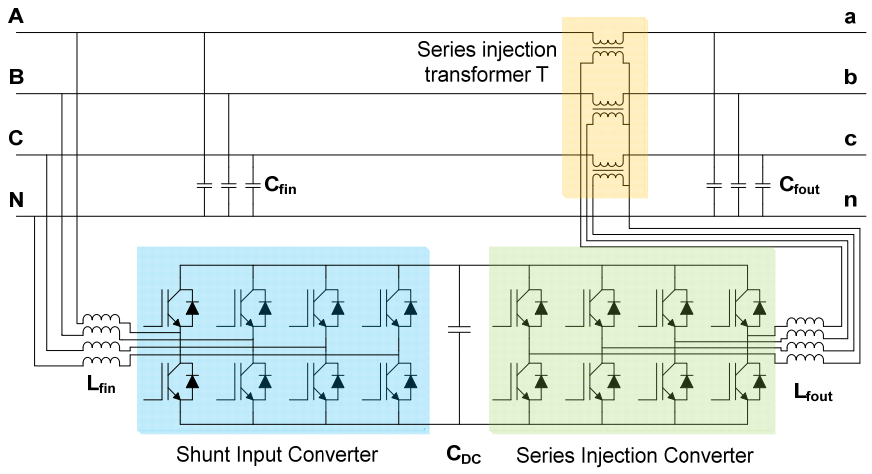

Figure 3.1 A 4+4 leg UPFC based compensator with reduced DC bus capacitor

3.3. Modelling of the 4+4 leg UPFC in continuous time domain

Modern switching converters, especially below 100kVA where the switching frequencies often exceed 10kHz, can be usefully modelled for control purposes in continuous domains [105]. The proposed 4+4 leg UPFC based compensator is first modelled in the continuous time domain. The continuous domain model of the UPFC based compensator mainly consists of series and shunt converters with a DC bus capacitor.

The series converter is controlled to produce the injected voltages and the parallel converter is current controlled to satisfy the instantaneous power requirements for the series converters. The DC bus capacitor power is the difference between the input parallel converter power and the output series injection powers, and the voltage is the integral of the resulting charging current.

3.4. Instantaneous power flow analysis through UPFC

3.4.1. Voltage regulation

Instantaneous reactive power theory [20] has been applied to control the proposed 4+4 leg UPFC based compensator. The 4+4 leg UPFC based compensator provides voltage compensation to regulate voltages at the output terminals a, b and c by injecting a controllable series voltage component, v_s . In LV four-wire distribution networks, unbalanced variation in voltage results from either unbalanced loading or generation, or unequal impedances. To correct such unbalance voltages, the series injection voltage should be unbalanced and this injected series voltage, v_s, may have positive, negative and zero sequence components. The series injection converter must have four phase legs to produce the necessary degrees of freedom to inject these sequence components of voltage. The continuous domain model of the compensator with continuous time voltage and current sources is shown in Figure 3.2.

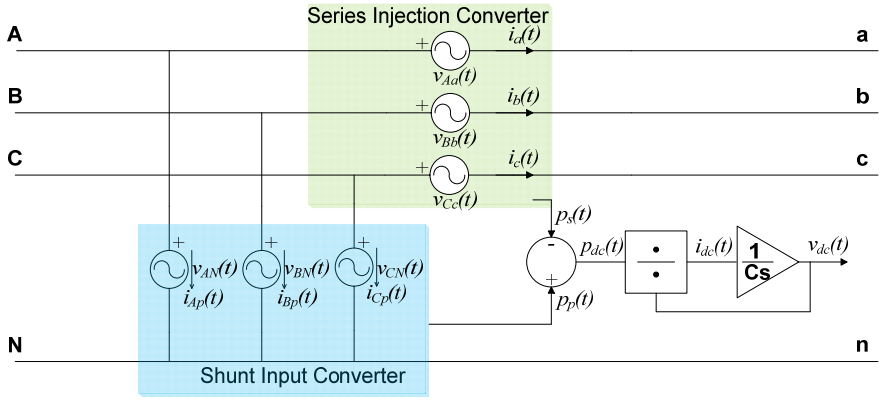

Figure 3.2 Continuous time domain model of 4+4 leg UPFC based compensator [19]

The instantaneous power developed by the series injection elements is given by [19]:

$$p_s(t) = i_a(t) \times v_{Aa}(t) + i_b(t) \times v_{Bb}(t) + i_c(t) \times v_{Cc}(t)$$

$$= \overline{p_s} + \widetilde{p_s} \qquad (1)$$

The instantaneous power can be expressed as an average value, $\overline{p}$, and an oscillatory component, $\tilde{p}$. The injected voltage is expressed as a sum of positive, negative and zero sequence components as follows:

$$v_{Aa}(t) = \sqrt{2}V_{s+}sin(\omega t + \varphi_{vs+}) + \sqrt{2}V_{s-}sin(\omega t + \varphi_{vs-}) + \sqrt{2}V_{s0}sin(\omega t + \varphi_{vs0}) \quad (2)$$

$$v_{Bb}(t) = \sqrt{2}V_{s+}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{vs+}\right) + \sqrt{2}V_{s-}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{vs-}\right) + \sqrt{2}V_{s0}sin(\omega t + \varphi_{vs0}) \quad (3)$$

$$v_{Cc}(t) = \sqrt{2}V_{s+}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{vs+}\right) + \sqrt{2}V_{s-}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{vs-}\right) + \sqrt{2}V_{s0}sin(\omega t + \varphi_{vs0}) \quad (4)$$

Similarly the line currents can be expressed as:

$$i_a(t) = \sqrt{2}I_{s+}sin(\omega t + \varphi_{is+}) + \sqrt{2}I_{s-}sin(\omega t + \varphi_{is-}) + \sqrt{2}I_{s0}sin(\omega t + \varphi_{is0}) \quad (5)$$

$$i_b(t) = \sqrt{2}I_{s+}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{is+}\right) + \sqrt{2}I_{s-}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{is-}\right) + \sqrt{2}I_{s0}sin(\omega t + \varphi_{is0}) \quad (6)$$

$$i_c(t) = \sqrt{2}I_{s+}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{is+}\right) + \sqrt{2}I_{s-}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{is-}\right) + \sqrt{2}I_{s0}sin(\omega t + \varphi_{is0}) \quad (7)$$

The resulting average and oscillatory powers of the series injection converter are expressed as [20, 118]:

$$\overline{p_s} = 3\,V_{s+}\,I_{s+}\cos(\varphi_{vs+} - \varphi_{is+}) + 3\,V_{s-}\,I_{s-}\cos(\varphi_{vs-} - \varphi_{is-}) + 3\,V_{s0}\,I_{s0}\cos(\varphi_{vs0} - \varphi_{is0}) \quad (8)$$

$$\begin{aligned}\widetilde{p_s} = &-3\,V_{s+}\,I_{s-}\cos(2\omega t + \varphi_{vs+} + \varphi_{is-}) \\ &-3\,V_{s-}\,I_{s+}\cos(2\omega t + \varphi_{vs-} + \varphi_{is+}) \\ &-3\,V_{s0}\,I_{s0}\cos(2\omega t + \varphi_{vs0} + \varphi_{is0})\end{aligned} \quad (9)$$

Assume the input voltages to the parallel converter are:

$$v_{AN}(t) = \sqrt{2}V_{p+}sin\left(\omega t + \varphi_{vp+}\right) + \sqrt{2}V_{p-}sin\left(\omega t + \varphi_{vp-}\right) + \sqrt{2}V_{p0}sin\left(\omega t + \varphi_{vp0}\right) \quad (10)$$

$$v_{BN}(t) = \sqrt{2}V_{p+}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{vp+}\right) + \sqrt{2}V_{p-}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{vp-}\right) + \sqrt{2}V_{p0}sin\left(\omega t + \varphi_{vp0}\right) \quad (11)$$

$$v_{CN}(t) = \sqrt{2}V_{p+}sin\left(\omega t + {}^{2\pi}/_{3} + \varphi_{vp+}\right) + \sqrt{2}V_{p-}sin\left(\omega t - {}^{2\pi}/_{3} + \varphi_{vp-}\right) + \sqrt{2}V_{p0}sin\left(\omega t + \varphi_{vp0}\right) \quad (12)$$

In a voltage regulator with negligible energy storage, the series injected power must be balanced by power delivered by the shunt converter. A LV distribution network with unbalanced loading or unbalanced solar generation will produce unbalanced current, and the input currents thus have positive, negative and zero sequence components. Power balance can be satisfied by controlling the input currents in terms of the positive, negative and zero sequence components. So, the shunt converter must draw positive, negative and zero sequence components simultaneously. This is only possible if the shunt converter has four phase legs to produce the necessary degrees of freedom. However, the input currents are arbitrarily controlled with the positive, negative and zero sequence components as follows:

$$i_{Ap}(t) = \sqrt{2}I_{p+}sin(\omega t + \varphi_{ip+}) + \sqrt{2}I_{p-}sin(\omega t + \varphi_{ip-}) + \sqrt{2}I_{p0}sin(\omega t + \varphi_{ip0}) \quad (13)$$

$$i_{Bp}(t) = \sqrt{2}I_{p+}sin(\omega t - {}^{2\pi}/_{3} + \varphi_{ip+}) + \sqrt{2}I_{p-}sin(\omega t + {}^{2\pi}/_{3} + \varphi_{ip-}) + \sqrt{2}I_{p0}sin(\omega t + \varphi_{ip0}) \quad (14)$$

$$i_{Cp}(t) = \sqrt{2}I_{p+}sin(\omega t + {}^{2\pi}/_{3} + \varphi_{ip+}) + \sqrt{2}I_{p-}sin(\omega t - {}^{2\pi}/_{3} + \varphi_{ip-}) + \sqrt{2}I_{p0}sin(\omega t + \varphi_{ip0}) \quad (15)$$

The parallel input converter instantaneous power is:

$$p_p(t) = i_{Ap}(t) \times v_{AN}(t) + i_{Bp}(t) \times v_{BN}(t) + i_{Cp}(t) \times v_{CN}(t)$$

$$= \overline{p_p} + \widetilde{p_p} \quad (16)$$

The average and oscillatory powers for the parallel converter are [20]:

$$\overline{p_p} = 3\,V_{p+}\,I_{p+}\cos(\varphi_{vp+} - \varphi_{ip+}) + 3\,V_{p-}\,I_{p-}\cos(\varphi_{vp-} - \varphi_{ip-}) + 3\,V_{p0}\,I_{p0}\cos(\varphi_{vp0} - \varphi_{ip0}) \quad (17)$$

$$\widetilde{p_p} = -3\,V_{p+}\,I_{p-}\cos(2\omega t + \varphi_{vp+} + \varphi_{ip-}) - 3\,V_{p-}\,I_{p+}\cos(2\omega t + \varphi_{vp-} + \varphi_{ip+}) - 3\,V_{p0}\,I_{p0}\cos(2\omega t + \varphi_{vp0} + \varphi_{ip0}) \quad (18)$$

In practical applications, the shunt converter input voltage has a dominant positive sequence component, $V_{p+}\angle\varphi_{vp+}$, but is not necessarily completely balanced.

If $$V_{p+} \gg V_{p-} \tag{19}$$

Then $$\overline{p_p} = 3\,V_{p+}\,I_{p+}\cos(\varphi_{vp+} - \varphi_{ip+}) \tag{20}$$

$$\widetilde{p_p} = -3\,V_{p+}\,I_{p-}\cos(2\omega t + \varphi_{vp+} + \varphi_{ip-}) \tag{21}$$

Equation (20) shows that the average power, $\overline{p}$, could be satisfied with the lowest current if the shunt converter draws positive sequence unity power factor current. Equation (21) shows that the oscillatory power can be balanced by the input converter by drawing a negative sequence current with an appropriate magnitude and phase.

3.4.2. Active filtering

If the parallel converter is to draw the compensation current for harmonics, the instantaneous power will have oscillatory components which will further produce DC bus voltage fluctuations. This requires the development of instantaneous power flow equations for the parallel converter due to harmonic currents which will provide a design guideline for the selection of DC bus capacitance with the presence of nonlinear loads. For a three phase four-wire system, the nonlinear loads can be expressed as the sum of fundamental current and harmonic current [119]. During the steady state, the harmonic component of the load current will charge or discharge the DC bus capacitor, and can thus cause fluctuations in DC bus voltage. The energy storage, E_c due to the harmonic components of the load current at the DC bus capacitor is given by:

$$E_c = \frac{1}{2}C_{DC}(V_U^2 - V_L^2) \tag{22}$$

Consider the balanced 5th harmonic current set which is a negative sequence set and will have no positive and zero sequence component. The 5th harmonic current set is:

$$i_{Ah}(t) = \sqrt{2} I_{h-} sin(5\omega t + \varphi_{ih-}) \tag{23}$$

$$i_{Bh}(t) = \sqrt{2} I_{h-} sin\left(5\omega t + {}^{2\pi}/_{3} + \varphi_{ih-}\right) \tag{24}$$

$$i_{Ch}(t) = \sqrt{2} I_{h-} sin\left(5\omega t - {}^{2\pi}/_{3} + \varphi_{ih-}\right) \tag{25}$$

Instantaneous power flow into the parallel converter due to the balanced 5th harmonic current set is given by:

$$p_h(t) = i_{Ah}(t) \times v_{AN}(t) + i_{Bh}(t) \times v_{BN}(t) + i_{Ch}(t) \times v_{CN}(t)$$

$$= \overline{p_h} + \widetilde{p_h} \tag{26}$$

The average and oscillatory powers for the parallel converter due 5th harmonic current are:

$$\overline{p_h} = 0 \tag{27}$$

$$\widetilde{p_h} = -3\, V_{p+}\, I_{h-} \cos\left(6\omega t + \varphi_{vp+} + \varphi_{ih-}\right) + 3\, V_{p-}\, I_{h-} \cos\left(-4\omega t + \varphi_{vp-} - \varphi_{ih-}\right) \tag{28}$$

The average power term is zero and the 5th harmonic current produces an oscillatory power term at $\omega(n-1)$ and $\omega(n+1)$, where n is the harmonic number. In practical applications, the shunt converter input voltage has a dominant positive sequence component, $V_{p+} \angle \varphi_{vp+}$, but is not necessarily completely balanced if $V_{p+} \gg V_{p-}$. In this case, $\widetilde{p_h}$ becomes:

$$\widetilde{p_h} \approx -3\, V_{p+}\, I_{h-} \cos\left(6\omega t + \varphi_{vp+} + \varphi_{ih-}\right)$$

$$\approx -\widetilde{P_h} \cos\left(6\omega t + \varphi_{vp+} + \varphi_{ih-}\right) \tag{29}$$

If the DC bus capacitor must carry the oscillatory harmonic power, $\widetilde{p_h}$, then the energy storage would be the area under the one half cycle of the cosine waveform. The calculated energy storage is then given by:

$$E_c = \frac{2}{\pi} \times \widetilde{P_h} \times \tau \tag{30}$$

For the cosine term with 6ω oscillations, the time constant, τ, would be equal to $\frac{T}{12}$ and substituting this value yields the total energy storage as:

$$E_c = \frac{2}{\pi} \times P_h \times \frac{T}{12} \tag{31}$$

Equating (22) and (31) and using the energy balance concept, the DC bus capacitance can be determined as:

$$C_{DC} = \frac{2V_{p+}\, I_{h-}}{\omega(V_U^2 - V_L^2)} \tag{32}$$

The required capacitor size depends upon the upper and lower bus voltage limits, V_U and V_L respectively. It also depends upon the positive sequence r.m.s magnitude of source voltage, V_{p+}, and harmonic current, I_{h-}.

3.4.3. Ancillary services

Apart from the voltage regulation and active filtering duties, the shunt converter can provide the zero sequence and reactive current compensation. For zero sequence current compensation, the parallel converter can draw zero sequence current without producing either an average power term or an oscillatory power term as the zero sequence current magnitude is absent from (20) and (21). For a positive sequence reactive current, the phase angle between the voltage and current in (20) is π/2, resulting in a zero cosine term. The implication is that the parallel converter can compensate zero sequence current and positive sequence reactive power without any implication for the DC bus capacitor size. A negative sequence current, however, will produce an oscillatory power that will be present at the DC bus. This presents the following design choices:

- A design with a minimum bus capacitor that controls the parallel converter negative sequence current to provide instantaneous power balance.
- A design with a large bus capacitor that can provide negative sequence current for phase balancing up to the current limits of the phase legs.
- A compromise design with a DC capacitor that is sized to allow a controlled amount of negative sequence current.

3.5. Control strategies for UPFC based compensator

3.5.1. Voltage control strategy for series converter

One of the possible voltage control arrangements for the series converter is shown in Figure 3.3. The series converter is voltage controlled to force the output voltages to follow a positive sequence reference set of magnitude $230V_{rms}$.

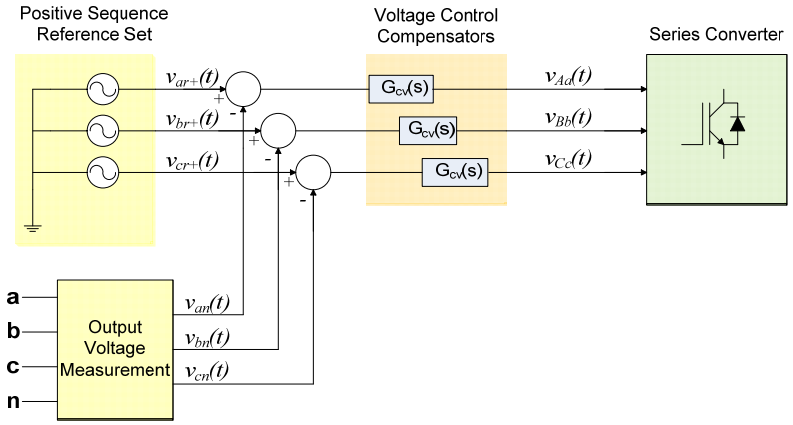

Figure 3.3 Voltage control arrangement for the series converter of UPFC based compensator [19]

In practice, the three controlled voltage sources will need to inject positive, negative and zero sequence components. The shunt converter must be controlled to provide the instantaneous power demands of the series converter. This type of voltage control gives a wider control bandwidth, but the stability of the control loop is often limited in practice by the resonant frequency and output impedance of the filter. Another approach is the sequence based control where a rotating dq reference frame at fundamental frequency, ω, is established such that the time-varying output voltages are transformed into DC quantities. This enables perfect tracking of the reference for the positive sequence component of the output voltage. In this method, the compensating voltage terms are injected into the duty cycles based on the negative and zero sequence content of the output voltages. The sequence based controller has a lower control bandwidth and may be practically easier to stabilise the control loop. Another advantage of the sequence based controller is that it will not automatically respond to the harmonics. Figure 3.4 represents the simplified control

diagram for a sequence based voltage regulator. A Phase Locked Loop (PLL) is used to extract a local sine and cosine reference from the incoming grid voltages. The output positive, negative and zero sequence voltages are detected using transformations into rotating d, q, 0 reference frames [120].

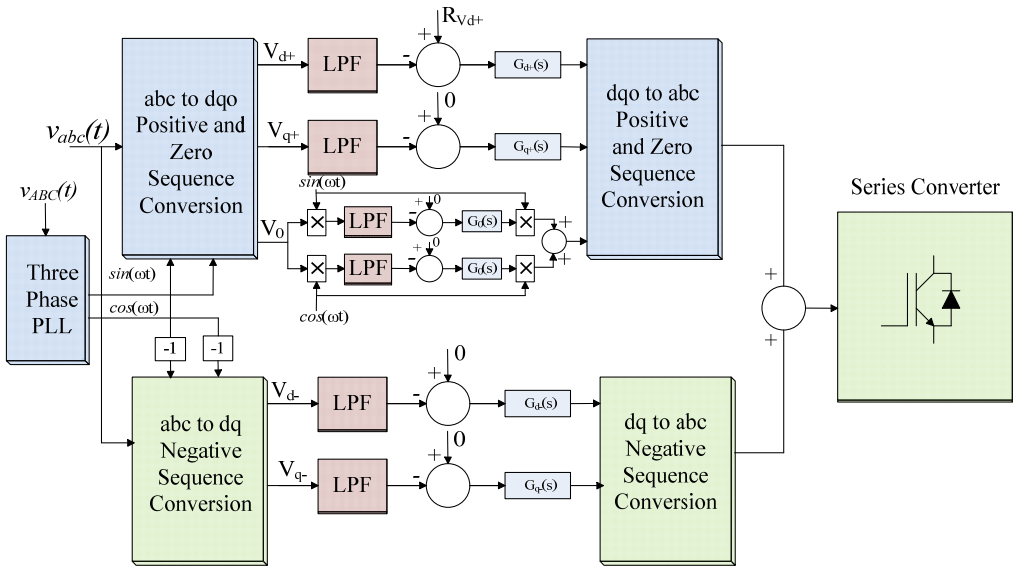

Figure 3.4 Sequence based voltage control strategy for series converter of UPFC based compensator

A unique feature of sequence based control is the use of two rotating reference frame controllers to independently control the positive sequence output voltage and to achieve balance by forcing the negative and zero sequence output voltages to zero. In the positive sequence frame rotating at the fundamental frequency of ω, the direct axis voltage should track a fixed reference voltage, R_{Vd+} while the quadrature axis voltage should be zero in the balanced case. This forces the regulator positive sequence output voltage to be in phase with the input positive sequence voltage, and this requires the lowest level of voltage injection. However, in a three phase four-wire system, the fourth leg of the inverter facilitates control of the zero sequence current and voltage when the system becomes unbalanced. This zero sequence voltage appears in the 0-axis at the fundamental frequency. Because the 0-axis actually exists in the stationary frame, there is no way to rotate the 0-

axis voltage in order to transform it into a DC quantity. So a technique is applied to compensate the zero sequence quantity which is shown in the fundamental frequency positive rotating frame. The zero sequence controller can be implemented in any dqo reference frame as the 0-axis remains the same in all rotating reference frames. The d, q and 0 axis voltage errors drive PI regulators that establish voltage targets for the series converter. These are converted into phase voltages by an inverse d, q to a, b, c transformation.

In the negative sequence frame rotating at the fundamental negative frequency of -ω, the output voltages should be forced to zero by the action of the PI controllers. The negative sequence phase voltages are formed with an inverse d, q to a, b, c transformation. The negative and positive sequence targets are added and converted to line to line voltage targets.

3.5.2. Power control strategy for shunt converter

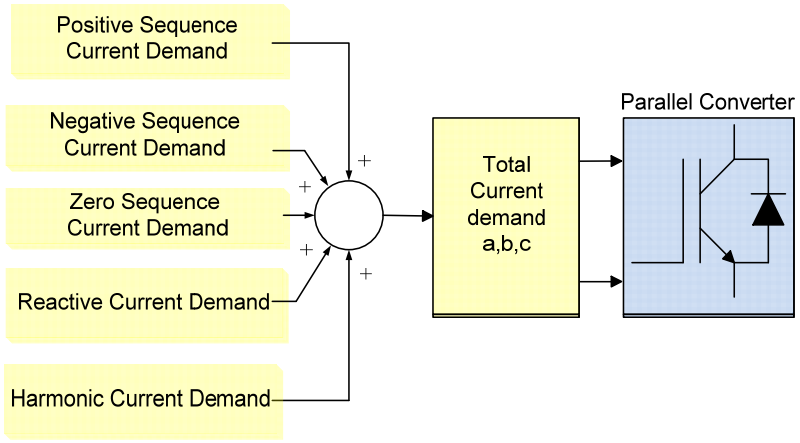

Figure 3.5 Complete current control strategy for shunt converter of UPFC based compensator

A possible power control solution which requires the parallel converter to be equipped with a responsive current control system is illustrated in Figure 3.5. The instantaneous power control is performed by a positive, negative and zero sequence framework approach instead of an α,β framework. Direct control of the 2ω oscillatory powers in the α,β

framework will produce fundamental and third harmonic line currents [19]. This is avoided in the positive, negative and zero sequence based approach. The power control system for the shunt converter which consists of responsive five current components is shown in Figure 3.5. The average power control system is shown in Figure 3.6. It consists of a feed forward current control loop, DC capacitor average voltage control loop and an instantaneous average DC bus voltage limit function. These three systems produce a total positive sequence magnitude demand signal that is multiplied by a three phase positive sequence sinusoidal reference set to produce phase demand signals. The reference set is generated from the converter input voltages using a PLL. Figure 3.7 shows the oscillatory 2ω power control loop. This oscillatory 2ω power control loop balances the oscillatory powers introduced by unbalanced loading of the series converter. In Figure 3.7, the oscillatory power difference between the series and parallel converters is determined by subtraction. A sine and cosine synchronous detector and the associated 5ms moving average filters determine the oscillatory powers at 2ω.

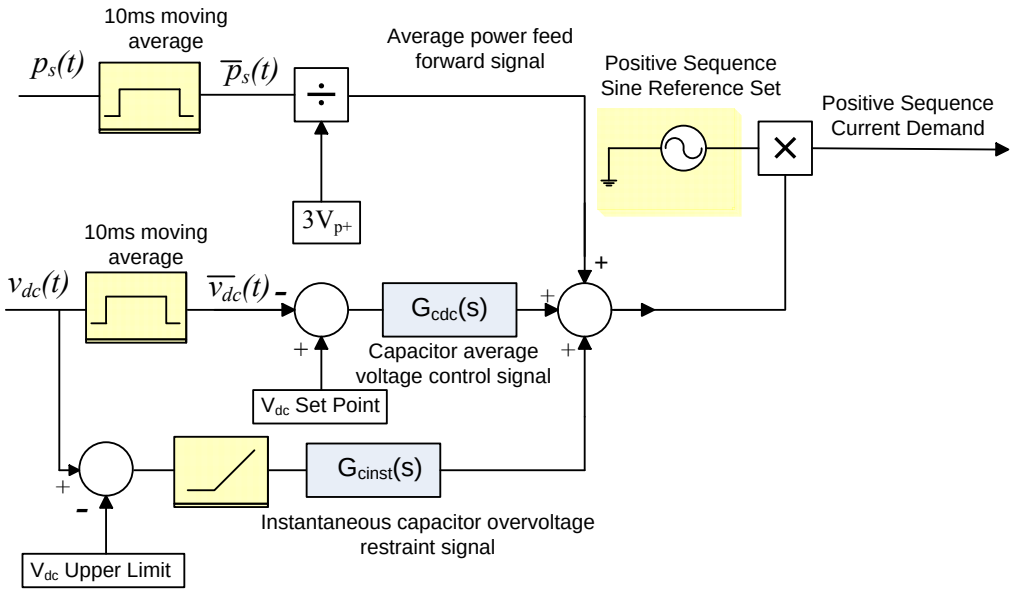

Figure 3.6 Average power control arrangement

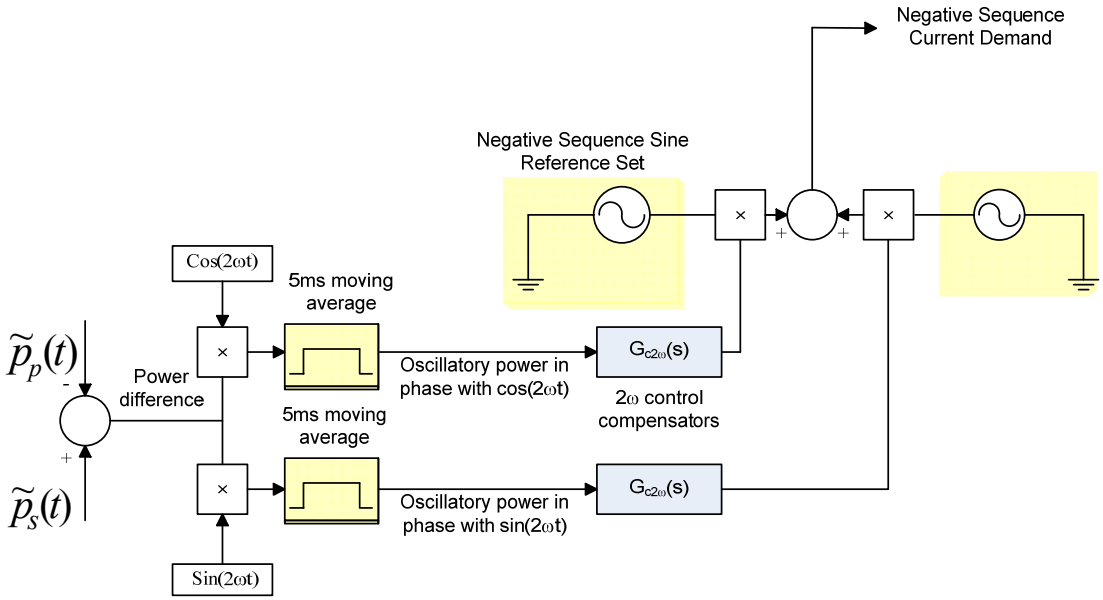

Figure 3.7 2ω oscillatory power control arrangement

These components are forced to zero by the actions of the control amplifiers $G_{c2\omega}(s)$. A residual oscillatory power in phase with cos(2ωt) is cancelled by injecting a sinusoidal negative sequence current into the phase current demand signals driving the shunt converter. The schematic for reactive current compensation which provides the reactive current demand is depicted in Figure 3.8. In this control strategy, the supply current is multiplied by a positive sequence cosine reference set. This will produce 2ω oscillation of the supply current. The products are summed and then averaged over a 10ms window to detect the appropriate DC value of the reactive component of the supply current by removing the time varying parts. Then a feedback control system with PI regulator is used to force any tracking error to zero by the action of the reactive current compensator, $G_{crc}(s)$. The output of PI regulator gives a DC value of the reactive current demand.

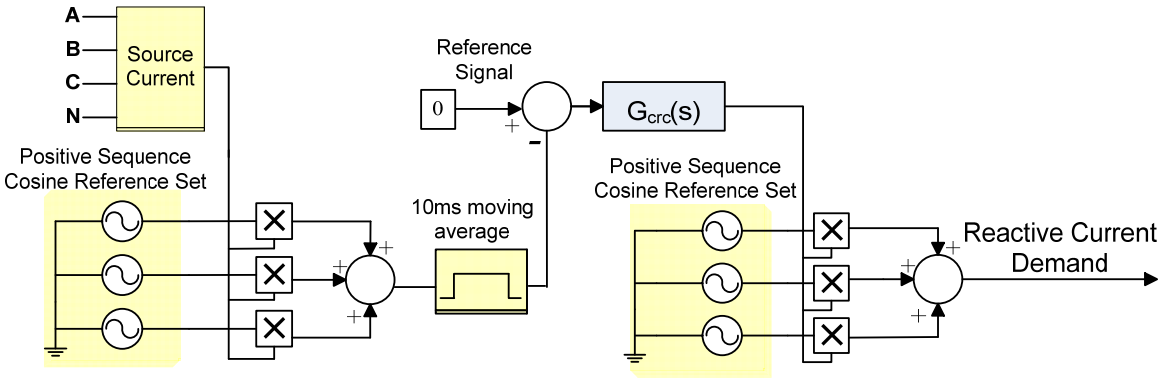

Figure 3.8 Reactive current compensation arrangement

This current is then finally multiplied by the positive sequence cosine reference set to produce the reactive current demand of the loads. The parallel converter draws and supplies the reactive current demand of the load to the PCC while producing no average power term. Thus reactive power control is achieved by the UPFC that makes it possible to implement power factor correction. Regardless of the load power factor, the source will provide the supply current in phase with the supply voltage. The zero sequence current demand is used to compensate the neutral current of the A, B, C, N input terminals of the voltage regulator. The parallel converter draws zero sequence current demand while producing no average and oscillatory power terms.

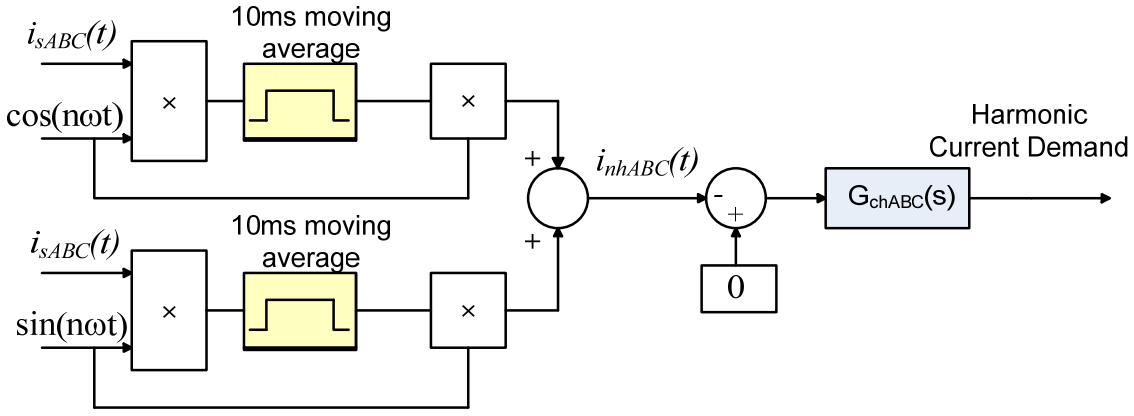

Figure 3.9 Harmonic current reference detection and control arrangement

Figure 3.9 shows the method of finding the harmonic current reference while extracting the fundamental current and adding the cancelling harmonic at the PCC through the active filter. A synchronous reference framework method has been applied at each phase to extract the fundamental current, and the feedback control system has been used to force the harmonic current error to zero. The three phase currents $i_{sABC}\ (t)$ are measured at the PCC. These three phase currents are multiplied with two orthogonal signals, i.e. sine and cosine terms at the harmonic frequency, $n\omega$. In each case, the resultant is low pass filtered with a 10ms moving average which removes the fundamental component and provides a DC level proportional to the harmonic current. This signal is further multiplied by the sine and cosine terms at the harmonic frequency, $n\omega$ and then summed up to produce the resultant harmonic current references $i_{nhABC}\ (t)$ for the three phases.

3.6. Conclusion

In this chapter, the modelling of the proposed UPFC based compensator for a set of duties is provided and the necessary mathematical equations are derived for each of that set of duties. The modelling of the UPFC is carried out in the continuous time domain with the assumption that the switching frequency of the converters is more than 10kHz and the converter power is below 100kVA. Instantaneous power theory is applied to control the series and shunt converters of the UPFC, and the general equations for the average and oscillatory power are presented. A mathematical equation is derived to provide guidance on the selection of the DC bus capacitor if the UPFC is to provide the compensation current for the harmonics. In addition, a set of converter design choices is provided based on the selection of the DC bus capacitor. The voltage and power control approaches are also presented and discussed with the relevant schematics.

Chapter 4 SIMULATION RESULTS

4.1. Introduction

In this chapter, the operation of the 4+4 leg UPFC based compensator is confirmed by a series of simulations. The simulations are conducted in Matlab Simulink. The simulations are carried out on the compensator for voltage regulation, active filtering and other ancillary services including power factor correction and zero sequence current compensation. Simulation results confirm that the compensator is capable of effectively regulating the load voltage of a distribution feeder while providing reactive current and neutral current compensation. It is also shown that the shunt converter of the UPFC can also provide the harmonic compensation current for nonlinear loads.

4.2. Application of UPFC based compensator in LV distribution feeder

The simulations make use of a test case based distribution configurations present in the Perth Solar City and first presented in [19]. A four-wire UPFC based compensator is located at the mid-point of a 300m LV four-wire three phase distribution feeder as shown in Figure 4.1. In this case, an aerial feeder is considered which is constructed with a 7/3.75mm all aluminium conductor. This conductor is extensively used within Australian distribution networks and commonly designated as “Mars”. The conductor impedance is (0.452+0.270j)Ω/km. The supply transformer is rated at 200kVA, 415/240V, 50Hz and has a per-unit series impedance of 0.01+0.03jΩ. Each phase of the feeder is loaded by $100A_{rms}$ 0.95 power factor lagging loads which are located at the far end of the distribution feeder. A switchable solar panel of $50A_{rms}$ unity power factor is also placed at the far end of the feeder and is connected with phase “b” of the distribution feeder. The simulation parameters are listed in Tables 4.1 and 4.2. The positive sequence sine and negative sequence sine and cosine sets have unit peak magnitude. To improve the stability of the

simulation, 10μF capacitors are connected at the regulator input from terminals A,B,C to N and at the load terminals, phase to neutral.

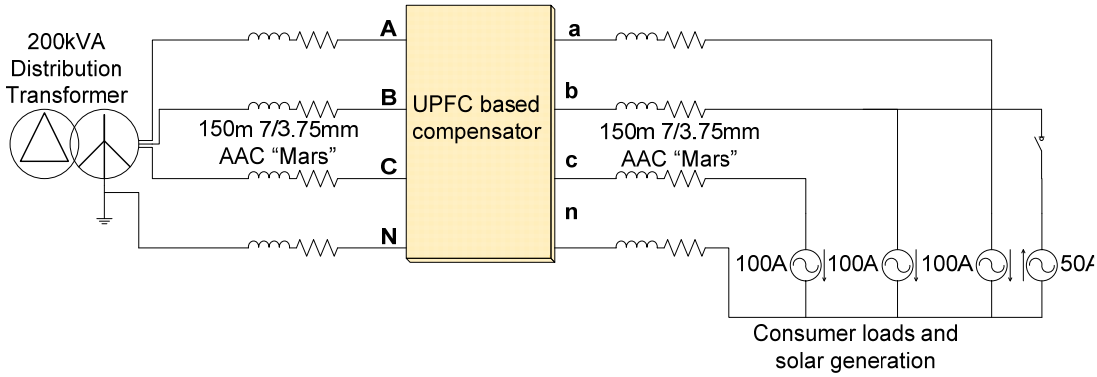

Figure 4.1 Application of 4+4 leg UPFC based compensator in LV distribution feeders [19]

Table 4.1 PI controllers used in the simulation

PI Controllers	Proportional gain, K_p	Integral gain, K_i
Reactive current compensator, G_{crc} (s)	1	100
Zero sequence current controller, G_{cl0} (s)	0.4	8000
Output voltage regulators, G_{ccv} (s)	2	10000
DC bus voltage regulator, G_{cdc} (s)	0.0004	0.004
DC bus instantaneous voltage limit regulators, G_{cinst} (s)	0.1 only if V_{dc} > 800V	0
2ω oscillatory power compensators, $G_{c2\omega}$ (s)	2	200

Table 4.2 Different parameters used in the simulation and their values

Parameters	Value
DC bus capacitor	10μF
Vdc set point	700V
Vdc upper limit	800V
Series injection controlled voltage source gain	1
DC bus voltage regulator current limit	10A peak

4.3. Simulation results for UPFC based compensator

The simulation of the 4+4 leg UPFC based compensator is carried out for two cases. The UPFC based compensator is first configured to provide full voltage compensation and only zero sequence current compensation. Then, the compensator is designed to provide voltage compensation with both neutral and reactive current compensation.

4.3.1. UPFC with zero sequence current compensator

The dynamic response of the UPFC based compensator equipped with zero sequence current compensator is explored in Figures 4.2 to 4.10. The colour convention for the representation of phase voltages used in the entire thesis is red for phase "a", green for phase "b" and blue for phase "c" unless otherwise specified. The industry convention is to use white or yellow for phase "b" but these do not have sufficient contrast when printed on a white figure background. The UPFC based compensator is allowed to settle into steady state operation with a balanced $100A_{rms}$ 0.95 power factor lagging load. At t = 0.5067s, the voltage zero crossing in "b" phase (green), a $50A_{rms}$ unity power factor solar generator commences its operation. The solar current ramps up over one 20ms cycle and reaches its full current at t = 0.5267s. The performance of the proposed four-leg UPFC based compensator as a voltage regulation device is explored in Figures 4.2 and 4.3. Figure 4.2 shows the three phases voltages at A,B,C,N input terminals and a,b,c,n output terminals respectively without the operation of the compensator when the series voltage injection loop is disabled and does not inject any correction voltage with the feeder. It is seen that the output voltages are not regulated and the voltage at phase "b" becomes higher than the other two phases after the solar generation enters into the networks. The action of the voltage regulator is depicted in Figure 4.3. It is observed that the voltages at a,b,c,n output terminals are constant and well regulated before and after the solar generation comes into operation.

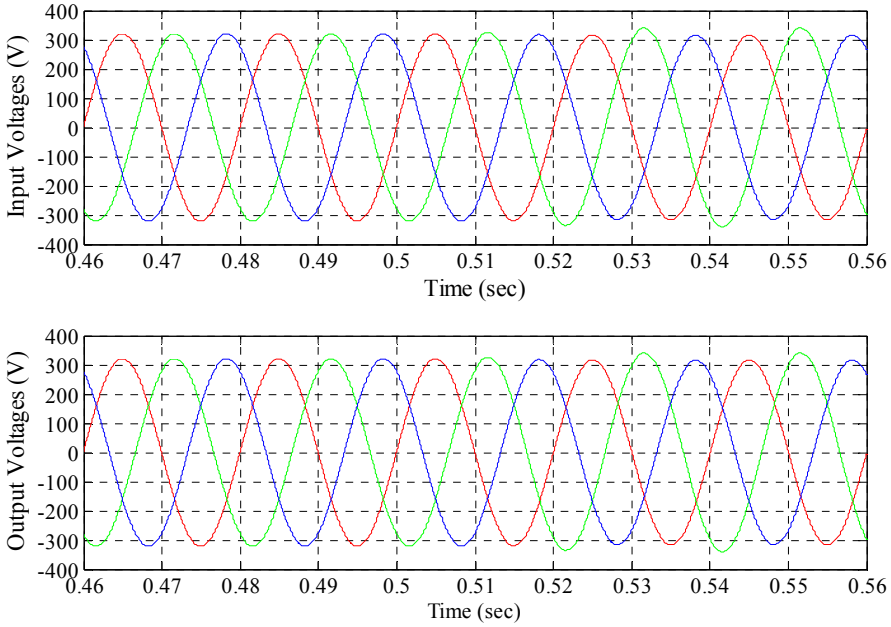

Figure 4.2 Voltages at A,B,C,N input and a,b,c,n output terminals without UPFC based compensator

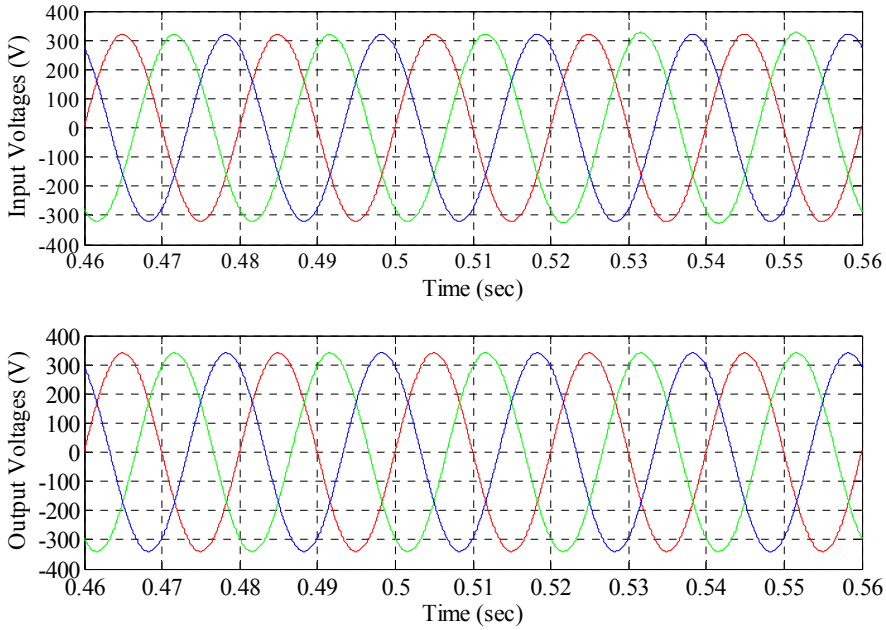

Figure 4.3 Voltages at A,B,C,N input and a,b,c,n output terminals with UPFC based compensator

The input voltages prior to t = 0.5067s are balanced but low. When the solar generation commences its operation at phase “b”, the input voltage at phase “b” (green) rises slightly as the phase current reduces. The currents from the input and output terminals of the UPFC based compensator are presented in Figures 4.4 and 4.5. The currents from the input and output terminals of the UPFC based compensator without zero sequence current

controller is shown in Figure 4.4. Prior to t = 0.5067s, both the input and output currents are completely balanced and no current flows through the neutral conductor. At t = 0.5067s when the solar generator commences its operation, the input and output line currents become unbalanced and the zero sequence current (black trace) is present at the neutral conductor which flows through both the A,B,C,N input and a,b,c,n output terminals as seen from Figure 4.4. The action of the zero sequence current controller is then obvious from Figure 4.5. When the solar generation initiates its operation at t = 0.5067s, the zero sequence current controller becomes active and forces the neutral current from A,B,C,N input terminals to nearly zero while simultaneously reducing the phase current imbalance. As a result, the input currents are significantly free of neutral current and only appear at the output terminal. The response of the series injection converter of the UPFC based compensator is shown in Figure 4.6. Prior to t = 5067s when the solar generation is off, the injected voltages in all three phases are completely balanced to regulate the output voltages.

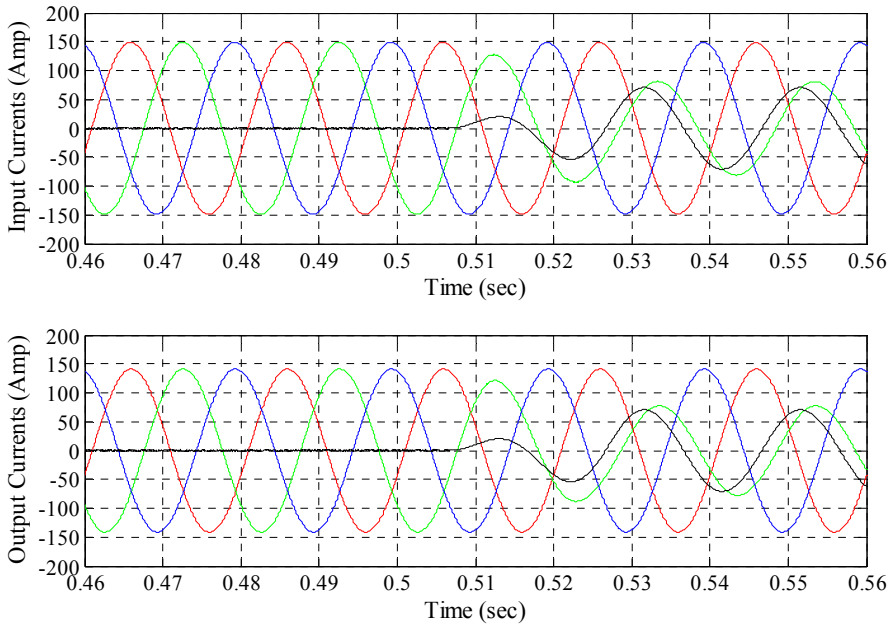

Figure 4.4 Currents from A,B,C,N input and a,b,c,n output terminals of the UPFC based compensator without zero sequence current compensator

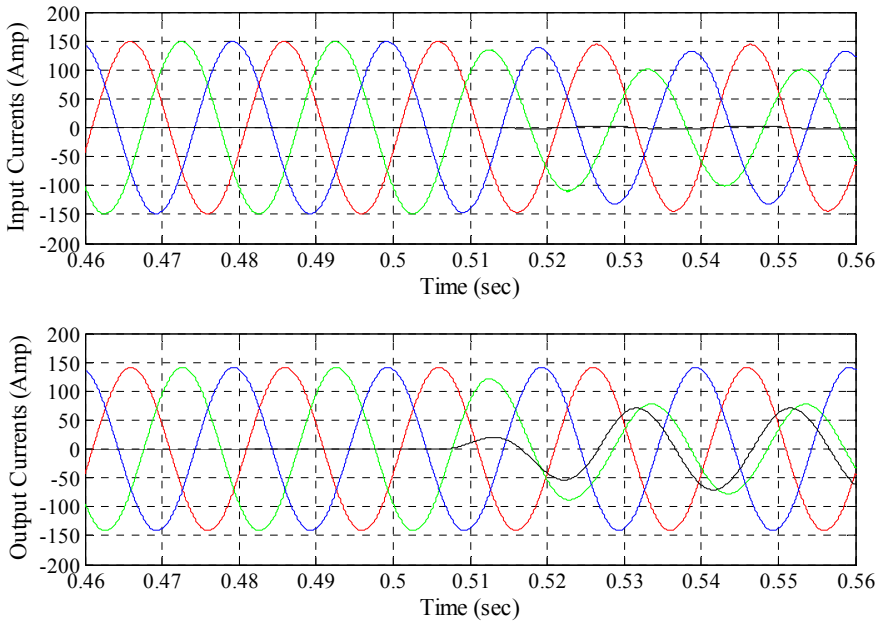

Figure 4.5 Currents from A,B,C,N input and a,b,c,n output terminals of the UPFC based compensator with zero sequence current compensator

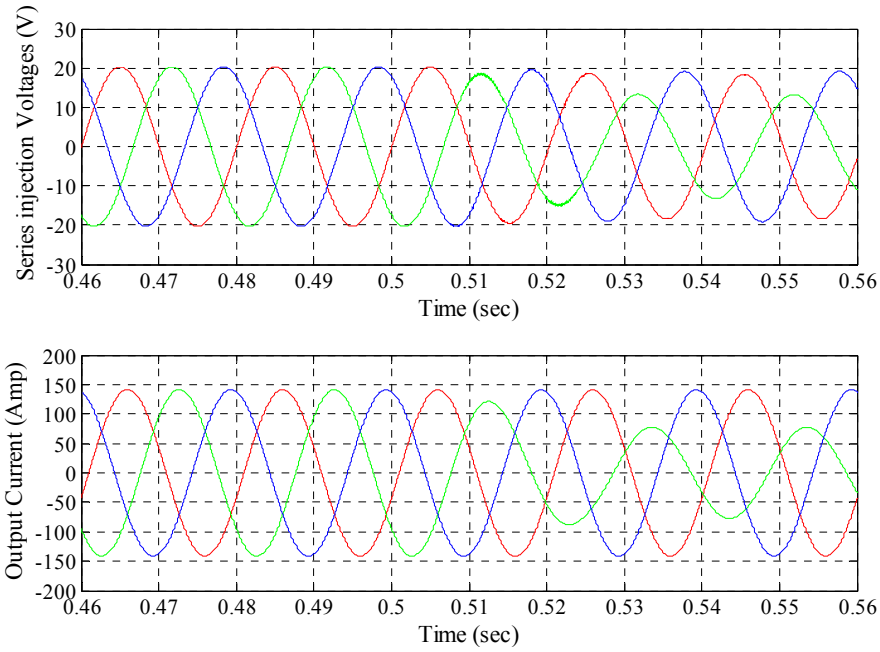

Figure 4.6 Series injection voltages and output currents from terminals a,b,c,n

After t = 0.5067s, when the solar generator commences in phase “b” (green), the current in phase “b” (green) reduces significantly over one cycle which consequently lowers the voltage injected in phase “b” (blue), seen in the upper trace. The response of the parallel converter of the UPFC based compensator is demonstrated in Figure 4.7. Prior to t =

0.5067s, the input current is balanced and the compensator adds only a balanced positive sequence voltage to control the voltages at output terminals a,b,c,n.

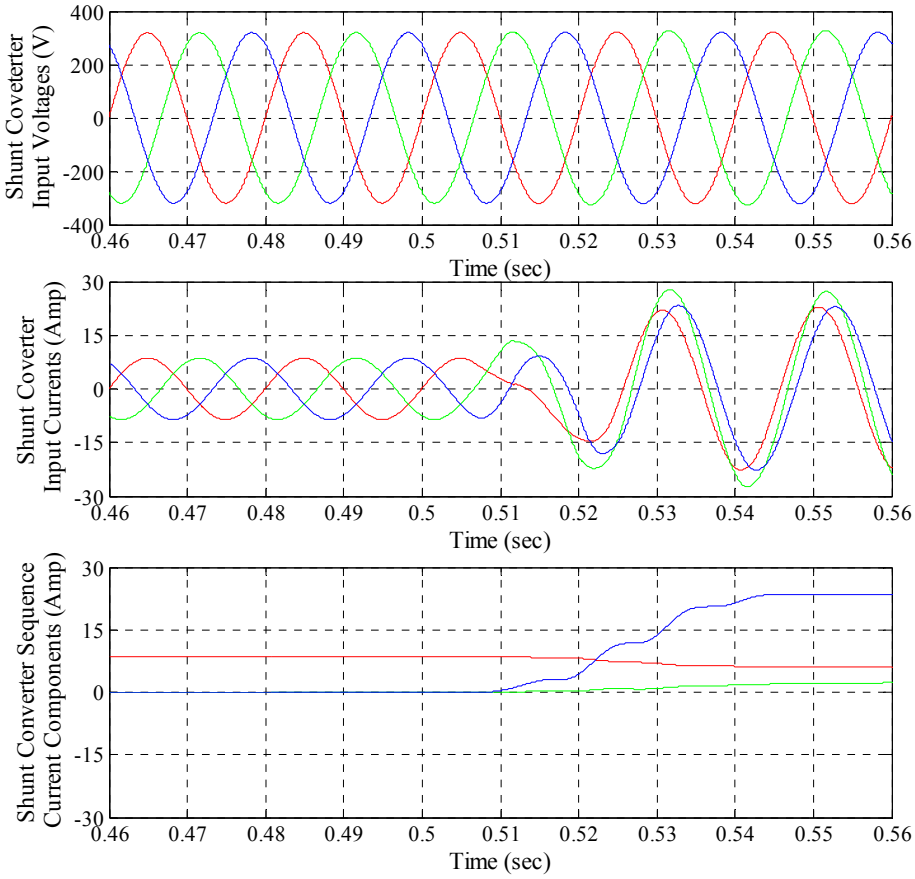

Figure 4.7 Shunt converter input voltages and currents with their sequence components (+ve sequence, red, -ve sequence, green, zero sequence, blue)

As a result, the shunt converter current prior to the operation of solar generation is completely balanced and positive sequence to meet the real power demand by the series converter. Before the solar generation commences, the real power requirement of the series converter is slightly above 4kW. Once the solar generation starts, the real power requirement drops and an oscillatory power requirement develops. Due to this reduction in real power demand by the series converter, the shunt converter draws a slightly less positive sequence current while increasing negative sequence current to meet the oscillatory power requirement developed due to solar generation. However, the parallel converter draws a combination of positive (red), negative (green) and zero sequence (blue)

currents to satisfy the average and oscillatory power requirement as seen in the lower trace. The shunt converter draws zero sequence current only when the solar generation commences as seen in Figure 4.7. Figure 4.8 shows the positive sequence current control system and control of the DC bus voltage.

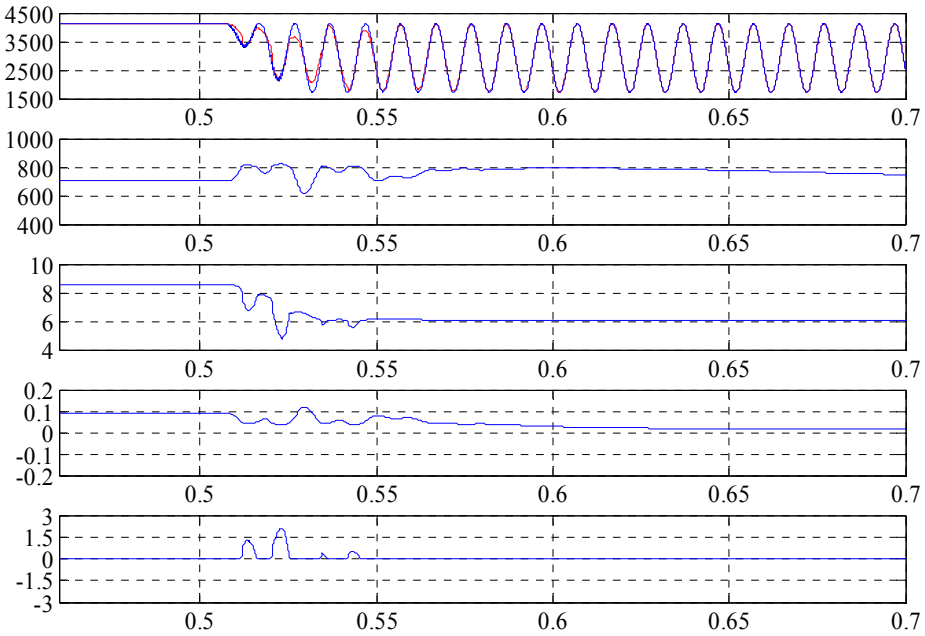

Figure 4.8 Top traces: series converter power (blue) and shunt converter power (red). Other traces top to bottom: DC bus voltage; positive sequence current demand feed forward signal; DC bus voltage regulator current demand; Instantaneous bus voltage current demand

As the solar generation commences, the line currents become unbalanced and the series converter demands a lower average power, shown as the upper blue trace. The parallel converter, the upper red trace, should rapidly follow the power demand to control the DC bus capacitor voltage shown as the second trace. The DC bus voltage is seen to be fluctuating until the shunt converter power reaches the power demand of the series converter. The positive sequence current forward system has a minimum 10ms response time and the demand signal is shown as the third trace. The positive sequence current demand is reduced as the real power demand is decreased by the series converter because of the solar generation in phase “b”. The capacitor voltage regulation loop, the demand signal of which is shown as the fourth trace, is slow responding and only corrects any

minor tracking errors in the feed forward system. The instantaneous power balance causes the capacitor voltage to rise rapidly. Once the capacitor voltage reaches 800Vdc, the instantaneous voltage limit system becomes active as shown in the lower trace. This instantaneously reduces the positive sequence current drawn by the parallel converter, thus limiting the voltage rise. From t = 0.55s, the instantaneous loop is inactive and the normal voltage control loop can rebalance the capacitor power and voltage as seen in Figure 4.8. The capacitor voltage becomes settled and reaches the steady state at t = 0.7s. Figure 4.9 shows the actions of the 2ω control loops. Prior to t = 0.5067s, the operation of 2ω control loops is inactive as the system is balanced and produces no oscillatory power demand. When the solar generator commences its operation at t = 0.5067s, the oscillatory power requirement develops and the 2ω control amplifiers begin to demand negative sequence sine and cosine currents to eliminate the oscillatory power fluctuation as shown in the lower traces of Figure 4.9. The effectiveness of the control systems in managing the DC bus capacitor voltage is illustrated in Figure 4.10. To do so, the instantaneous voltage limit control system and the 2ω control loops are turned off.

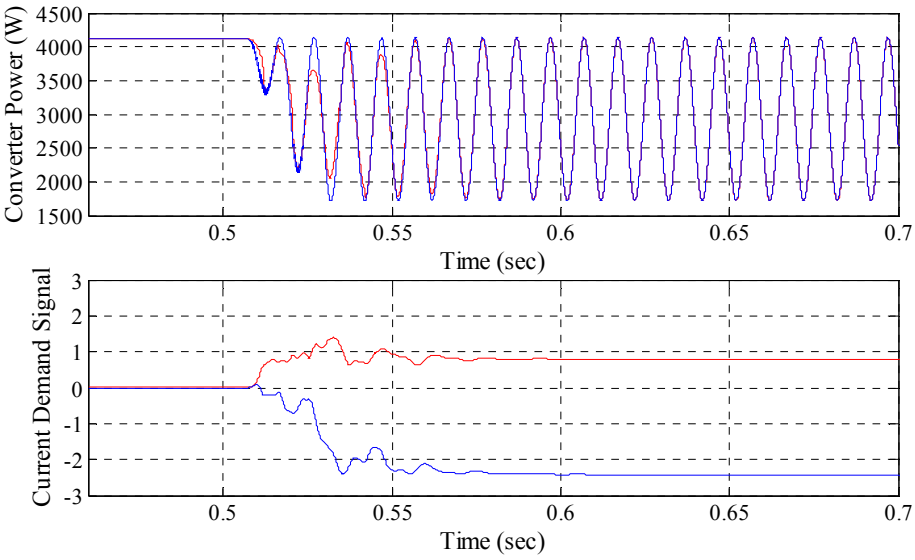

Figure 4.9 Series converter power (blue) and shunt converter power (red), and current demand signals for negative sequence cosine (blue) and sine (red) terms

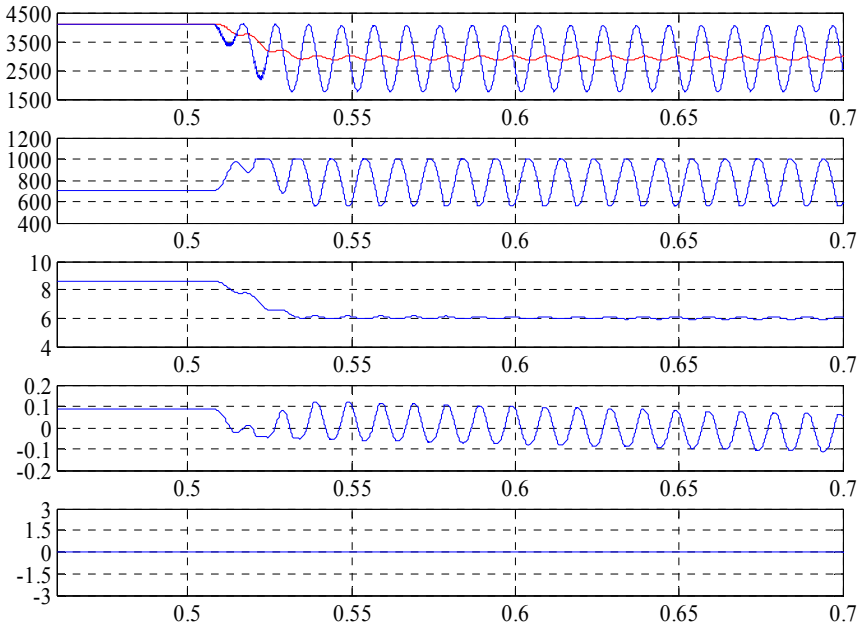

Figure 4.10 Top traces: series converter power (blue) and shunt converter power (red). Other traces top to bottom: DC bus voltage; positive sequence current demand feed forward signal; DC bus voltage regulator current demand; Instantaneous bus voltage current demand

From t = 0.5067s, the parallel converter cannot track the 2ω power oscillations and the DC bus voltage regulators and feed forward systems cannot respond rapidly to the capacitor voltage rise. The DC bus voltage rises sharply and exceeds 1000Vdc, as seen in the second trace. The DC bus average voltage does slowly reduce, but the capacitor voltage has a sustained 2ω voltage ripple as the small capacitor is forced to absorb the oscillatory power.

Table 4.3 outlines the steady state regulatory performance of the 4+4 leg UPFC based compensator with zero sequence current compensation when the solar generation is in service. It is shown that this form of loading produces significant zero sequence voltages, $V_0 = 0.4V_{rms}$ at the a,b,c,n output terminals without zero sequence current compensation, which are four times higher than the negative sequence voltages, $V_- = 0.1V_{rms}$. It is also observed that a zero sequence current, $I_0 = 16.7A_{rms}$ is present at input and output terminals of the UPFC based compensator. The zero sequence current compensator is applied to force the zero sequence current to nearly zero in the A,B,C,N input terminals and also to eliminate the zero sequence voltage component from the a,b,c,n output terminals.

Table 4.3 Input and output voltages and currents with zero sequence current compensation

Regulator State	Terminals A,B,C,N	Terminals a,b,c,n	Consumer Terminals
Inactive and Solar Generation Enabled (No Zero Sequence Compensation)	$V_+ = 229.1V_{rms}\ \varphi_+ = 0.9^o$ $V_- = 2.3V_{rms}\ \varphi_- = 124.2^o$ $V_0 = 9.1V_{rms}\ \varphi_0 = -116.0^o$ $I_+ = 83.9A_{rms}\ \varphi_+ = -21.0^o$ $I_- = 16.7A_{rms}\ \varphi_- = -59.2^o$ $I_0 = 16.7A_{rms}\ \varphi_0 = 60.6^o$	$V_+ = 229.1V_{rms}\ \varphi_+ = 0.9^o$ $V_- = 2.3V_{rms}\ \varphi_- = 124.2^o$ $V_0 = 9.1V_{rms}\ \varphi_0 = -116.0^o$ $I_+ = 84.1A_{rms}\ \varphi_+ = -21.4^o$ $I_- = 16.7A_{rms}\ \varphi_- = -59.2^o$ $I_0 = 16.7A_{rms}\ \varphi_0 = 60.6^o$	$V_+ = 218.3V_{rms}\ \varphi_+ = 1.8^o$ $V_- = 4.5V_{rms}\ \varphi_- = 124.2^o$ $V_0 = 18.2V_{rms}\ \varphi_0 = -116.0^o$ $I_+ = 84.1A_{rms}\ \varphi_+ = -21.4^o$ $I_- = 16.7A_{rms}\ \varphi_- = -59.2^o$ $I_0 = 16.7A_{rms}\ \varphi_0 = 60.6^o$
Inactive and Solar Generation Enabled (Zero Sequence Compensated)	$V_+ = 229.1V_{rms}\ \varphi_+ = 0.9^o$ $V_- = 2.3V_{rms}\ \varphi_- = 126.8^o$ $V_0 = 0.3V_{rms}\ \varphi_0 = 0^o$ $I_+ = 84A_{rms}\ \varphi_+ = -21.4^o$ $I_- = 16.7A_{rms}\ \varphi_- = -56.6^o$ $I_0 = 0.6A_{rms}\ \varphi_0 = 150.3^o$	$V_+ = 229.1V_{rms}\ \varphi_+ = 0.9^o$ $V_- = 2.3V_{rms}\ \varphi_- = 146.8^o$ $V_0 = 0.3V_{rms}\ \varphi_0 = 0^o$ $I_+ = 84.1A_{rms}\ \varphi_+ = -21.9^o$ $I_- = 16.7A_{rms}\ \varphi_- = -56.7^o$ $I_0 = 16.7A_{rms}\ \varphi_0 = 63.6^o$	$V_+ = 218.3V_{rms}\ \varphi_+ = 1.8^o$ $V_- = 4.5V_{rms}\ \varphi_- = 126.2^o$ $V_0 = 2.3V_{rms}\ \varphi_0 = -104.5^o$ $I_+ = 84.1A_{rms}\ \varphi_+ = -21.9^o$ $I_- = 16.7A_{rms}\ \varphi_- = -56.7^o$ $I_0 = 16.7A_{rms}\ \varphi_0 = 63.2^o$
Active and Solar Generation Enabled (No Zero Sequence Compensation)	$V_+ = 228.4V_{rms}\ \varphi_+ = 0.9^o$ $V_- = 2.4V_{rms}\ \varphi_- = 123.0^o$ $V_0 = 9.1V_{rms}\ \varphi_0 = -115.9^o$ $I_+ = 88.5A_{rms}\ \varphi_+ = -19.8^o$ $I_- = 17.7A_{rms}\ \varphi_- = -60.4^o$ $I_0 = 16.7A_{rms}\ \varphi_0 = 60.7^o$	$V_+ = 240.3V_{rms}\ \varphi_+ = 0.8^o$ $V_- = 0.1V_{rms}\ \varphi_- = 0^o$ $V_0 = 0.4V_{rms}\ \varphi_0 = 0^o$ $I_+ = 84.1A_{rms}\ \varphi_+ = -21.4^o$ $I_- = 16.7A_{rms}\ \varphi_- = -59.2^o$ $I_0 = 16.7A_{rms}\ \varphi_0 = 60.7^o$	$V_+ = 229.5V_{rms}\ \varphi_+ = 1.7^o$ $V_- = 2.3V_{rms}\ \varphi_- = 126.0^o$ $V_0 = 9.1V_{rms}\ \varphi_0 = -114.1^o$ $I_+ = 84.1A_{rms}\ \varphi_+ = -21.4^o$ $I_- = 16.7A_{rms}\ \varphi_- = -59.2^o$ $I_0 = 16.7A_{rms}\ \varphi_0 = 60.7^o$
Active and Solar Generation Enabled (Zero Sequence Compensated)	$V_+ = 228.6V_{rms}\ \varphi_+ = 0.9^o$ $V_- = 2.5V_{rms}\ \varphi_- = 125.6^o$ $V_0 = 0.3V_{rms}\ \varphi_0 = 0^o$ $I_+ = 87.2A_{rms}\ \varphi_+ = -22.2^o$ $I_- = 18.5A_{rms}\ \varphi_- = -57.4^o$ $I_0 = 0.6A_{rms}\ \varphi_0 = 148.7^o$	$V_+ = 240.5V_{rms}\ \varphi_+ = 1.4^o$ $V_- = 1.3V_{rms}\ \varphi_- = 127^o$ $V_0 = 0V_{rms}\ \varphi_0 = 0^o$ $I_+ = 84.1A_{rms}\ \varphi_+ = -21.6^o$ $I_- = 16.7A_{rms}\ \varphi_- = -58.2^o$ $I_0 = 16.7A_{rms}\ \varphi_0 = 61.7^o$	$V_+ = 229.6V_{rms}\ \varphi_+ = 2.4^o$ $V_- = 3.6V_{rms}\ \varphi_- = 125.7^o$ $V_0 = 2.3V_{rms}\ \varphi_0 = -115.1^o$ $I_+ = 84.1A_{rms}\ \varphi_+ = -21.6^o$ $I_- = 16.7A_{rms}\ \varphi_- = -58.2^o$ $I_0 = 16.7A_{rms}\ \varphi_0 = 61.7^o$

From the simulation, it is clearly seen that the compensator, when in active state with zero sequence compensation mode, adjusts the voltages at the a,b,c,n output terminals and forces the zero sequence voltages to zero, $V_0 = 0V_{rms}$ and eliminates about 97% of the zero sequence current from the A,B,C,N input terminals. The UPFC based compensator equipped with zero sequence current compensation increases the input positive sequence current to provide the real power requirement to correct the positive sequence voltage drop. At the same time, the negative sequence current is slightly increased to provide the oscillatory power necessary to eliminate the negative and zero sequence voltages at the regulator output terminals. In this case, the negative sequence current is slightly greater to provide the additional oscillatory power demand.

4.3.2. UPFC with zero sequence and reactive current compensation

Table 4.4 outlines the steady state regulatory performance of the 4+4 leg UPFC based compensator with the solar generation in service with zero sequence and reactive current compensation together. In this case, the power factor of the loads is taken to be 0.90 lagging. The reactive current control is to supply or absorb the reactive current demand of load locally through the shunt converter.

Table 4.4 Input and output voltages and currents with zero sequence current and reactive current compensation

Regulator State	Terminals A,B,C,N	Terminals a,b,c,n	Consumer Terminals
Inactive and Solar Generation Enabled (No zero sequence and reactive current compensation)	V_+ =229.7$V_{rms}\varphi_+$= 1.29º V_- = 2.27$V_{rms}\varphi_-$= 124.7º V_0 = 9.08$V_{rms}\varphi_0$= -115.5º I_+ = 84.7$A_{rms}\varphi_+$= -30.14º I_- = 16.67$A_{rms}\varphi_-$= -58.76º I_0 = 16.67$A_{rms}\varphi_0$= 61.01º	V_+ =229.7$V_{rms}\varphi_+$= 1.29º V_- = 2.27$V_{rms}\varphi_-$= 124.7º V_0 = 9.08$V_{rms}\varphi_0$= -115.5º I_+ = 85.13$A_{rms}\varphi_+$= -30.56º I_- = 16.67$A_{rms}\varphi_-$= -58.74º I_0 = 16.67$A_{rms}\varphi_0$= 61.11º	V_+ = 219.5$V_{rms}\varphi_+$= 2.73º V_- = 4.54$V_{rms}\varphi_-$= 124.7º V_0 = 11.36$V_{rms}\varphi_0$= -115.5º I_+ = 85.13$A_{rms}\varphi_+$= -30.56º I_- = 16.67$A_{rms}\varphi_-$= -58.74º I_0 = 16.67A_{rms} φ_0= 61.11º
Inactive and Solar Generation Enabled (Zero sequence and reactive current compensation)	V_+ = 229.9$V_{rms}\varphi_+$= -0.14º V_- = 2.26$V_{rms}\varphi_-$= 124.7º V_0 = 0.35V_{rms} φ_0= 0º I_+ =73.4$A_{rms}\varphi_+$=-0.13º I_- = 16.63$A_{rms}\varphi_-$= -58.71º I_0 = 0.65$A_{rms}\varphi_0$= 146.8º	V_+ = 229.9$V_{rms}\varphi_+$= -0.11º V_- = 2.28$V_{rms}\varphi_-$= 124.7º V_0 = 0.35$V_{rms}\varphi_0$= 0º I_+ = 84.92$A_{rms}\varphi_+$= -30.31º I_- = 16.67$A_{rms}\varphi_-$= -60.19º I_0 = 16.67$A_{rms}\varphi_0$= 59.76º	V_+ =219.69$V_{rms}\varphi_+$=1.217º V_- = 4.53$V_{rms}\varphi_-$= 123.9º V_0 = 2.31$V_{rms}\varphi_0$= -108º I_+ = 84.92$A_{rms}\varphi_+$= -30.31º I_- = 16.67$A_{rms}\varphi_-$= -60.19º I_0 = 16.67$A_{rms}\varphi_0$= 59.76º
Active and Solar Generation Enabled (No zero sequence and reactive current compensation)	V_+ = 229.1$V_{rms}\varphi_+$= 1.28º V_- = 2.4$V_{rms}\varphi_-$= 123º V_0 = 9.0V_{rms} φ_0= -115.5º I_+ = 88.52$A_{rms}\varphi_+$= -28.81º I_- = 16.67$A_{rms}\varphi_-$= -60.42º I_0= 16.66$A_{rms}\varphi_0$= -61.09º	V_+ = 240.3$V_{rms}\varphi_+$= 1.2º V_- = 0.07$V_{rms}\varphi_-$= 0º V_0 = 0.28$V_{rms}\varphi_0$= 0º I_+ = 85.06$A_{rms}\varphi_+$= -30.53º I_- = 16.67$A_{rms}\varphi_-$= -58.74º I_0 = 16.67$A_{rms}\varphi_0$= 61.18º	V_+ = 230.2$V_{rms}\varphi_+$= 2.57º V_- = 2.27$V_{rms}\varphi_-$= 126.5º V_0 = 2.3$V_{rms}\varphi_0$= -108.4º I_+ = 85.06$A_{rms}\varphi_+$= -30.53º I_- = 16.67$A_{rms}\varphi_-$= -58.74º I_0 = 16.67$A_{rms}\varphi_0$= 61.18º
Active and Solar Generation Enabled (Zero sequence and reactive current compensation)	V_+ = 229.4$V_{rms}\varphi_+$= -0.15º V_- = 2.5V_{rms} φ_-= 123.2º V_0 = 0.35V_{rms} φ_0= 0º I_+ = 77.14$A_{rms}\varphi_+$= -0.14º I_- = 20.40$A_{rms}\varphi_-$= -60.22º I_0= 0.65$A_{rms}\varphi_0$= 146.8º	V_+ = 240.3$V_{rms}\varphi_+$= -0.23º V_- = 0.07V_{rms} φ_-= 0º V_0 = 0.01$V_{rms}\varphi_0$= 0º I_+ = 88.92$A_{rms}\varphi_+$= -30.29º I_- = 16.67$A_{rms}\varphi_-$= -60.17º I_0 = 16.7$A_{rms}\varphi_0$= 59.45º	V_+ = 230$V_{rms}\varphi_+$= 1.06º V_- = 2.27$V_{rms}\varphi_-$= 125.1º V_0 = 2.26$V_{rms}\varphi_0$= -116.8º I_+ = 88.24$A_{rms}\varphi_+$= -21.6º I_- = 16.7$A_{rms}\varphi_-$= -58.2º I_0 = 16.7$A_{rms}\varphi_0$= 59.75º

From the simulation, it is clearly seen that the UPFC based compensator, when in active state with reactive current and zero sequence current compensation, adjusts the voltages at a,b,c,n output terminals and reduces the positive sequence current drawn from terminals

A,B,C,N while forcing the negative and zero sequence voltages nearly to zero. As expected with reactive current compensation, the input positive sequence current drawn from terminals A,B,C,N decreases and follows the same phase angle as input positive voltages as seen from Table 4.4. The loads meet the reactive current demand locally from the shunt converter instead of taking current from terminals A,B,C,N and working at unity power factor. Since the shunt converter is now drawing a zero sequence and reactive compensation current, this will cause some oscillatory power fluctuation at the DC bus. This will cause the negative sequence current to slightly increase to provide the additional oscillatory power demand and eliminate the negative and zero sequence voltages at the regulator output terminals.

The dynamic response of the UPFC based compensator equipped with reactive current and zero sequence current compensation is explored in Figures 4.11 to 4.18. The compensator is allowed to settle into steady state operation with a balanced $100A_{rms}$ 0.9 power factor lagging load. At t = 0.5067s, the voltage zero crossing in "b" phase, a $50A_{rms}$ unity power factor solar generator commences its operation. The solar current ramps up over one 20ms cycle and reaches its full current at t = 0.5267s. The performance of the proposed voltage regulator with reactive current and zero sequence current compensator is explored in Figure 4.11. The input voltages prior to t = 0.5067s are balanced but low. When the solar generation commences its operation at phase "b", the input voltage at phase "b" (green) rises slightly as the phase current reduces. It is observed that the voltages at a,b,c,n output terminals are constant and well regulated.

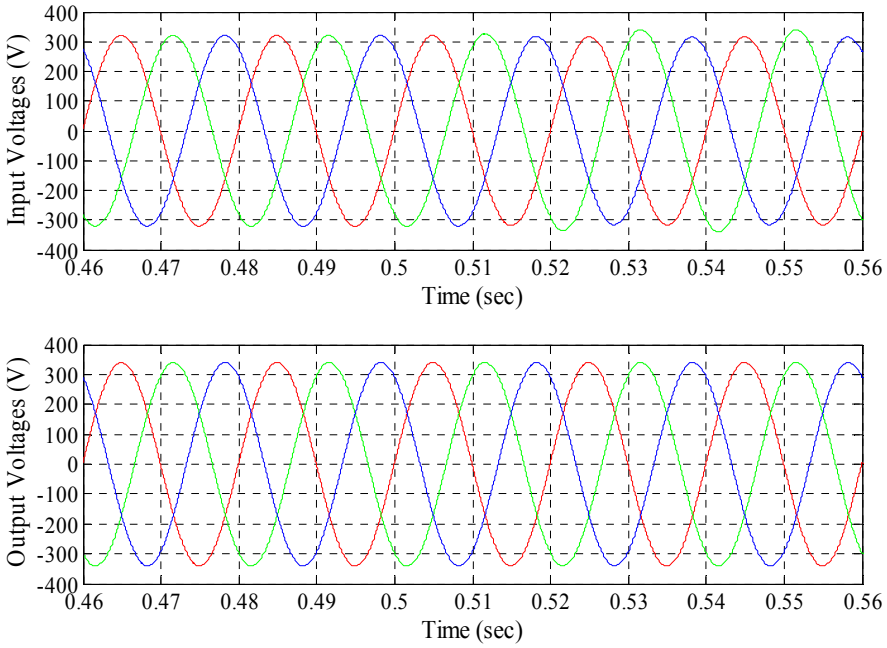

Figure 4.11 Voltages at A,B,C,N input and a,b,c,n output terminals with zero sequence and reactive current compensation

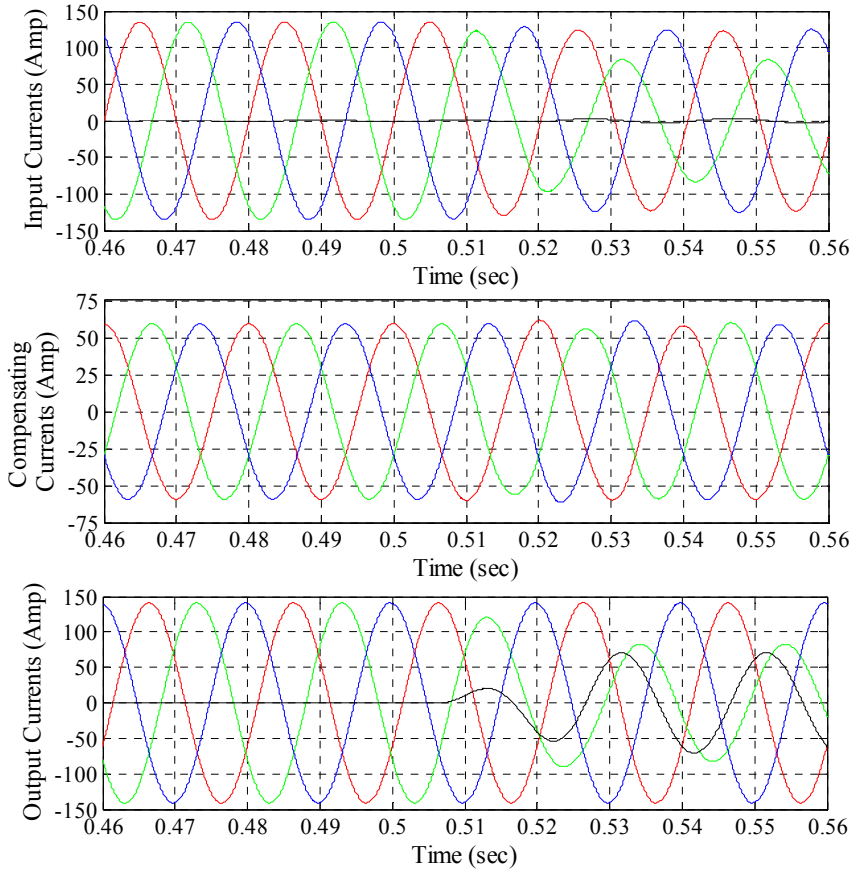

Figure 4.12 Currents from A,B,C,N input and a,b,c,n output terminals and injected compensating currents with zero sequence and reactive current compensator

Figure 4.12 demonstrates the performance of the reactive current and zero sequence current compensator used in the UPFC based compensator. The upper trace represents the currents from input terminals which are zero sequence and reactive current compensated. The input currents reduce in magnitude because of the reactive current compensation. The middle trace shows the compensating current supplied to the loads by the shunt converter which is purely orthogonal to the input currents. The lower trace shows the output currents from a,b,c,n output terminals and the phase currents are slightly higher in magnitude than that of the input currents. Figure 4.13 shows the voltage and current waveforms upstream of the UPFC based compensator. The input voltages and input currents are in the same phase which implies that the system is operating at unity power factor regardless of the load power factor which is chosen to be 0.9 lagging. Due to this reactive power compensation, the input currents only have real current components and the components of reactive current demand are supplied to the loads by the shunt converter.

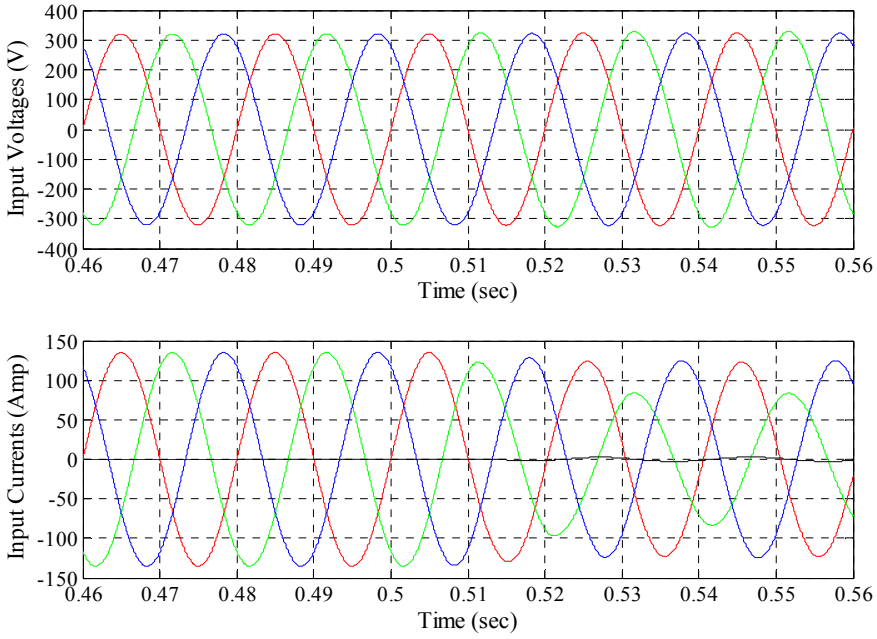

Figure 4.13 Input voltages at terminals A,B,C,N and input currents from terminals A,B,C,N of the voltage regulator with zero sequence and reactive current compensator

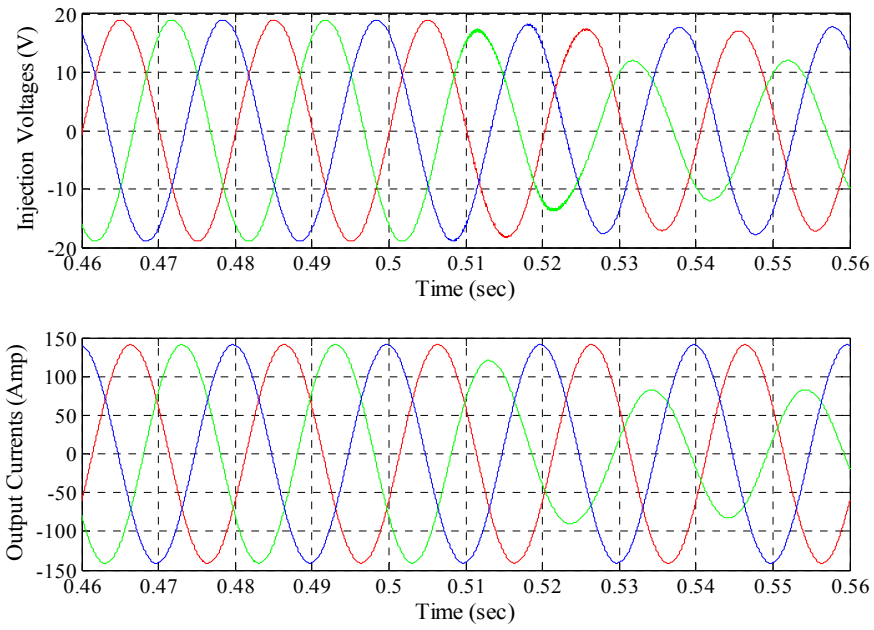

Figure 4.14 Series injection voltages and output currents from terminals a,b,c,n

The response of the series injection converter is shown in Figure 4.14. Prior to t = 5067s, the injected voltage in all three phases are completely balanced but slightly reduced. This is because the real power demand by the series converter is now reduced to 3.8kW due to the reactive current compensation. After t = 0.5067s when solar generator commences in phase “b” (green), the current in phase “b” (green) reduces significantly over one cycle which consequently lowers the voltage injected in phase “b” (green), seen in the upper trace.

The response of the parallel converter equipped with zero sequence and reactive current compensation is demonstrated in Figure 4.15. Prior to t = 0.5067s, the input current is balanced and the UPFC based compensator adds only a balanced positive sequence voltage to control the voltages at a,b,c,n output terminals. The real power requirement is now about 3.8kW. Once the solar generation starts, the real power requirement drops and an oscillatory power requirement develops. The shunt converter also draws the reactive component of input current for reactive compensation for the feeder.

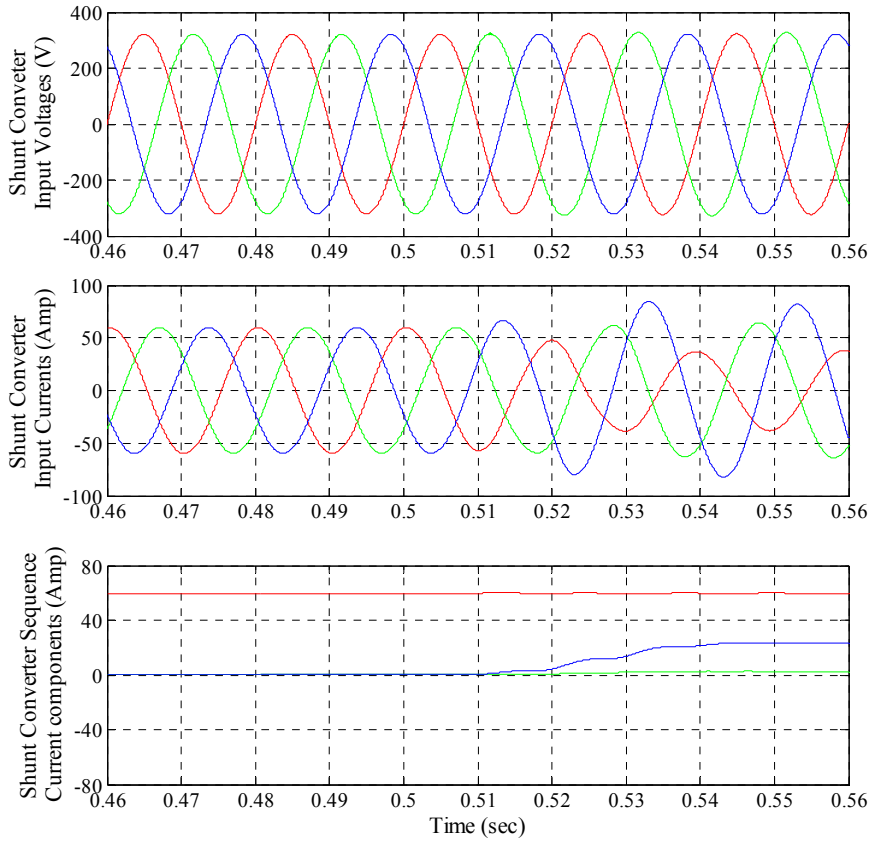

Figure 4.15 Shunt converter input voltages and currents with their sequence components (+ve sequence, red; -ve sequence, green; zero sequence, blue) with zero sequence and reactive current compensation

This increases the currents through the shunt converter as seen in the middle trace. The lower trace shows the shunt converter currents in terms of their sequence current components. The shunt converter draws only positive sequence current before the solar generator operates, and starts to draw zero sequence current and a degree of negative sequence current when solar generation commences. Figure 4.16 shows the positive sequence current control system and control of the DC bus voltage when the regulator is equipped with zero sequence and reactive current compensator. As the solar generation commences, the line currents become unbalanced and the series converter demands a lower average power, shown as the upper blue trace. The parallel converter, the upper red trace, should rapidly follow the power demand to control the DC bus capacitor voltage shown as the second trace. The positive sequence current forward system has a minimum 10ms

response time and the demand signal is shown as the third trace. The capacitor voltage regulation loop, the demand signal of which is shown as the fourth trace, is slow responding and only corrects any minor tracking errors in the feed forward system. The instantaneous power balance causes the capacitor voltage to rise rapidly. Once the capacitor voltage reaches 800Vdc, the instantaneous voltage limit system becomes active as shown in the lower trace. This instantaneously reduces the positive sequence current drawn by the parallel converter, thus limiting the voltage rise. From t = 0.55s, the instantaneous loop is inactive and the normal voltage control loop can rebalance the capacitor power and voltage as seen in Figure 4.16.

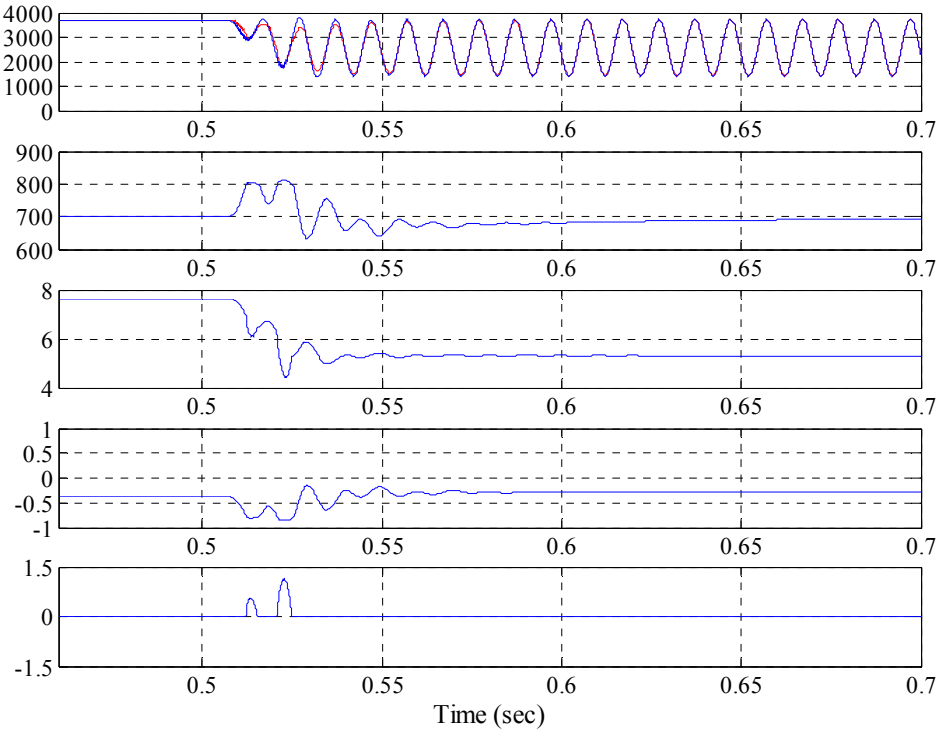

Figure 4.16 Top traces: series converter power (blue) and shunt converter power (red). Other traces top to bottom: DC bus voltage; positive sequence current demand feed forward signal; DC bus voltage regulator current demand; Instantaneous bus voltage current demand

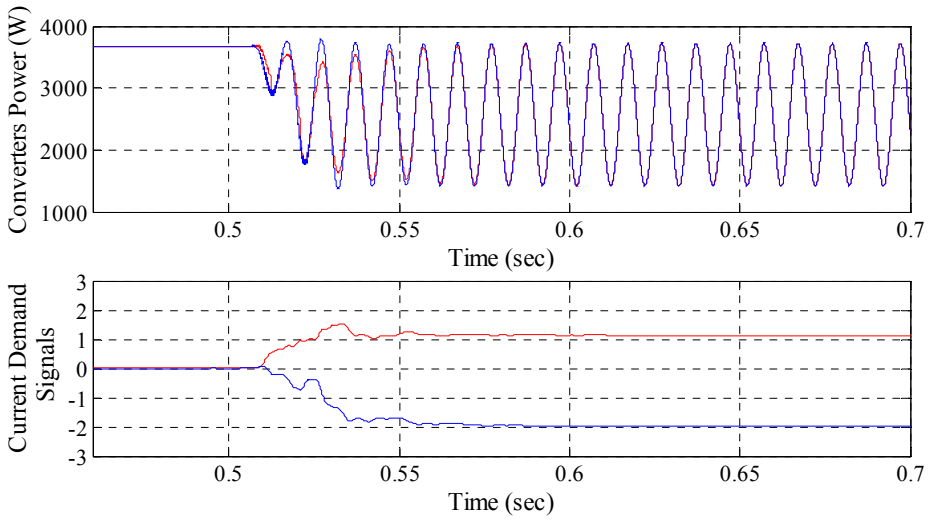

Figure 4.17 Series converter power (blue) and shunt converter power (red), and current demand signals for negative sequence cosine (blue) and sine (red) terms

Figure 4.17 shows the actions of the 2ω control loops. Prior to t = 0.5067s, the operation of the 2ω control loops is inactive. When the solar generator commences its operation at t = 0.5067s, the oscillatory power requirement develops and the 2ω control amplifiers begin to demand negative sequence sine and cosine currents to eliminate the oscillatory power fluctuation as shown in the lower traces. The effectiveness of the control systems in managing the DC bus capacitor voltage with zero sequence and reactive current controllers is illustrated in Figure 4.18. To do so, the instantaneous voltage limit control system and the 2ω control loops are turned off. From t = 0.5067s, the parallel converter cannot track the 2ω power oscillations and the DC bus voltage regulators and feed forward systems cannot respond rapidly to the capacitor voltage rise. The DC bus voltage rises sharply and exceeds 800Vdc, as seen in the second trace. The DC bus average voltage does slowly reduce, but the capacitor voltage has a sustained 2ω voltage ripple as the small capacitor is forced to absorb the oscillatory power.

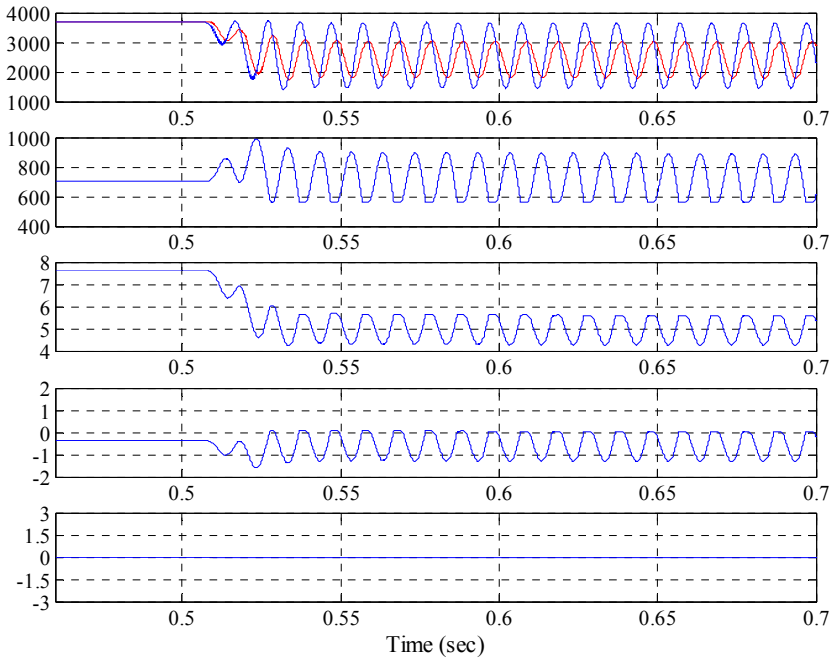

Figure 4.18 Top traces: series converter power (blue) and shunt converter power (red). Other traces top to bottom: DC bus voltage; positive sequence current demand feed forward signal; DC bus voltage regulator current demand; Instantaneous bus voltage current demand

4.4. Application of UPFC based compensator for active filtering

Nonlinear loads with PV penetration are used to demonstrate the active filtering capability of the UPFC based compensator as shown in Figure 4.19. The nonlinear loads are designed as a combination of balanced $100A_{rms}$ 0.95 power factor lagging loads and $5A_{rms}$ 5^{th} harmonic loads. A switchable $50A_{rms}$ unity power factor load is connected at phase "b". The four-leg UPFC based compensator is connected to a LV distribution aerial feeder, commonly used in Australian distribution networks. The transformer and feeder parameters used in this simulation are kept exactly the same as that considered for the simulation of the UPFC based voltage regulator in section 4.2. In this simulation model, the UPFC is additionally equipped with the harmonic compensator to have active filtering capability. During the simulation, apart from the harmonic compensation, the zero sequence and reactive current compensation modes will also remain active. However, the active filtering capability of the UPFC and its control at the presence of nonlinear loads are discussed through simulation results as the operation of zero sequence and reactive current

compensator with their controls are previously explained through a series of simulation conducted in section 4.3. The controllers and other parameters used in this simulation are listed in Tables 4.5 and 4.6 respectively.

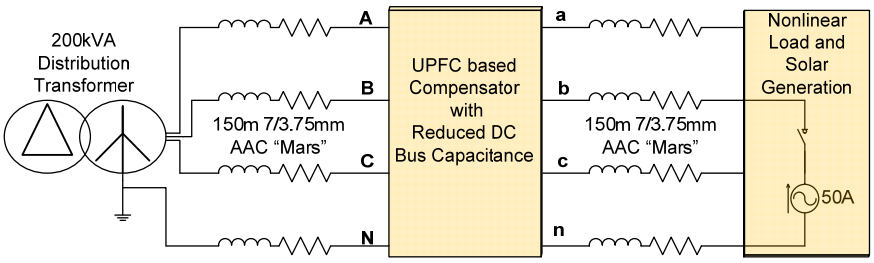

Figure 4.19 Application of 4+4 leg UPFC based compensator for active filtering in LV distribution feeders

Table 4.5 PI controllers used in the simulation

PI Controllers	Proportional gain, K_p	Integral gain, K_i
Harmonic compensator, G_{chABC} (s)	$\frac{100000}{s+10000}$	
DC bus voltage regulator, G_{cdc} (s)	0.04	0.4
DC bus instantaneous voltage limit regulators, G_{cinst} (s)	0.1 only if $V_{dc} > 624V$	0
2ω oscillatory power compensators, $G_{c2\omega}$(s)	1	100

Table 4.6 Different parameters used in the simulation and their values

Parameters	Value
DC bus capacitor	100μF
Vdc set point	600V
Vdc upper limit	624V
Series injection controlled voltage source gain	1
DC bus voltage regulator current limit	10A peak
5^{th} harmonic balanced currents magnitude	7.07A peak

4.4.1. Simulation results for 4+4 leg UPFC based active filter

The dynamic current and voltage responses of the UPFC based compensator for active filtering are presented in Figures 4.20 and 4.21 respectively. The active filtering capability of the UPFC based compensator and action of harmonic compensation is well

demonstrated in Figurer 4.20. The top trace shows the supply side source currents from A,B,C,N terminals which have no harmonic content after active filtering. Prior to t = 0.5067s, the source current is completely harmonic free, balanced and sinusoidal. After t = 0.5067s when solar generation commences in phase “b”, the phase “b” current (green) is reduced and source current becomes unbalanced but still harmonic free. The middle trace shows the output currents from the a,b,c,n terminals which have the harmonic content. The lower trace illustrates the full current compensation role of the UPFC based compensator while working as active filter.

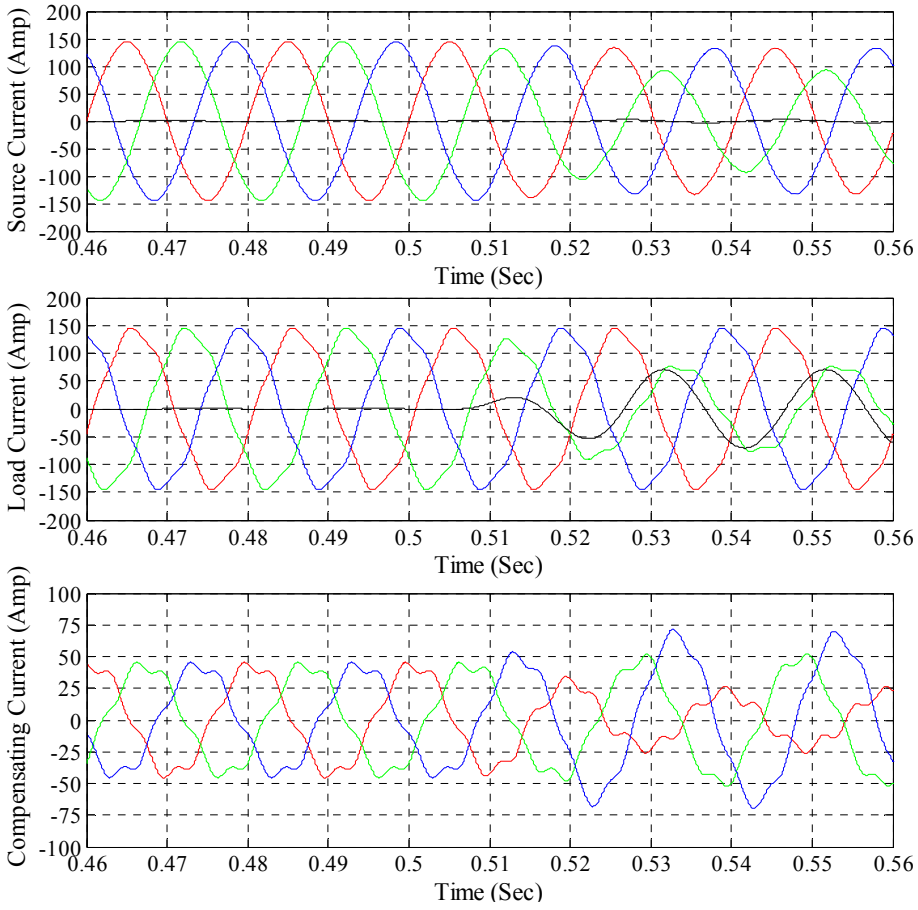

Figure 4.20 Source currents from A,B,C,N input terminals, load currents from a,b,c,n output terminals and the compensating currents

The parallel converter draws composite currents to compensate harmonic current, reactive current, neutral current and a degree of negative and positive sequence current. Prior to t = 0.5067s, the composite compensating current is balanced but has a harmonic content. The

effect of neutral current compensation is seen from the top and middle traces. The source and load currents are balanced and produce zero neutral current (black) until solar generation comes into operation. After solar generation commences, the source and load currents become unbalanced and the fourth conductor carries the neutral current. The neutral current or zero sequence current (black) is effectively eliminated upstream of the UPFC based compensator. Figure 4.21 shows the response of input voltage, output voltage and the DC bus voltage when the UPFC is operated in voltage regulation with parallel compensation mode.

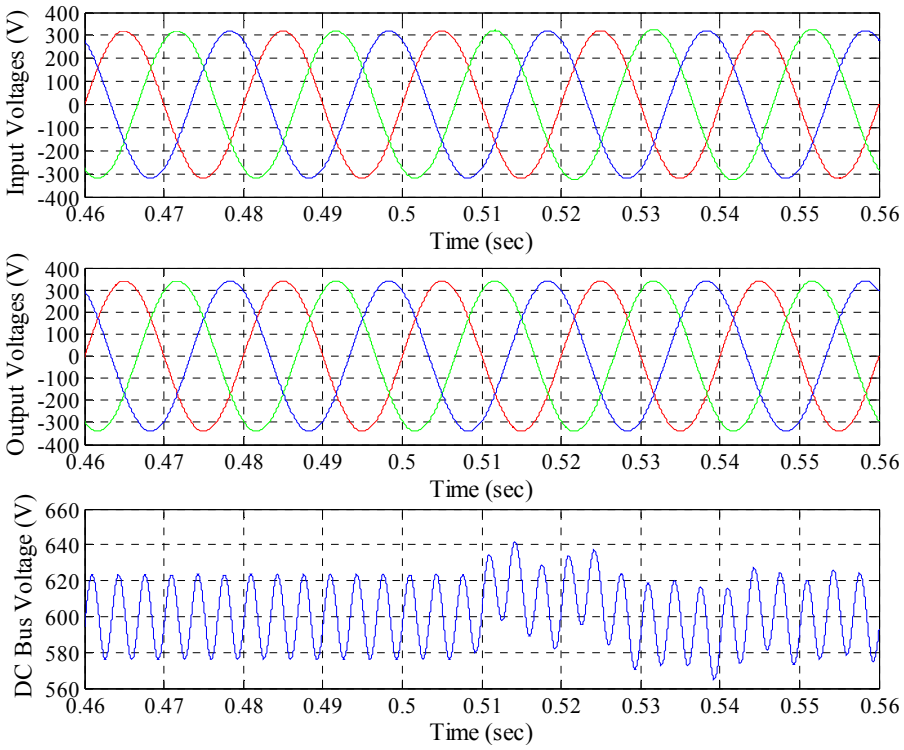

Figure 4.21 Input voltages at A,B,C,N terminals, output voltages at a,b,c,n terminals and the DC bus voltage

Due to the action of 2ω control amplifiers during any unbalanced operation of load, the parallel converter is clearly forced to carry the 2ω power fluctuations and these do not appear on the DC bus. Inspection of equation (29) shows that, if the parallel converter takes the additional action of 5th harmonic current compensation, a 6ω oscillation will appear at the DC bus capacitor. In this work, this large fluctuation is internalised at the DC

bus by slightly increasing the capacitor size rather than passing it through the shunt converter which requires the shunt converter to draw harmonic currents. The DC bus voltage operating range is $V_L = 560$ to $V_U = 624$Vdc. Applying equation (32) shows that a 100μF polypropylene DC bus capacitor is sufficient to effectively internalise the fluctuations due to harmonic current compensation. The lower trace shows that the DC bus capacitor exceeds the upper limit of operating voltage band 624Vdc during the transient period when solar commences operation and reaches a steady state condition within 15ms. In this case, the instantaneous voltage limit system becomes active and limits the voltage rise by reducing the positive sequence current drawn by the parallel converter.

4.5. Conclusion

In this chapter, a 4+4 leg UPFC based compensator is demonstrated for providing voltage and current compensation for LV distribution networks. Initially, the UPFC based compensator is equipped with zero sequence and reactive current controllers and is shown capable of actively regulating the positive, negative, and zero sequence voltages at the output terminals. At the same time, the regulator is capable of reactive current, zero sequence or neutral current compensation and a degree of negative sequence current compensation. The compensator can effectively meet the requirement of reactive power demanded by the load which reduces the current from upstream of the UPFC based compensator. Thus the power factor upstream of the UPFC based compensator becomes unity. The neutral current is eliminated from upstream of the UPFC based compensator by the action of the zero sequence current controller. Instantaneous reactive power theory has been applied to ensure the 2ω power fluctuations can be compensated by allowing the input shunt converter to draw a negative sequence current. In the steady state, 2ω voltage fluctuations are removed from the DC bus capacitor voltage. Suppression of 2ω voltage fluctuations are activity performed by controlling the shunt converter negative sequence

current. Thus, the UPFC based compensator is designed and simulated to work as an active filter with the design of a harmonic compensator. The UPFC based compensator is loaded with nonlinear load and solar generations for simulation of active filtering capability. This device is shown to be capable of actively removing the harmonic component from the supply side source current. Instantaneous reactive power theory shows that 2ω and 6ω voltage oscillations will be present at the DC bus. The 2ω voltage oscillations are removed from the DC bus by controlling the shunt converter negative sequence current, while 6ω fluctuations are internalised with a slightly larger capacitor of 100μF.

Chapter 5 HARDWARE AND EXPERIMENTAL RESULTS

5.1. Introduction

Once proper operation of the UPFC was confirmed with a series of simulations conducted in Matlab, the laboratory scale prototype of the UPFC based compensator was designed for the experimental testing. The hardware is designed to operate at 400/230Vac with 400Vdc bus voltage. For safety reason, the experimental work presented here was conducted at reduced voltages at 40/23Vac and 40Vdc.

In this chapter, the internal architecture of the laboratory prototype is presented and discussed. A three degree of freedom space vector modulation method for the series and shunt converters of the UPFC based compensator is also described and the method of calculating duty cycles from three independent voltages specified in abc coordinates is provided. A three phase PLL which is used to synchronise the grid with converter voltages of the UPFC is presented. The input filter and its design considerations are also presented and described with their appropriate frequency response and time domain step response.

This chapter contains three experimental tests which are conducted at low voltage. These tests exercise the key operational features of the UPFC. These are:

- A demonstration of the voltage regulation characteristics of the series converter;
- A demonstration of the current regulation characteristics of the shunt converter;
- A demonstration of the regulation of the DC bus voltage by the input converter.

These tests were selected to demonstrate the most important features of the converter in the limited time available for the experimental testing. The following individuals are recognised for their contributions to the production of the experimental equipment:

- Mr Ben Sneath undertook the hardware construction using hardware designs provided by Professor Wolfs;

- Mr Mark Hayman provided the coding for the SVM algorithm for the Delfino processor. This algorithm had been previously coded by Mr Hayman for use in an unrelated DSTATCOM project based on an Infineon processor. Source code, for an Infineon processor, for the PLL was provided from that project.

The candidate undertook the subsequent programming tasks required to implement the three laboratory tests.

5.2. Phase locked loop

Accurate frequency and phase angle measurement of the power system voltage is required for many applications where precise voltage synchronisation is essential. For example, the reliable control of power electronics converters in distribution systems for voltage regulation requires the phase and frequency of line voltages to be synchronised with the phase and frequency of converter output voltage. A PLL is generally used for voltage synchronisation which requires the measurement of frequency and phase angle of the line voltage. The PLL proposed in [121] based on the two wattmeter method check and is implemented to provide synchronization for the four-leg UPFC based compensator as shown in Figure 5.1. The phases to neutral voltages are designated as sinusoidal reference set. The method requires the measurement of two sinusoidal line-to-line voltages which are compared to a cosine reference set to produce the phase error, φ_e signal. The respective three phase cosine reference set is as follows:

$$R_a\, C = cos(\omega t) \tag{33}$$

$$R_b\, C = cos(\omega t - 2\pi/3) \tag{34}$$

$$R_c\, C = cos(\omega t + 2\pi/3) \tag{35}$$

The phase error signal is proportional to the sine of the angular difference and can be calculated as:

$$\varphi_e = V_{ab} \times R_a C + V_{cb} \times R_c C \tag{36}$$

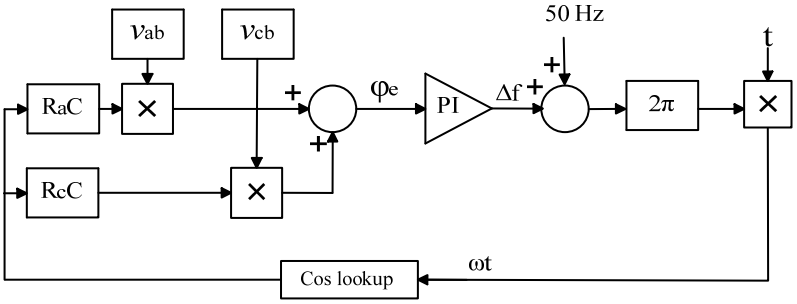

Figure 5.1 PLL based on power measurement by two wattmeter method principle [121]

The PI controller drives the phase error signal and produces a frequency, Δf, which follows the frequency of the line voltages of the grid and accordingly tries to catch up or slow down. Then the integrator integrates its actual frequency, $\Delta f + 50$, to produce its actual phase angle at the output of integrator. The three phase reference cosine values are then calculated corresponding to the actual value of the phase angle. In the DSP implementation, the Cos lookup function in the figure is implemented using a sinusoidal function look up table. The table covers 360 degrees in 0.1 degree steps. The sine function values are real values in single precision floating point. The PI controllers tuning parameters are mentioned in Table 5.1.

Table 5.1 Tuning parameters of the PLL

Parameters	Values
K_p	0.1
K_i	50×10^{-6}

5.3. Three dimensional space vector modulation

In conventional three-leg inverters, two dimensional space vector modulation techniques are used to generate an average voltage vector equal to the reference voltage vector. The four-leg converter has an additional degree of freedom which requires an extension of the modulation method. Three-dimensional space vector modulation (3-D-SVM) in abc coordinates as proposed in [100] is used as the modulation technique for the four-leg voltage source converter (VSI) in this experimental work. This method is equivalent to [99]

with the only difference being that, rather than expressing the input voltages in $\alpha\beta\gamma$ coordinates as in [99], they are expressed in abc coordinates. This greatly simplifies the selection of tetrahedron and the calculation of switching times.

Table 5.2 Switching states, voltage terminals and switching vectors in abc coordinates [100]

State	s_f	s_a	s_b	s_c	v_{af}	v_{bf}	v_{cf}	Vector
1	0	0	0	0	0	0	0	V1
2	0	0	0	1	0	0	1	V2
3	0	0	1	0	0	1	0	V3
4	0	0	1	1	0	1	1	V4
5	0	1	0	0	1	0	0	V5
6	0	1	0	1	1	0	1	V6
7	0	1	1	0	1	1	0	V7
8	0	1	1	1	1	1	1	V8
9	1	0	0	0	-1	-1	-1	V9
10	1	0	0	1	-1	-1	0	V10
11	1	0	1	0	-1	0	-1	V11
12	1	0	1	1	-1	0	0	V12
13	1	1	0	0	0	-1	-1	V13
14	1	1	0	1	0	-1	0	V14
15	1	1	1	0	0	0	-1	V15
16	1	1	1	1	0	0	0	V16

In Table 5.2, the sixteen switching combinations of the converter are presented for the four-leg VSC topology as shown in Figure 2.13, expressing the switching vectors in abc coordinates. To simplify the notation, the vectors are normalised by dividing them by V_{dc}. Using this representation, it is evident that the vectors are all in the vertices of two cubes, with an edge length of one: one of them is placed in the "all positive" region (defined by vectors V1 to V8) and the other is in the "all negative" region (defined by vectors V9 to V16) as represented in Figure 5.2. The common vertex of both cubes represents, precisely, the zero voltage of a double vector (V1 and V16). Joining the corresponding vertices of the two cubes, the region included in this dodecahedron is completely equivalent to the one that appears in the $\alpha\beta\gamma$ representation [99], but the distribution of the switching voltage vectors appears more clearly, allowing the development of simpler 3-D-SVM algorithms.

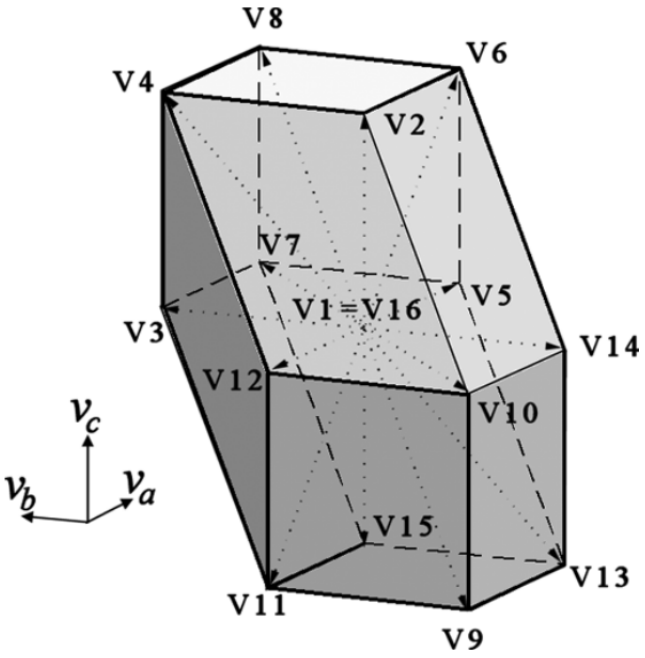

Figure 5.2 Dodecahedron that contains the control region, in abc coordinates, showing the switching vectors [100]

The planes that define the control region of the four-leg converter topology of Figure 2.13, in which the voltage vectors will be included, present very simple expressions. Six of them are parallel to the coordinate planes, expressed by the equations $v_a = \pm 1$, $v_b = \pm 1$ and $v_c = \pm 1$. These planes define a cube, with edge equal to 2, containing the control region. These planes represent the conditions that every phase-neutral voltage must be less than or equal to the DC-link voltage in a given interval. The other six planes form a 45° angle over the coordinate planes, and their equations are also very simple: $v_a - v_b = \pm 1$, $v_b - v_c = \pm 1$, $v_c - v_a = \pm 1$. These planes express the conditions that force the line (or phase-to-phase) voltages to be less than or equal to the DC-link voltage. The dodecahedron shown in Figure 5.2 can be split into 24 tetrahedrons, each of which contain three non-zero switching vectors (NZSVs) along with the zero (double) vector [99]. In Figure 5.3, the different tetrahedrons are shown where each cube is divided into six tetrahedrons and the intermediate region is divided into twelve tetrahedrons. All of the tetrahedrons are equal in size, providing a symmetrical division of the control region.

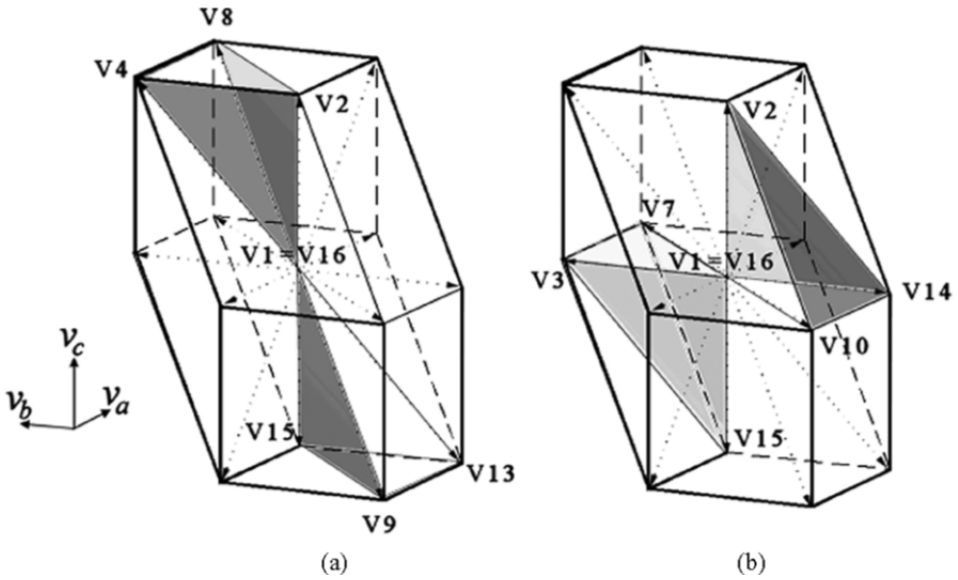

Figure 5.3 Representation of some of the obtained tetrahedrons (a) Regions RP = 8 and RP = 57. (b) Regions RP = 13 and RP = 52 [100]

Therefore, using the equations of these planes, it can be determined in which of the 24 tetrahedrons any voltage vector is included. A very efficient way to make the selection of the tetrahedron is presented as [100]:

$$C_1 = Sign(INT(v_{a\_ref} + 1)) \tag{37}$$

$$C_2 = Sign(INT(v_{b\_ref} + 1)) \tag{38}$$

$$C_3 = Sign(INT(v_{c\_ref} + 1)) \tag{39}$$

$$C_4 = Sign(INT(v_{a_{ref}} - v_{b\_ref} + 1)) \tag{40}$$

$$C_5 = Sign(INT(v_{b_{ref}} - v_{c\_ref} + 1)) \tag{41}$$

$$C_6 = Sign(INT(v_{a\_ref} - v_{c\_ref} + 1)) \tag{42}$$

Each of the above equations for C_i represents the six indexes representing one of the six planes and the voltages are the reference voltage vectors normalised with V_{dc}. The operator INT(x) represents the integer part of x and Sign(x) extracts the sign of x, being 1 if x is

positive, -1 if x is negative, and 0 if x equals zero. Then a pointer to the region in which the reference vector is included can be calculated as [100]:

$$RP = 1 + \sum_{i=1}^{6} C_i \times 2^{(i-1)} \tag{43}$$

Though the pointer RP is theoretically ranged from 1 – 64, it will adopt only one of 24 different possible values that correspond to the 24 tetrahedrons, as all of them are not independent and are composed of three NZSVs (*Vd1*, *Vd*2, *Vd*3) and the double zero voltage vector (*Vd0*). Table 5.3 shows the 24 tetrahedrons with their RP indexes and the three NZSVs. Once the NZSVs are selected, the next decision concerns the switching pattern to be applied. In this application, the selection of the switching pattern was made based on a minimum commutation criterion.

Table 5.3 Region pointer of the 24 tetrahedrons and their NZSV vectors [100]

RP	*Vd*1	*Vd*2	*Vd*3	RP	*Vd*1	*Vd*2	*Vd*3
1	V9	V10	V12	41	V9	V13	V14
5	V2	V10	V12	42	V5	V13	V14
7	V2	V4	V12	46	V5	V6	V14
8	V2	V4	V8	48	V5	V6	V8
9	V9	V10	V14	49	V9	V11	V15
13	V2	V10	V14	51	V3	V11	V15
14	V2	V6	V14	52	V3	V7	V15
16	V2	V6	V8	56	V3	V7	V8
17	V9	V11	V12	57	V9	V13	V15
19	V3	V11	V12	58	V5	V13	V15
23	V3	V4	V12	60	V5	V7	V15
24	V3	V4	V8	64	V5	V7	V8

Employing this technique, the ZSV is always selected as the vector V1 (*Vd*0 = V1) and applied first. Then, the three NZSVs are distributed symmetrically along the middle of the switching period in the order specified in Table 5.3 as represented in Figure 5.4 for RP = 1. In this figure, the duty cycles (d_0, d_1, d_2, and d_3) are also marked.

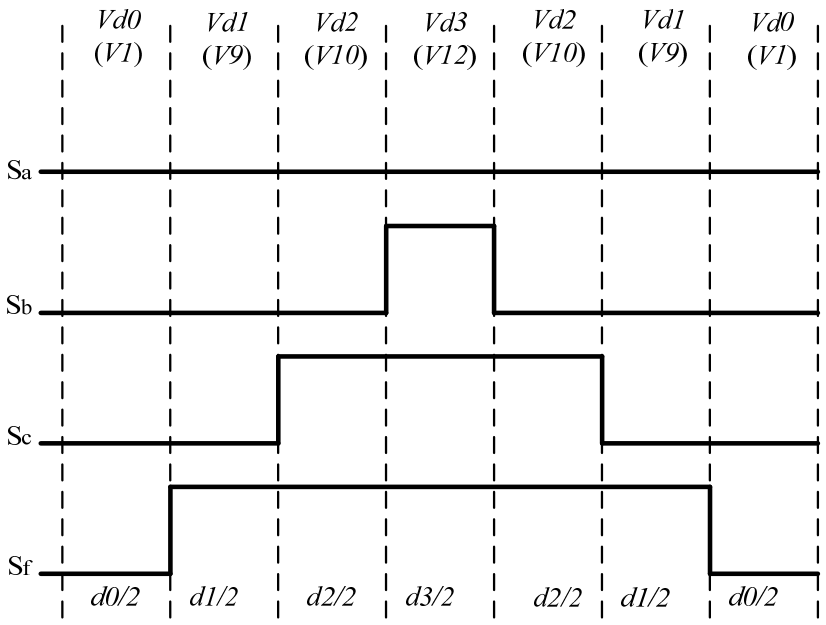

Figure 5.4 Switching signals to produce a vector in region RP = 1

Now the calculation of the duty cycles, d_i, can be easily achieved using the large signal model of the inverter expressed as:

$$\vec{d} = M_d^{-1} \times \vec{v}_{ref} \tag{44}$$

where $\vec{d} = \begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix}$, $M_d = \begin{bmatrix} Vd1_a & Vd2_b & Vd3_c \\ Vd1_a & Vd2_b & Vd3_c \\ Vd1_a & Vd2_c & Vd3_c \end{bmatrix}$ and $\vec{v}_{ref} = \begin{bmatrix} v_{a\_ref} \\ v_{b\_ref} \\ v_{c\_ref} \end{bmatrix}$

It is important to note that the matrix, M_d, in abc coordinates, presents a very simple expression, as all the elements are 0, 1, or -1. So the inversion process is straightforward and all the elements are 0, 1, or -1. Hence the duty cycle calculations imply only addition or subtraction of the reference voltage components as shown in Table 5.4.

The complete calculation of the duty cycle for RP = 1 is shown below. Using Figure 5.4 and Table 5.4, the duty cycle for each phase leg of the inverter will be calculated as follows:

$$d_a = 0 \tag{45}$$

$$d_b = d_3 = -v_{a\_ref} + v_{b\_ref} = -v_{ab} \tag{46}$$

$$d_c = d_2 + d_3 = \left(-v_{b\_ref} + v_{c\_ref}\right) + \left(-v_{a_{ref}} + v_{b_{ref}}\right) = -v_{ac} \tag{47}$$

$$d_f = d_1 + d_2 + d_3 = \left(-v_{a\_ref}\right) + \left(-v_{b\_ref} + v_{c\_ref}\right) + \left(-v_{a\_ref} + v_{b\_ref}\right) = -v_a \tag{48}$$

Similarly, the duty cycles for other sets of RP can be determined by the same procedure.

Table 5.4 Summary of equations for duty cycle calculation [100]

RP	***Vd*1**	***Vd*2**	***Vd*3**	***d*1**	***d*2**	***d*3**
1	V9	V10	V12	$-v_{c\_ref}$	$-v_{b\_ref} + v_{c\_ref}$	$-v_{a\_ref} + v_{b\_ref}$
5	V2	V10	V12	v_{c_ref}	$-v_{b\_ref}$	$-v_{a\_ref} + v_{b\_ref}$
7	V2	V4	V12	$-v_{b\_ref} + v_{c\_ref}$	v_{b_ref}	$-v_{a\_ref}$
8	V2	V4	V8	$-v_{b\_ref} + v_{c\_ref}$	$-v_{a\_ref} + v_{b\_ref}$	v_{a_ref}
9	V9	V10	V14	$-v_{c\_ref}$	$-v_{a\_ref} + v_{b\_ref}$	$v_{a\_ref} - v_{b\_ref}$
13	V2	V10	V14	v_{c_ref}	$-v_{a\_ref}$	$v_{a\_ref} - v_{b\_ref}$
14	V2	V6	V14	$-v_{a\_ref} + v_{c\_ref}$	v_{a_ref}	$-v_{b\_ref}$
16	V2	V6	V8	$-v_{a\_ref} + v_{c\_ref}$	$v_{a\_ref} - v_{b\_ref}$	v_{b_ref}
17	V9	V11	V12	$-v_{b\_ref}$	$v_{b\_ref} - v_{c\_ref}$	$-v_{a\_ref} + v_{c\_ref}$
19	V3	V11	V12	v_{b_ref}	$-v_{c\_ref}$	$-v_{a\_ref} + v_{c\_ref}$
23	V3	V4	V12	$v_{b\_ref} - v_{c\_ref}$	v_{c_ref}	$-v_{a\_ref}$
24	V3	V4	V8	$v_{b\_ref} - v_{c\_ref}$	$-v_{a\_ref} + v_{c\_ref}$	v_{a_ref}
41	V9	V13	V14	$-v_{a\_ref}$	$v_{a\_ref} - v_{c\_ref}$	$-v_{b\_ref} + v_{c\_ref}$
42	V5	V13	V14	v_{a_ref}	$-v_{c\_ref}$	$-v_{b\_ref} + v_{c\_ref}$
46	V5	V6	V14	$v_{a\_ref} - v_{c\_ref}$	v_{c_ref}	$-v_{b\_ref}$
48	V5	V6	V8	$v_{a\_ref} - v_{c\_ref}$	$-v_{b\_ref} + v_{c\_ref}$	v_{b_ref}
49	V9	V11	V15	$-v_{b\_ref}$	$-v_{a\_ref} + v_{b\_ref}$	$v_{a\_ref} - v_{c\_ref}$
51	V3	V11	V15	v_{b_ref}	$-v_{a\_ref}$	$v_{a\_ref} - v_{c\_ref}$
52	V3	V7	V15	$-v_{a\_ref} + v_{b\_ref}$	v_{a_ref}	$-v_{c\_ref}$
56	V3	V7	V8	$-v_{a\_ref} + v_{b\_ref}$	$v_{a\_ref} - v_{c\_ref}$	v_{c_ref}
57	V9	V13	V15	$-v_{a\_ref}$	$v_{a\_ref} - v_{b\_ref}$	$v_{b\_ref} - v_{c\_ref}$
58	V5	V13	V15	v_{a_ref}	$-v_{b\_ref}$	$v_{b\_ref} - v_{c\_ref}$
60	V5	V7	V15	$v_{a\_ref} - v_{b\_ref}$	v_{b_ref}	$-v_{c\_ref}$
64	V5	V7	V8	$v_{a\_ref} - v_{b\_ref}$	$v_{b\_ref} - v_{c\_ref}$	v_{c_ref}

5.4. Experimental system architecture

In order to demonstrate the performance of two four-leg converters of UPFC based compensator for their application in providing voltage and current compensation in LV distribution networks, an experimental development board is built in the laboratory. The main part of the development board is two four-leg inverters. These are fabricated using three phase IGBT converter modules that are often used in appliances such as air-conditioners. In this implementation, the modules are STGIPL14K60 which are a module with six IGBTs (600V, 15A) and bootstrap gate drivers. These modules provide a total of nine phase legs which can be arranged to produce two four-leg converters. The converters share a common DC bus and DC bus capacitor. The board has provision for both polypropylene and electrolytic capacitors. The two four phase IGBT inverter bridges are controlled by a floating point DSP (TMS320F28377D, Delfino Processor @ 200MHz). This device has four independent PWM modules which can operate two phase legs each. This allows the simultaneous operation of eight phase legs in total. Feedback is provided by voltage and current transducers. The current transducers are the LEM CAS series and high impedance differential amplifiers (Op-Amp) are used as current and voltage sensors for the purpose of measuring currents and voltages. The built in analogue to digital converters (ADCs) of the Delfino processor are used to make the feedback quantities available for use. The high level schematic diagram of the experimental system architecture is shown in Figure 5.5. The 3-D-SVM algorithm is separately used in each converter. These modulators generate the duty cycles to produce the required PWM signals for the IGBTs. These PWM signals are being applied to the IGBT inverter's logic circuit to initiate the switching operation to achieve target voltage or current for compensation. Higher level control strategies provide abc voltage demands to control the currents and voltages of the shunt and series converters of the UPFC to achieve voltage regulation,

phase imbalance correction. A filter is placed at the input and output side of the shunt and series converters of the UPFC to remove switching ripple. A capacitor is used as a DC bus by which the power exchange between the shunt and series converters is facilitated. The Delfino processor is applied using a development board provided by Texas Instruments. The board includes the necessary processor programming interfaces and supporting items such as clock generators and power supply decoupling capacitors. This processor needs a 3.3Vdc to operate and this is provided by the external power supply. The pin out diagram of the Delfino processor development board is given in Figure 5.6.

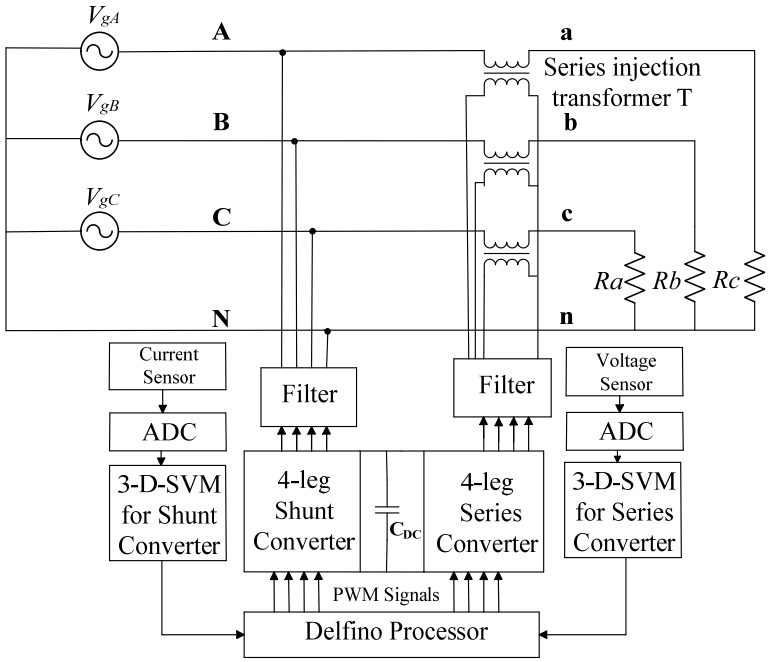

Figure 5.5 Complete experimental system architecture for UPFC based voltage compensator

This shows only the used pins in the experimental boards. This shows mainly the PWM channels and the ADC channels with some general purpose input output (GPIO) pins. PWM signals are produced by the Delfino processor according to the 3-D-SVM algorithm and exit on pins 49 to 64. While digital control may enable complex control designs, it does bring about the element of delay in the control loop. The control is implemented in a

discrete time domain rather than the analogue domain. DSPs used in the control of power converters require a finite time delay for accomplishing the functions of sampling analogue data, calculation, and updating digital and analogue outputs. A delay in the control loop has an obvious destabilising effect on feedback systems. The additional phase delay in the discrete implementations can be accounted for in several ways. The design can be conducted directly in a discrete time domain. The analogue design approaches can be adapted by allowing for the loss of phase margin do to the discrete time delays. The adaptation of the analogue controllers is an adequate approach if the final system bandwidths are modest, less than one tenth, relative to the switching frequencies. This approach has been adopted in this thesis. The details of the schematic diagram are provided in Appendix A.

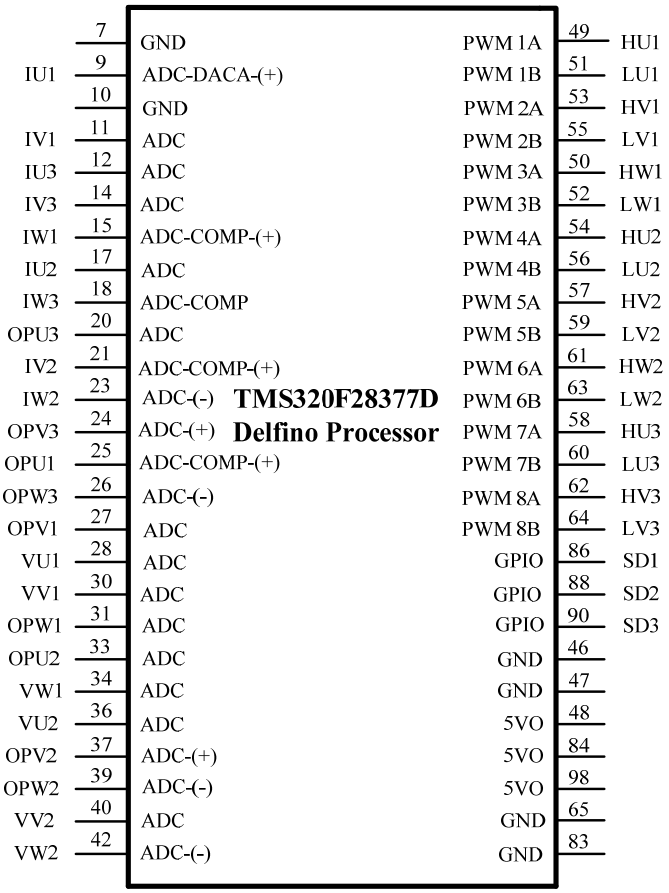

Figure 5.6 Pin out of the of TMS320F28377D Delfino processor control board

5.5. Background resources

The experimental test of the UPFC based compensator requires the hardware and software implementations which are done in the power engineering laboratory at CQUniversity. Some important hardware and software assets are already existed in the laboratory. The hardware was initially designed and constructed by Peter Wolfs and Ben Sneath for an earlier testing requirement. An introductory software installation was produced by Mark Hayman. This software was an open loop implementation of the 3-D-SVM for the Delfino processor. This modulator had been previously used in a four-leg DSTATCOM project using an Infineon processor. The PLL had been also developed on the Infineon processor but this code had not been transferred to the Delfino processor. The required software implementation for the project included:

- The transfer of the PLL software from Infineon processor to the Delfino processor.
- The development of the ADC routines to capture the current and voltage and the calibration of these outputs.
- The development of required control software for the experimental tests mainly series voltage regulation, parallel current control and the DC bus voltage regulation.

These three control experiments establish the key fundamental operations of the converter controls.

5.6. Filter design considerations

Switching converters usually require input and output filters to reduce switching frequency current and voltage components. The addition of an input filter to a converter naturally alters the control-to-output and other transfer functions of the converter. A LC filter introduces additional second-order dynamics and the inductor current and capacitor voltages are additional energy storage elements and have an associate state variable. The

filter may affect the stability of the control loop used in the converters if it is not properly considered in the control design. The minimum filter requires an inductor at the converter terminals. These terminals are voltage stiff and have switched voltages. The resulting inductor current will be continuous but have a degree of current ripple. A capacitor may be added to absorb some of the current ripple and produce continuous voltages. If the filter is not damped there is a possibility of control instability at the corner frequency. Damping can be produced by passive elements such as a capacitor and resistor combination across the main capacitors. The control system may provide active damping via classical methods such as lead compensation or modern methods such as full state variable feedback. Within its control bandwidth, power electronic converters are constant power devices and it thus presents negative incremental impedance to the filters [122]. This negative damping often results in unexpected control instabilities. If these resonant frequencies are lower than the crossover frequency of the controller loop gain, then the phase margin will become negative and the regulator will be unstable. The filter considered in the experimental design consists of a series inductor in parallel with a capacitor and the damping branch consists of a capacitor and a resistor. The filter circuit and filter parameters are shown in Figure 5.7 and Table 5.4 respectively. Apart from the time delay, the filter configuration has a strong influence on the stability of control systems for the converters.

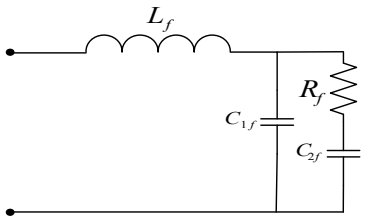

Figure 5.7 Schematic for filter circuit used in the experimental system

The transfer function of an undamped filter without R-C damper, $H_1(s)$, are given by:

$$H_1(s) = \frac{1}{L_f C_{1f} s^2 + 1} \tag{49}$$

$$H_1(s) = \frac{100\times10^6}{s^2+100\times10^6} \tag{50}$$

and the transfer function of the filter with R-C damper, $H_2(s)$, is given by the following equations:

$$H_2(s) = \frac{1+sR_fC_{2f}}{s^3R_fL_fC_{1f}C_{2f}+s^2(L_fC_{1f}+L_fC_{2f})+sR_fC_{2f}+1} \tag{51}$$

$$H_2(s) = \frac{100\times10^6s+7.4\times10^{11}}{s^3++14.81\times10^3s^2+100\times10^6s+7.4\times10^{11}} \tag{52}$$

Table 5.5 Filter parameters used in the experimental system

Parameters	Value
R_f	27Ω
L_f	2mH
C_{1f}	5μF
C_{2f}	5μF

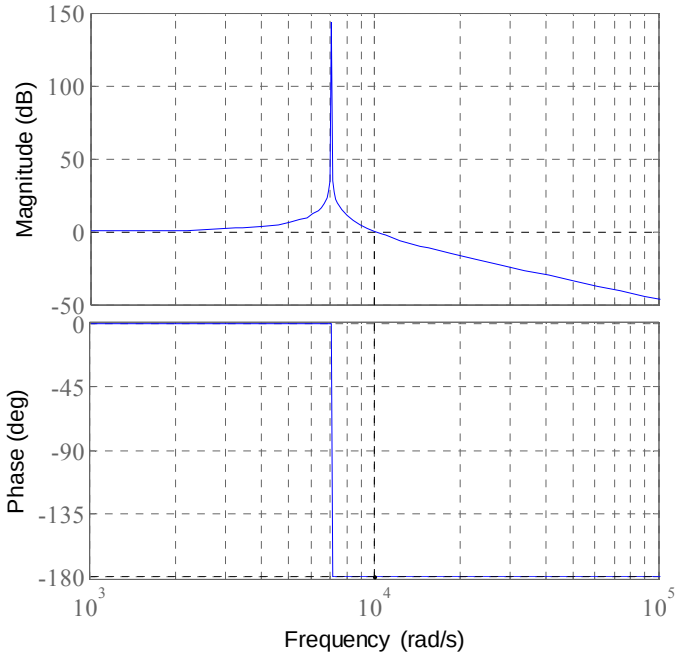

Figure 5.8 Bode plot of the transfer function, $H_1(s)$ of the undamped filter

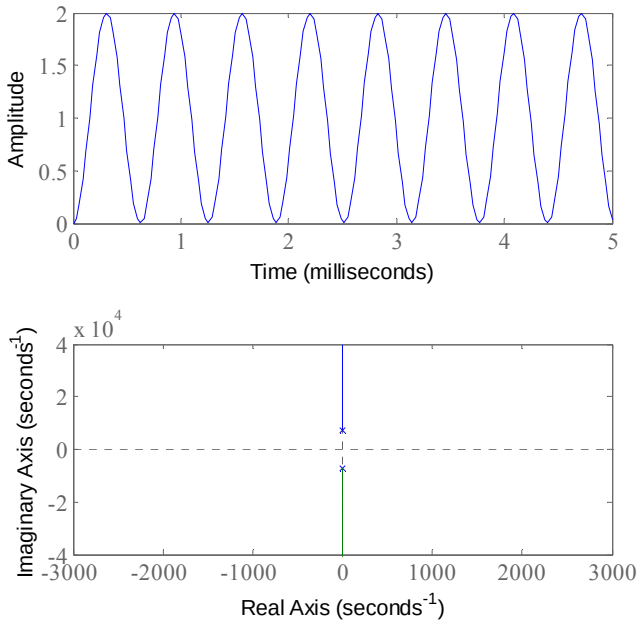

Figure 5.9 Step response and root locus plot of the transfer function, $H_1(s)$ of the undamped filter

The frequency and step responses of the undamped filter with the parameters from Table 5.5 are plotted in Figures 5.8 and 5.9 respectively. The bode diagram is shown in Figure 5.8 where a huge peaking is depicted well below the resonant frequency of the filter and the phase margin is zero.

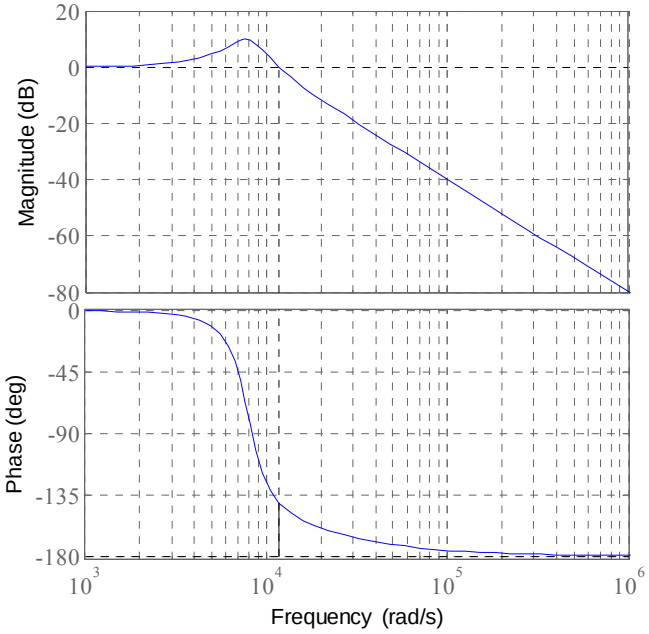

Figure 5.10 Bode plot of the transfer function, $H_2(s)$ of the undamped filter

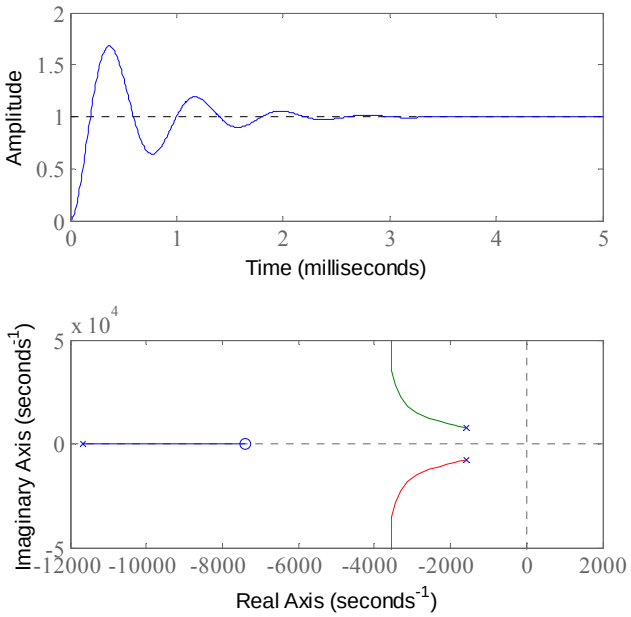

Figure 5.11 Step response and root locus plot of the transfer function, $H_2(s)$ of the undamped filter

The step response of the undamped filter is oscillatory because the conjugate pole pairs of the filter lie on the imaginary axis of the root locus which causes the filter to oscillate as shown in Figure 5.9. The frequency and step responses of the undamped filter with the R-C damper of Figure 5.7 are presented in Figures 5.10 and 5.11 respectively. Figure 5.10 shows how a resistor damper can damp out the huge peaking and shifts the zero crossover frequency while produce a significant positive phase margin which brings the control system stable. The step response and the root locus plot are demonstrated in Figure 5.11. The step response shows that the filter system provides some damping at the beginning and reaches a steady state at about 3.3ms. The effect of adding a resistor for damping is visible in the root locus plot as it helps to bring the complex conjugate pole pairs of an undamped filter into the left half plane (LHP) to ensure the stability of the system.

5.7. Voltage regulation and control of series converter of UPFC based compensator

5.7.1. Experimental diagram for voltage regulation

The schematic diagram used in the experimental system with a balanced three phase Y-connected load for voltage regulation in LV distribution networks is shown Figure 5.12. A

small resistor is connected with phase A at the input terminal to purposefully introduce a small voltage drop to make the input terminal voltage unbalanced. A voltage injection transformer is connected in series with each phase to add the compensation voltages. Each of these transformers is rated at 240V:24V. These transformers have winding resistances that are 2.2% on the transformer base. The primary resistance is 4Ω and secondary resistance is 40mΩ. The shunt converter is not connected to provide the power demanded by the series converter in this experiment. The DC bus voltage of 38V is supplied by an external DC power supply. The series converter is controlled by the Delfino processor. The 3-D-SVM used in this experiment is coded on the Delfino processor to produce the modulated PWM for the IGBT's logic circuits at a 20kHz switching frequency. The Delfino is a floating point processor so all variables, currents or voltages, are scaled to have a one to one relationship to the underlying physical variables. This allows easy comparisons to the simulation results and avoids the application of scaling factors to control gains.

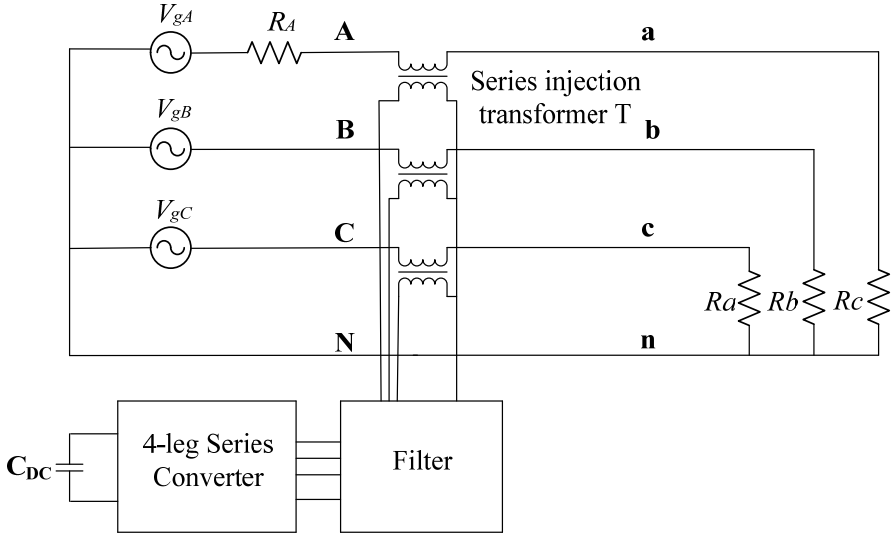

Figure 5.12 Experimental diagram of series converter of UPFC based compensator for voltage regulation

The output of the four-leg series converter of the UPFC is connected with the primary of the series injection transformer through the filter. The four-leg series converter is controlled to have the appropriate magnitude and phase of the injection voltage to regulate the load voltages. The component values used in this experimental system are listed in Table 5.6.

Table 5.6 List of resistors used in the experimental system

Resistors	Value
R_A	2.35Ω
R_a	30Ω
R_b	30Ω
R_c	30Ω

5.7.2. Closed loop control system for voltage regulation

The schematic of the closed loop control designed to control the series converter of the UPFC for regulating the load voltages is presented in Figure 5.13. In this case, the reference sinusoidal voltages, V_{ref}, is generated from the PLL as follows:

$$R_a S = sin(\omega t) \tag{53}$$

$$R_b S = sin(\omega t - 2\pi/3) \tag{54}$$

$$R_c S = sin(\omega t + 2\pi/3) \tag{55}$$

The load voltage, V_{load}, is measured and scaled to real voltage values by the ADC software functions. The control system is voltage controlled and designed to follow the reference voltages of magnitude $28V_{rms}$. From the stability point of view of the control system, a sequence based, rotating reference frame, voltage control is applied as this avoids an experimental stability issues. Wideband controls scheme proved to be sensitive to instabilities caused by the input filters. One drawback of the sequence based controller with two synchronously rotating reference frames is the narrow band nature of control. These will only compensate 50Hz quantities and will not respond to harmonics. A direct control over abc coordinates provides wide bandwidth controls but requires active damping

of the input filter dynamics and further control developments. The functional diagram of the sequence based voltage controller utilising positive and negative sequence synchronously rotating reference frame controllers is presented in Figure 3.4.

Table 5.7 Tuning parameters of voltage injection control loop

Parameters	Values
K_p	50
K_i	0.03
Integral limit	-20 to 20

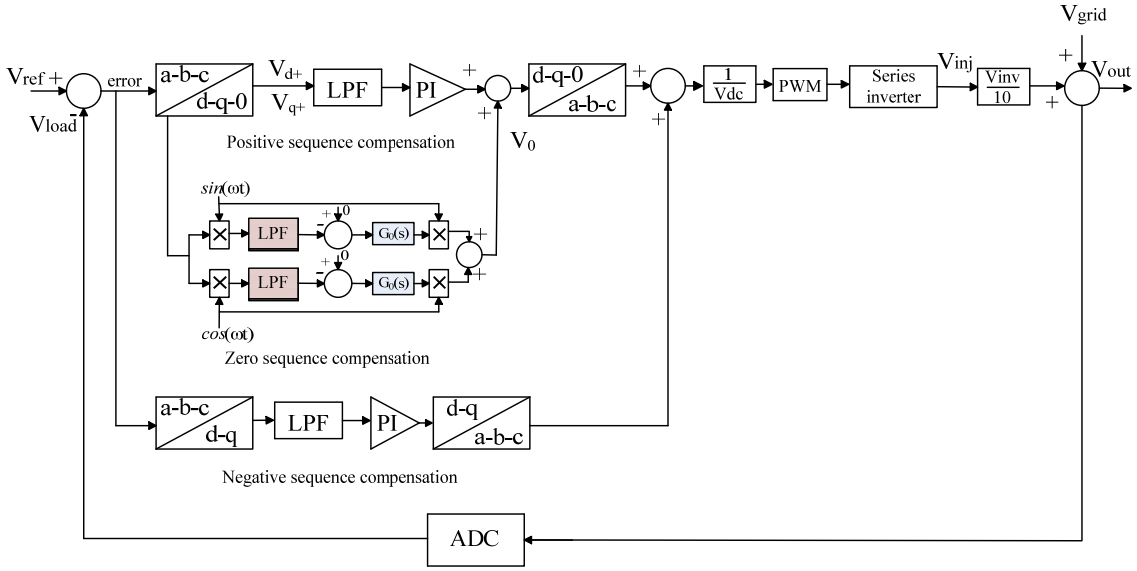

Figure 5.13 Closed loop control system used for voltage regulation in the experiment

The zero sequence controller is also included in the positive sequence reference frame controller as shown in Figure 3.4. The tuning parameter for the designed voltage regulator control loop is shown in Table 5.7. In this control system, the error is calculated by the reference voltages, V_{ref}, and the load voltages, V_{load}. The error voltages in abc coordinates are transformed into the dqo synchronous rotating positive and negative sequence reference frame to produce the DC values of the error. The dq signals are low pass filtered to have pure DC values at the output of the filter. The PI controllers are used to force the error voltages in positive and negative sequence reference frames to zero. An additional

control loop is required to control the zero sequence voltage. The zero sequence voltage is a sinusoid and this is converted into two DC quantities by multiplication with a sine and cosine reference signals. PI controllers are then used to force the zero sequence components to zero. Then the output of the PI controllers is transformed into the abc reference frame from the dqo reference frame. The saturation limit for the integrator of PI controllers is set to the DC bus voltage. The three phase voltages in the abc reference frame are normalised by the DC bus voltage to limit the duty cycles between -1 to 1. These normalised voltages are fed through the 3-D-SVM in the series converter to produce the duty cycles of required target voltages for voltage regulation. The PWM signals produced by the duty cycles are applied to the logic circuit of the IGBTs to produce the voltages at the transformer primary and the actual correction voltage injected into the line will be 10 times lower than the primary voltage. The correction voltage is added to the grid voltages to produce the load voltages.

5.7.3. Experimental results for voltage regulation

In this section, the experimental results for the voltage regulation system are described. The measurement data is outlined in Table 5.6 which shows the r.ms. magnitudes of the incoming grid voltages, input terminal voltages to input neutral N and output load voltages to output neutral terminal n. The incoming grid voltages available in the laboratory are well balanced. The voltages are purposefully unbalanced at the input A,B,C,N terminals of the experimental system by the inclusion of a small resistor that produces a voltage drop of about $2.13V_{rms}$ in phase A. The effectiveness of the control loop used in the voltage regulation system is evident from the output load voltages. The control system effectively produces the required correction voltages for all three phases to regulate the output voltages while simultaneously correcting the phase voltages unbalancing as seen from the output voltages of Table 5.8.

Table 5.8 Measurement data from experimentally designed voltage regulation system

Incoming grid voltages	Input Terminal voltages	Output load voltages
$V_{gA} = 28.35V_{rms}$	$V_{AN} = 26.22V_{rms}$	$V_{an} = 27.99V_{rms}$
$V_{gB} = 28.39V_{rms}$	$V_{BN} = 28.55V_{rms}$	$V_{bn} = 28.03V_{rms}$
$V_{gC} = 28.34V_{rms}$	$V_{CN} = 28.10V_{rms}$	$V_{cn} = 28.00V_{rms}$

The voltage regulatory performance of the series converter of the UPFC is demonstrated through the following observations from Figures 5.14 to 5.17. The experimental data is recorded from the oscilloscope and plotted in Matlab over two cycles. The input and output voltages of the voltage regulation system are shown in Figures 5.14 and 5.15. The input voltage is unbalanced as the phase A (red) voltage is slightly lower than that of the other two voltages, while the output voltages are well balanced as seen from Figure 5.15.

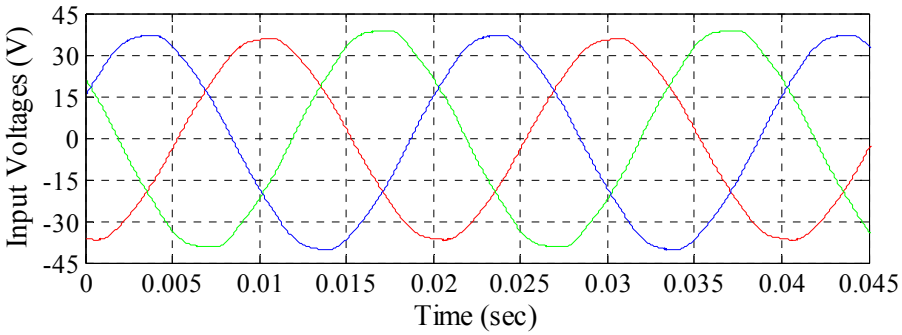

Figure 5.14 Input voltages at A,B,C,N terminals of the voltage regulation system

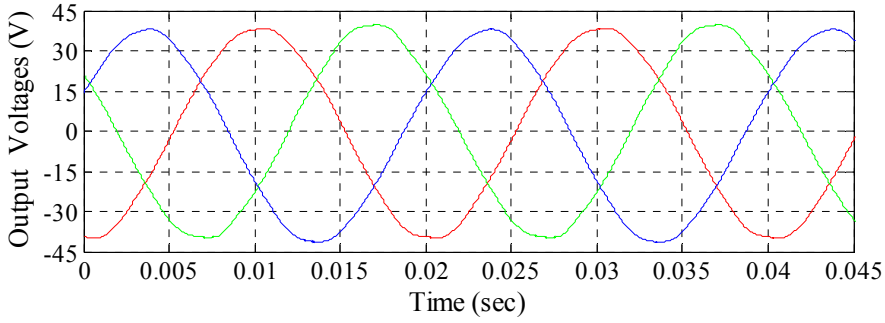

Figure 5.15 Output regulated load voltage at a,b,c,n terminal of the voltage regulation system

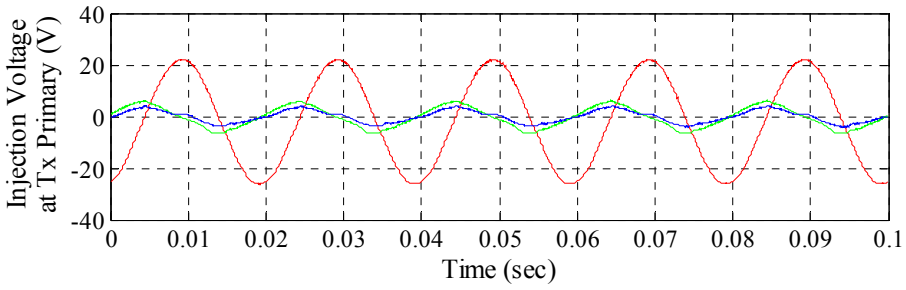

Figure 5.16 Series converter output voltages at the transformer primary

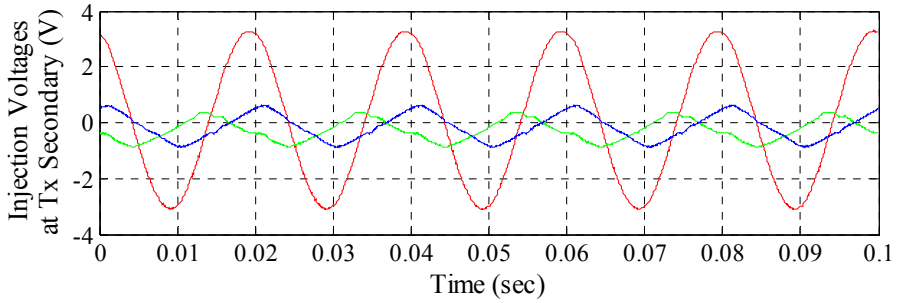

Figure 5.17 Series converter output voltages at the transformer secondary

The correction voltages produced by the series converter to regulate the load voltages are shown in Figures 5.16 and 5.17. The series converter output voltages are injected into the line by a series injection transformer and thus the output of the series injection transformer appears at the transformer primary as shown in Figure 5.16. Since a small resistor causes a voltage drop of $2.13V_{rms}$ in phase A, the injected voltage at phase A is higher than any other phases and the level of the injected voltage at phase A is very close to $2.13V_{rms}$ as can obviously be seen from Figure 5.17.

5.8. Current regulation and control of shunt converter of UPFC based compensator

5.8.1. Experimental diagram for current regulation

The schematic of the experimental set-up to control the shunt converter for current regulation is shown in Figure 5.18. When the converter is operated for current regulation, the four-leg series converter and the load are switched off as the DC bus voltage is supplied by an external DC voltage source. The grid voltages are controlled with a variable

AC voltage supply to test and control the four-leg shunt converter at low voltage levels. The small resistor in series with phase A is retained in this experiment. A filter is connected at the input of the four-leg shunt converter to remove switching ripple from the grid as shown in Figure 5.7. A 38Vdc source is connected to the DC bus.

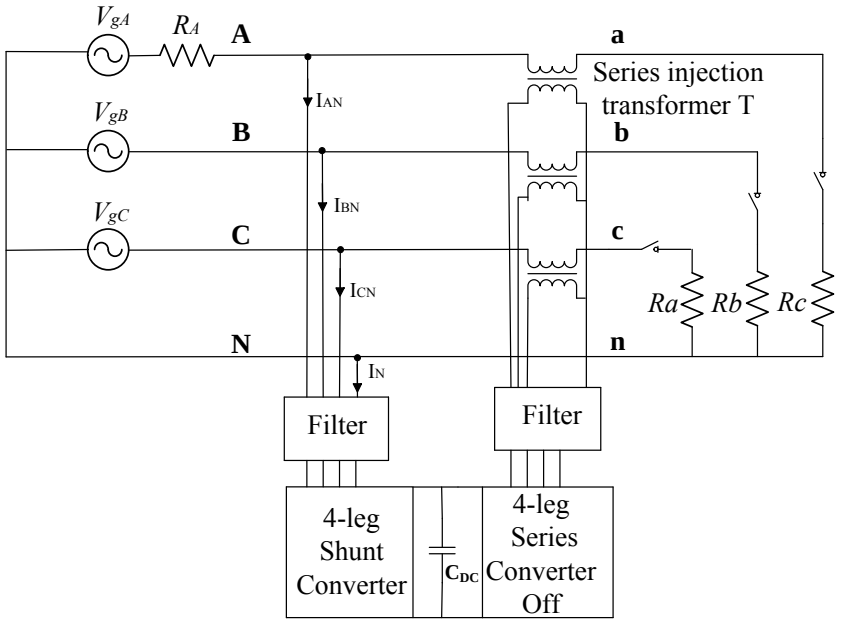

Figure 5.18 Experimental diagram of shunt converter of UPFC based compensator for current regulation

5.8.2. Closed loop control system for current regulation

The schematic of the closed loop control system for current regulation by the shunt converter is shown in Figure 5.19. The reference set of sine and cosine currents are generated by the PLL. Equations 53-55 show the sine references, and the cosine references are generated as follows:

$$R_a\, C = cos(\omega t) \tag{56}$$

$$R_b\, C = cos(\omega t - 2\pi/3) \tag{57}$$

$$R_c\, C = cos(\omega t + 2\pi/3) \tag{58}$$

The three phase reference current demands are calculated as follows:

$$I_{a\_demand} = I_{real} \times R_a S + I_{reactive} \times R_a C \tag{59}$$

$$I_{b\_demand} = I_{real} \times R_b S + I_{reactive} \times R_b C \tag{60}$$

$$I_{c\_demand} = I_{real} \times R_c S + I_{reactive} \times R_c C \tag{61}$$

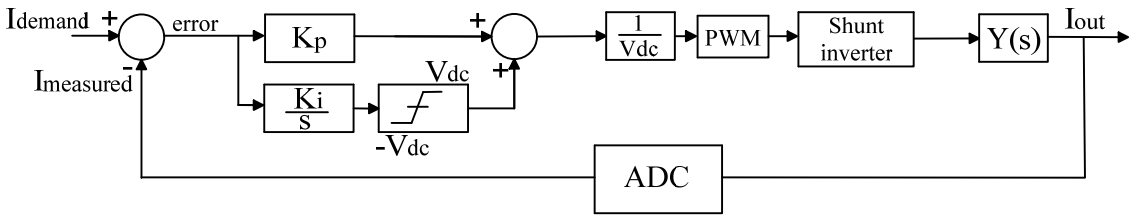

Figure 5.19 Closed loop control system used for current regulation in the experiment

The shunt converter is current controlled by a closed loop current regulator. The shunt inverter currents are measured by the ADC and used to calculate the current errors. PI controllers drive the error to get the target voltages for the shunt converter to regulate the currents. The voltage generated by the PI controllers is normalised by the DC bus voltage and fed though the 3-D-SVM used by the shunt converter to generate PWM pulses to trigger the shunt converter's IGBTS. The shunt converter input voltage is divided by the impedance of the input filter to produce the output shunt inverter currents. The impedance of the input filter is calculated from Figure 5.7 as follows:

$$Z(s) = sL_f + Z_f(s) \tag{61}$$

The effect of $Z_f(s)$ is ignored when designing the control loop for simplification. The load admittance Y(s) is dominated by the filter inductance and this gives a first order response. The bandwidth is set to 2kHz, one tenth of the switching frequency. The tunning parameters for designed current control loop of shunt converter are shown in Table 5.9.

Table 5.9 Tuning parameters for current control loop for shunt converter

Parameters	Values
K_p	15
K_i	4
Integral limit	-40 to 40

5.8.3. Experimental results for current regulation

The shunt converter experimental performance for current regulation is presented in Table 5.10. Four different operating modes are considered to test the performance of the shunt converter in terms of its control design. In all operating modes, the reference currents are set to 1Amp (peak) and the shunt converter is controlled to allow currents of 1Amp (peak) in each phase to follow the reference currents. The effectiveness of the shunt converter controller is seen from the shunt converter currents which are measured in terms of the r.m.s value, and the peak magnitude of those currents will be 1Amp. In forced capacitive and inductive modes, the real currents are set to zero while the reactive currents are set to 1Amp (peak) for the force capacitive case and -1Amp (peak) for the inductive case to produce the reference currents.

The reactive currents are set to zero when the shunt converter is controlled for real power export to the grid or import from the grid. When the real power is exported to the grid, the real currents flows from the converter to the grid and the phase voltages increase. This is evident from V_{AN} , which is higher compared to the other two phases due to the presence of the small resistor. During the import of real power from the grid, the direction of current flow is from the grid to the shunt converter. The voltages at phase A reduces due to that resistor. The experimental data of the shunt converter current regulation performance is recorded from the oscilloscope and plotted in Matlab over five cycles which are shown in Figures 5.20 to 5.29. The reactive currents and voltages, when the shunt converter is controlled for the force capacitive case, are shown in Figures 5.20 and 5.21.

Table 5.10 Measurement data from experimentally designed current regulation system

Operating mode	Shunt converter input voltages	Shunt converter currents
Forced capacitive	$V_{AN} = 8.95V_{rms}$ $V_{BN} = 8.84V_{rms}$ $V_{CN} = 8.77V_{rms}$	$I_{AN} = 0.7I_{rms}$ $I_{BN} = 0.7I_{rms}$ $I_{CN} = 0.7I_{rms}$
Forced inductive	$V_{AN} = 9.17V_{rms}$ $V_{BN} = 8.91V_{rms}$ $V_{CN} = 8.77V_{rms}$	$I_{AN} = 0.7I_{rms}$ $I_{BN} = 0.7I_{rms}$ $I_{CN} = 0.7I_{rms}$
Real power export to grid	$V_{AN} = 11.94V_{rms}$ $V_{BN} = 10.33V_{rms}$ $V_{CN} = 9.90V_{rms}$	$I_{AN} = 0.7I_{rms}$ $I_{BN} = 0.7I_{rms}$ $I_{CN} = 0.7I_{rms}$
Real power import from grid	$V_{AN} = 6.68V_{rms}$ $V_{BN} = 8.52V_{rms}$ $V_{CN} = 8.68V_{rms}$	$I_{AN} = 0.7I_{rms}$ $I_{BN} = 0.7I_{rms}$ $I_{CN} = 0.7I_{rms}$

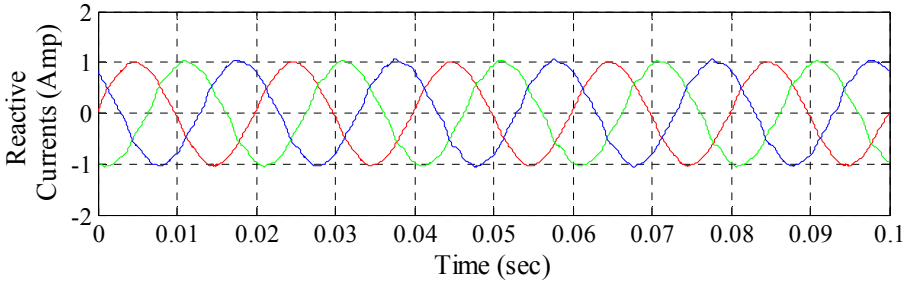

Figure 5.20 Reactive currents when the grid is forced to draw capacitive currents

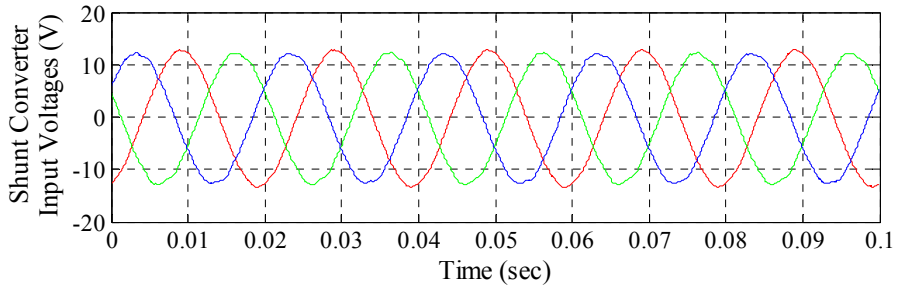

Figure 5.21 Shunt converter input voltages while the grid is forced to draw capacitive currents

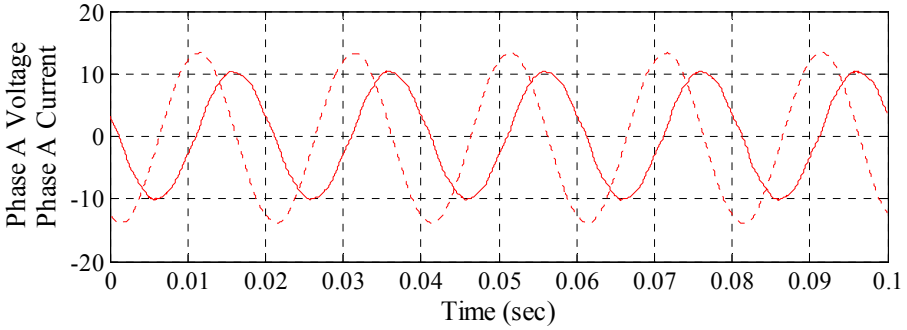

Figure 5.22 Shunt converter phase A currents (red) and phase A voltage (dashed red) in force capacitive mode. The scale is 10V/div for voltage and 1A/div for current

The reactive currents to the shunt converter are seen to be balanced with 1Amp (peak), and the shunt converter voltages are nearly balanced as the reactive current in phase A produces a voltage drop across the resistor. In forced capacitive mode, the voltage and current of phase A is shown in Figure 5.22 to show the phase angle difference between the voltage and current waveforms. The voltage (dashed red) and current (red trace) are almost 90° out of phase and the current leads the input phase voltage which confirms the operation of the shunt converter in forced capacitive mode and the effectiveness of control system as well. The control loop has a finite loop grain at 50Hz. The grid voltage acts as a disturbance which causes a 50Hz current flow that is suppressed by the loop gain. This residual current is superimposed upon the desired currents giving some angle variation. The disturbance current can be compensated by feed forward of the grid voltage. The reactive currents and shunt converter input voltages, when the shunt converter is controlled for forced inductive operation, are presented in Figures 5.23 and 5.24.

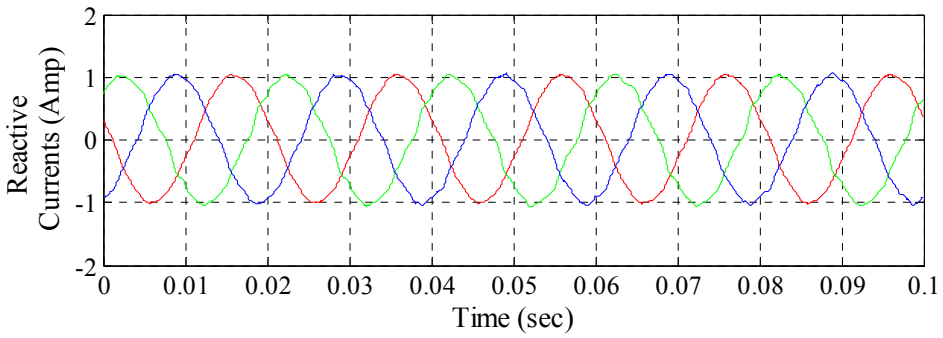

Figure 5.23 Reactive currents when the grid is forced to draw inductive currents

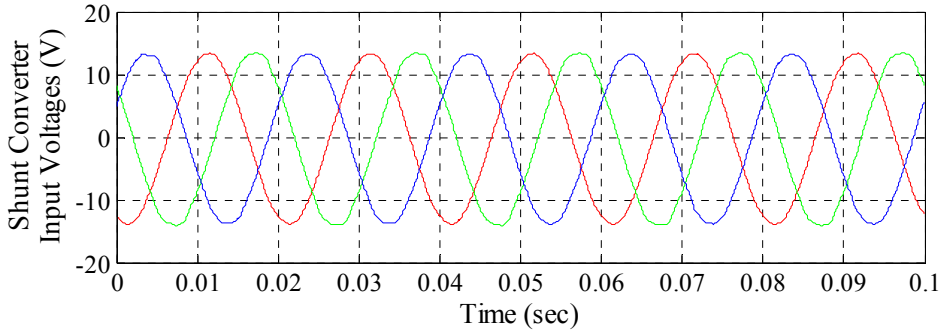

Figure 5.24 Shunt converter input voltages while the grid is forced to draw inductive currents

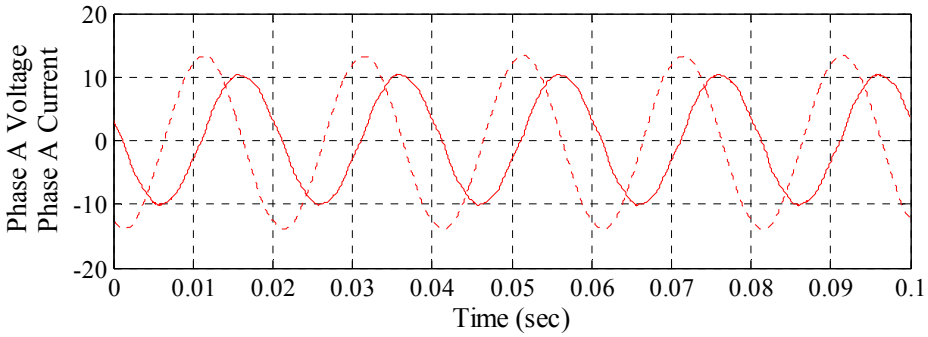

Figure 5.25 Shunt converter phase A currents (red) and phase A voltage (dashed red) in force inductive mode. The scale is 10V/div for voltage and 1A/div for current

In this case, the shunt converter reactive currents are also balanced with the 1Amp (peak). The phase angle difference is seen from Figure 5.25, where the voltage waveform (dashed red) leads the current waveform (red) by an angle of almost 90°.

The experimental waveforms of real currents exported by the shunt converter and shunt converter input voltages are shown in Figures 5.26 and 5.27. In this case, the shunt converter is controlled to provide the 1Amp (peak) real currents to grid and zero reactive currents. The shunt converter current supplied to the grid found experimentally are shown in Figure 5.26 which is exactly 1Amp (peak). However, the shunt converter input voltage is not balanced and phase A is higher than other two phases, because of the voltage drop at the small resistor in phase A is added to the grid voltage and pushes it up as shown in Figure 5.27. It is noteworthy that the phase difference of current and voltage are in same phase during the real power export to the grid. In this case, shunt converter power is positive which means the shunt converter is delivering power to the grid. The control action of the shunt converter is demonstrated during the power importing from the grid in Figures 5.28 and 5.29. 1Amp (peak) real current is now drawn by the shunt converter from the grid. The voltage drop at the phase A resistor lowers the shunt converter input voltages at phase A. However, the phase difference between the voltage and current is 180° in the

real power importing mode. This shunt converter power is now negative which means that the shunt converter is taking power from the grid as seen in Figures 5.28 and 5.29.

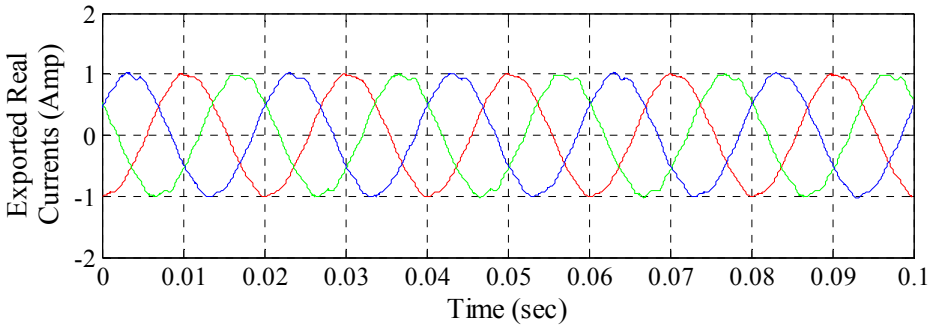

Figure 5.26 Exported real currents to the grid by shunt converter

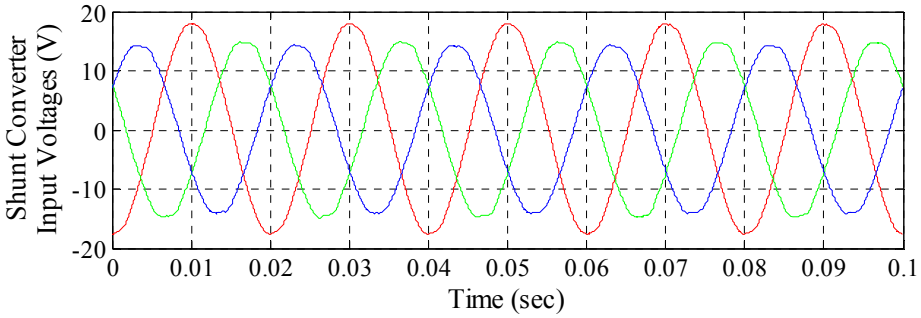

Figure 5.27 Shunt converter input voltages while exporting real currents to the grid

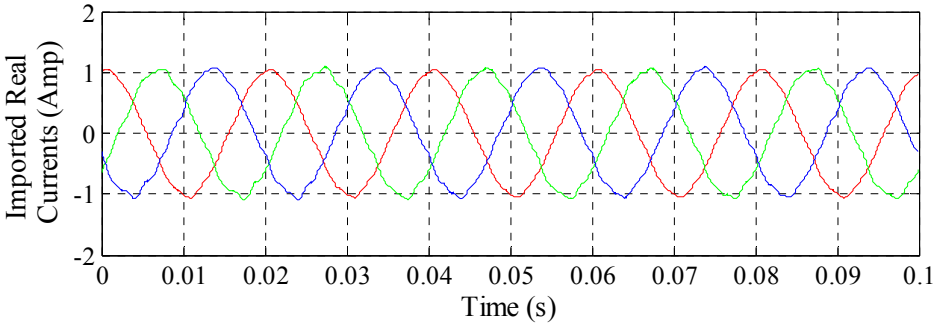

Figure 5.28 Imported real currents from the grid by the shunt converter

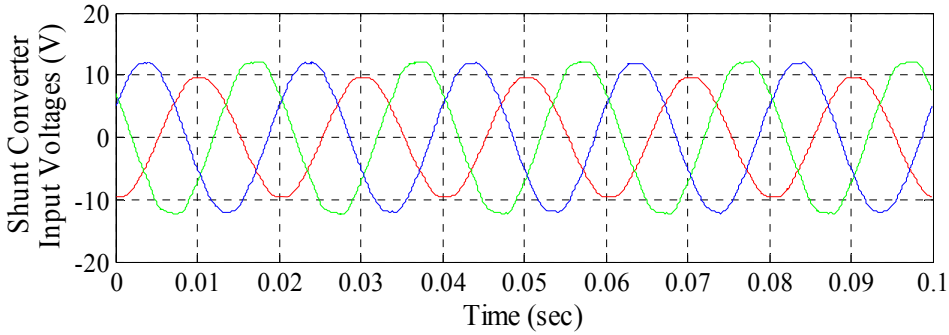

Figure 5.29 Shunt converter input voltages while importing real currents from the grid

5.9. DC bus voltage regulation system

5.9.1. Experimental diagram of the DC bus voltage regulation system

The schematic of the experimental set-up to control the four-leg shunt converter for DC bus voltage regulation of UPFC based compensator is shown in Figure 5.30. The experimental set-up is almost identical to the set-up used for shunt converter for current regulation. The one difference is that, in this case, the external DC power supply is removed and the DC bus capacitor, which is a combination of three polypropylene and two electrolytic capacitors, is used to provide the DC bus voltage. From the control point of view, the DC bus needs to be equipped with independent control to regulate the DC bus voltage, which will be discussed in the subsequent section. When the converter is operated for DC bus voltage regulation, the four-leg series converter and the load are switched off. The grid voltages are controlled with a variable AC voltage supply to test and control the DC bus voltage at low voltage levels. The small resistor in series with phase A is also retained in this experiment. A filter is connected at the input of the four-leg shunt converter to remove switching ripple from the grid as shown in Figure 5.7.

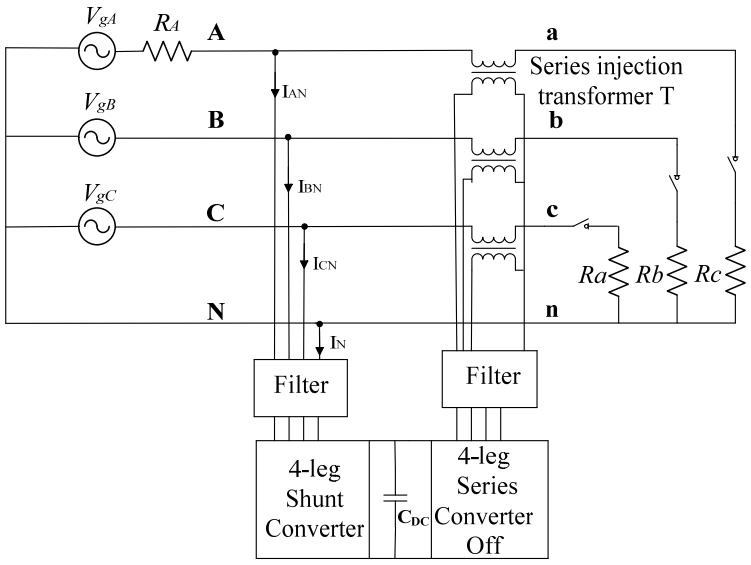

Figure 5.30 Experimental diagram of UPFC based compensator for DC bus voltage regulation

5.9.2. Closed loop control system for DC bus voltage regulation

The schematic of the closed loop DC bus voltage control system for DC bus voltage regulation is shown in Figure 5.31. The DC bus voltage control system is voltage controlled to produce the current demand of the shunt converter for DC bus voltage regulation. It consists of two control loops to achieve normal and high speed control of the DC bus voltage.

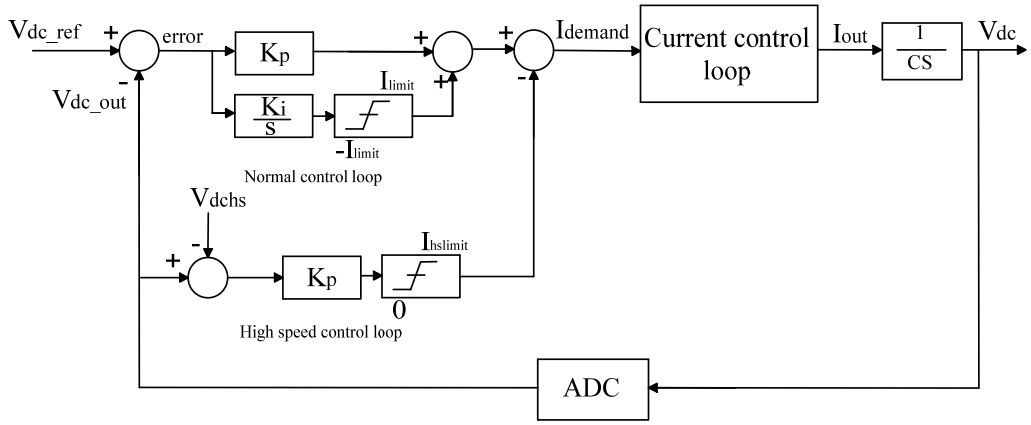

Figure 5.31 Closed loop control system for DC bus voltage regulation

A closed loop current regulator is used in the DC bus voltage regulation system for current control of shunt converter to produce target currents for the DC bus capacitor. The output current of the current regulator flows through the DC bus capacitor and develops the target DC bus voltage. The function of closed loop current control system is described in section 5.7.2. The normal DC bus voltage control loop compares target voltage, V_{dc_out}, with the reference set point DC voltage, V_{dc_ref}. A PI controller is used which responds to errors in the average DC bus voltage and forces the error to zero. The normal voltage control loop provides the current demand of the shunt converter to regulate the DC bus voltage. During transients, the DC bus voltage can be successfully limited by the high speed control of the shunt converter real power through its current demand. Once the DC bus capacitor voltage reaches the high speed set point voltage of Vdc, the high speed voltage control loop

becomes active to instantaneously reduce the current demand by the parallel converter limiting the voltage rise.

5.9.3. Experimental results for DC Bus voltage regulator

The measurement data from the experimental set-up of the DC bus voltage regulation system is shown in Table 5.11. In this case the DC power supply connected to the DC bus in previous experiments was removed. A 30Ω load was connected across the DC bus so that a moderate level of phase currents would be required to maintain the bus voltage. The DC bus voltage control system is controlled to regulate at 40Vdc and the regulated voltage at the DC bus is found 39.6Vdc. A small difference is seen and this may be due to the calibration error of the transducers since the experiment is conducted at lower voltage levels. The calibration of the transducers is expected to be accurate once the experiment will be conducted at the higher voltage levels.

Table 5.11 Measurement data from experimentally designed DC bus voltage regulation system

DC bus voltage	Shunt converter input voltages	Shunt converter currents
39.6Vdc	V_{AN} = 11.95V_{rms} V_{BN} = 14.96V_{rms} V_{CN} = 14.79V_{rms}	I_{AN} = 1.45I_{rms} I_{BN} = 1.45I_{rms} I_{CN} = 1.45I_{rms}

The shunt converter input voltage at phase A is lower than other two phases. This is due to the small resistor which develops a small voltage drop because the shunt converter imports the real current of 1.45A_{rms} from the grid as seen from the Table. 5.11. This resistor was included so that an unbalanced voltage would be present at the converter input and this would generate some 100Hz ripple on the DC bus. The DC bus voltage regulatory performance of the DC bus control system is demonstrated through the following Figures 5.32 to 5.34. The experimental data is recorded from the oscilloscope and plotted in Matlab over five cycles. The shunt converter input voltages and currents are shown in Figures 5.32

and 5.33. The input shunt converter voltages are seen from the Figure 5.32. The phase voltages in phase B and phase C are equal but drops at phase A which is due to the small resistor retained at phase A. The currents drawn by the shunt converter from the grid are shown in Figure 5.33.

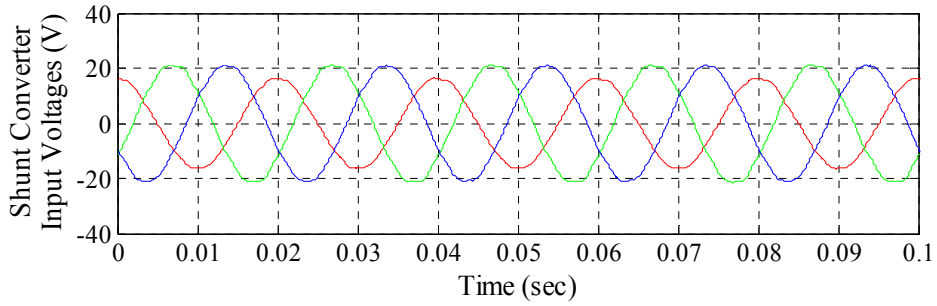

Figure 5.32 Shunt converter input voltages during DC bus regulation from DC bus capacitor

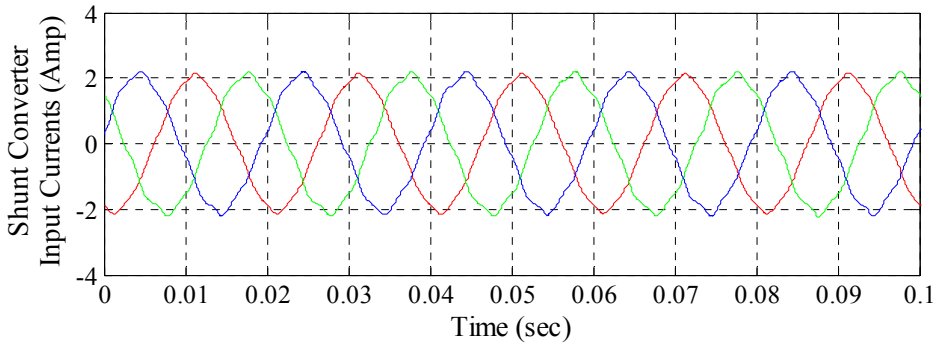

Figure 5.33 Shunt converter input currents during DC bus regulation from DC bus capacitor

The shunt converter currents are balanced and have equal magnitude of 2Amp (peak) in each phase. During the DC bus voltage regulation, the shunt converter is importing power from the grid and the phase angle difference should be ideally 180°. In DC bus control system, the shunt converter demands the real current to regulate the DC bus voltage. The current control loop has a finite loop grain at 50Hz. The grid voltage acts as a disturbance which causes a 50Hz current flow. This residual current is superimposed upon the desired phase currents. In this instance feed forward compensation was used to cancel the disturbance current. In practical terms this was implemented by setting the reactive current setting to 1Amp. Due to these reasons, there may be some angle difference between

voltage and current waveform. As seen from the Figure 5.32 and 5.33, the phase angle difference between voltages and currents are close to 180°.

The DC bus voltage across the DC bus capacitor is shown in Figure 5.34. The DC bus voltage is shown to be regulating at 40Vdc. The DC bus voltage contains a 100Hz ripple voltage of magnitude about 0.5V which represents a 1.25% ripple voltage.

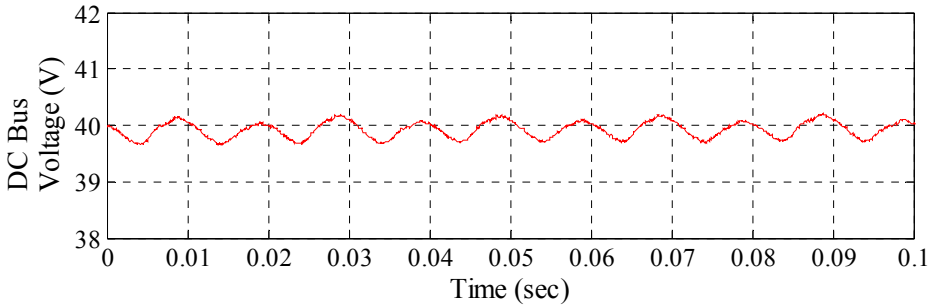

Figure 5.34 DC bus voltage

This 100Hz ripple is found due to the unbalanced operation of the system and needs to be removed from the DC bus voltage. The DC bus control system needs to have fast response characteristics. The LC input filter connected to the shunt converter at the grid side introduces potential unstable dynamics and this may affect the overall dynamics response of the DC bus control system. In this experimental system, damping is provided to the input filter passively by adding damping resistors. Experimentally it was observed that shorting the small resistor in phase A caused the 100Hz ripple to vanish, as the converter then operated with balanced input currents. The passive damping introduces some losses in the damping resistor. This should be avoided using a straightforward active damping solution.

5.10. Conclusion

In this chapter, the capabilities of the series and shunt converter of the proposed UPFC for voltage regulation and phase balancing are experimentally demonstrated in the laboratory. The UPFC based compensator is designed for an input voltage level of 400/230Vac with

the DC bus voltage of 400Vdc. Due to occupational health and safety related issues, the experiment is conducted at a low power level which is approximately reduced by a factor of 10. Hence the operating input voltage range becomes 40/23Vac with 40Vdc at the bus. The PLL is shown to be extremely precise in its locking capability even at the extra LV grid voltages (mV range). The PLL is also robust and because it responds to the fundamental frequency only it has a high rejection of any waveform distortions. It operates successfully with only a single phase available and is immune to the transient loss of a phase. The 3-D-SVM modulation methods is used for the series and shunt converters allow the generation of three independent phase to neutral voltage waveforms that make good use of all DC bus voltage with a minimum calculation overhead. The experimental waveform data are captured two to five cycles and is plotted in Matlab for different operations of the series and shunt converters. The experimental results show that the series converter can effectively regulate and balance the load voltages under unbalanced conditions while the shunt converter is shown capable of providing the reference current demands under different operating modes. The shunt converter control systems are designed to operate in four operational states, i.e. forced capacitive, forced reactive, real power export and real power import. The experimental results demonstrate the effectiveness of the shunt converter current control system. According to the experimental results, the currents and voltage are 90° out of phase in both forced capacitive and inductive mode, while the phase difference is 0° and 180° for power exporting and importing cases respectively. In the forced capacitive mode, the currents lead the voltages, while in the forced inductive mode, voltages lead the currents. The power becomes negative when importing/receiving from the grid and becomes positive when exporting/delivering to the grid. The DC bus voltage regulation system is demonstrated to control the DC bus voltage with its own capacitor at the bus. The experimental results

show the DC bus voltage effectively regulates the capacitor voltage at the bus while importing power from the grid. A ripple voltage of about 0.5V at 100 Hz is seen from the DC bus voltage when the phase voltages were unbalanced to produce 100Hz power fluctuations.

Chapter 6 DISCUSSIONS, CONCLUSIONS AND FUTURE WORK

6.1. Discussions

With increasing retail costs and increasing environmental awareness, PV is becoming a more important resource for customers to meet their electricity demand. The annual installation rates of PV globally are increasing rapidly and a large proportion of this is being installed as residential or commercial rooftop PV.

As the increasing installation of distributed rooftop PV systems introduces overvoltage, reverse power flow and voltage unbalance, it is becoming very challenging to maintain the usual operational behaviour of the distribution networks. The most serious effect is the overvoltage which may be a consequence of reverse power flow in the LV distribution networks. This requires quick corrective measures to keep the customer supply voltage within acceptable limits. The customers may also suffer from phase unbalance where loads and PV are not uniformly allocated across the phases. A variety of methods are proposed in recent publications for mitigation of voltage problems in LV distribution networks. The commercially available mitigation methods such as on-load tap changers and fixed or switched capacitors are not effective in compensating those problems as these require fast control action. Emerging mitigation methods mainly include VAR control of PV inverters, distributed batteries and FACTS controllers. Of these, FACTS controllers are very effective particularly the UPFC based compensator. A review of the other two methods shows VAR control of PV inverters is restricted by current practices specified in the applicable standards and distributed batteries are very expensive.

This thesis proposed a UPFC based compensator for the LV distribution networks which is designed to provide both the voltage and current compensation. Modelling of the proposed UPFC has been undertaken to ensure that it can adequately carry out the full set of compensation duties, and the necessary mathematical equations are derived for each set of

duties. The thesis studied a range of series and parallel compensation duties for four-leg series and shunt converters.

To perform series voltage compensation, two methods are introduced with their control loops. The first is the direct control of output voltage in abc coordinates which requires the positive sequence voltage reference and the output voltage measurement. The other method is the sequence based synchronously rotating frame approach which requires the time varying voltages to be transformed into two dq rotating reference frames. The sequence based synchronous reference frame approach requires an additional zero sequence voltage control loop to compensate any zero sequence voltage that appears during the unbalanced operations. The sequence based control of output voltage is applied in the experimental test as this had better tolerance to filter induced oscillations.

The shunt converter is controlled to have a set of duties involving active filtering/harmonic current compensation, zero sequence current compensation, reactive current compensation and a degree of negative sequence current compensation.

The modelling of the UPFC was carried out in continuous time domain with the assumption that the switching frequency of the converters is sufficiently high relative to the control bandwidths. This is practically true to converters of less than 100kVA where the switching frequency can easily be more than 10 kHz. Instantaneous power theory was applied to control the series and shunt converters of the UPFC, and the general equations for the average and oscillatory power are provided. A set of converter design choices is provided based on the selection of the DC bus capacitor. A design equation for the DC bus capacitor size is provided for 50Hz cases and if the shunt converter is controlled to draw additional harmonic current demand. The voltage and power control approaches are also modelled.

The simulation studies focused on a test case inspired by the Perth Solar city Trials. The proposed 4+4 leg UPFC based voltage regulator was placed at the midpoint of a 300m long "Mars" feeder from the distribution transformer to the customer load. The simulation of the UPFC is conducted in Matlab Simulink. Initially, the four-leg UPFC based compensator is equipped with zero sequence and reactive current controllers. The compensator is shown capable of actively regulating the positive, negative, and zero sequence voltages at the output terminals using the series converter. At the same time, the regulator is capable of providing compensation for reactive, zero sequence and a degree of negative sequence current using the shunt converter. The compensator can effectively meet the reactive power demand required by the load which reduces the current from upstream of the voltage regulator. Thus the power factor upstream of the voltage regulation device becomes unity. The neutral current is eliminated from upstream of the voltage regulator by the action of the zero sequence current controller. Instantaneous reactive power theory has been applied to ensure the 2ω power fluctuations can be compensated by allowing the input shunt converter to draw a negative sequence current. In the steady state, 2ω voltage fluctuations are removed from the DC bus capacitor voltage. Suppression of 2ω voltage fluctuations are activity performed by controlling the shunt converter negative sequence current. Then, the UPFC based compensator is designed and controlled for exploring the active filtering capability. The nonlinear load is added with the solar generation to reflect the presence of harmonics content at the load side. The UPFC based compensator is shown to be capable of actively removing the harmonic component from the supply side source current. The power flow equation developed due to the additional 5^{th} harmonic current flow through the shunt converter shows that 2ω and 6ω voltage oscillations will be present at the DC bus. The 2ω voltage oscillations are actively removed from the DC bus by

controlling the shunt converter negative sequence current, while 6ω fluctuations are internalised with a slightly larger capacitor of 100 μF.

The experimental works required the systematic design and construction of hardware for the UPFC based compensator and the development of the necessary control software for the experimental testing of the UPFC based compensator for voltage regulation, parallel current control and DC bus voltage regulation. The hardware was designed and constructed by Peter Wolfs and Ben Sneath. An introductory software installation was produced by Mark Hayman. This software was an open loop implementation of the 3-D-SVM for the Delfino processor. This modulator had previously been used in a four-leg DSTATCOM project using an Infineon processor. The PLL had also been developed on the Infineon processor, but this code had not been transferred to the Delfino processor. The required software implementation for the project included:

- Transfer of the PLL software from the Infineon processor to the Delfino processor.
- Development of the ADC routines to capture the current and voltage and the calibration of these outputs.
- Development of required control software for the experimental tests, mainly series voltage regulation, parallel current control and the DC bus voltage regulation.

These three control experiments establish the key fundamental operations of the converter controls. The capabilities of the proposed UPFC based compensator for voltage regulation; parallel converter current control and DC bus voltage control were experimentally demonstrated in the laboratory. The UPFC based compensator is designed for an input voltage level of 400/230Vac with the DC bus voltage of 400Vdc. Due to time restrictions and occupational health and safety related issues, the experiments were conducted at a low

power level, and the operating input voltage range becomes 40/23Vac with 40Vdc at the bus.

The series converter was demonstrated in a voltage controlled mode and used the sequence based synchronous reference frame approach for voltage regulation. The experimental results show that the series converter can effectively regulate and balance the load voltages under unbalanced conditions.

The shunt converter was demonstrated in a current controlled mode with a closed loop current regulator. The shunt converter was forced to follow one of four operational modes, namely: forced capacitive; forced inductive; real power export and real power import. According to the experimental results, the currents and voltage are 90° out of phase in both forced capacitive and inductive modes, while the phase difference is 0° and 180° for power exporting and importing cases respectively. In the forced capacitive mode, the currents lead the voltages, while in the forced inductive mode, voltages lead the currents. The power becomes negative when importing from the grid and becomes positive when exporting to the grid.

The DC bus voltage regulation system is also demonstrated to control the DC bus voltage on the capacitor at the bus. The experimental results show the DC bus voltage effectively regulates the capacitor voltage at the bus while importing power from the grid to provide current to a DC bus load. The parallel converter could be operated with unbalanced voltages to generate a small ripple voltage at 100 Hz on the DC bus voltage.

6.2. Conclusions

This thesis is a systematic exploration and expansion of capabilities of the UPFC based compensator. A UPFC based on two back to back four phase leg converters with a reduced DC bus capacitance is introduced with a full range of series and parallel compensation

duties and their control strategies as the further extension of the previous work [19]. This work was based on the simulations only conducted in Matlab Simulink. This work covered mainly voltage regulation, phase balancing and DC bus voltage control capability of UPFC.

The shunt converter was only able to draw positive and negative sequence current, because of the use a three leg converter, and no shunt current compensation techniques discussed or implemented.

This thesis introduces new control features for series and parallel compensation of the UPFC based compensator and confirmed these with simulation and some key laboratory experiments. The addition of a fourth leg in the shunt converter provides an additional degree of freedom. The additional features covered in this thesis are:

- Development of a 4+4 leg UPFC based compensator with two four-leg converters - an additional fourth leg is included in the shunt converter.
- The sequence based synchronously rotating frame method is established to regulate the load voltages through a four-leg series converter and a series injection transformer.
- A zero sequence voltage compensation technique is established to remove the zero sequence voltage which appears at the output terminal during any unbalanced operation of the system.
- Active filtering capability of the UPFC is explored to provide harmonic compensation through the ability of the four-leg shunt converter.
- Zero sequence current compensation is established with the addition of fourth leg in the shunt converter.
- Reactive current compensation is provided which enables power factor correction of the system.

- DC bus voltage control strategies are established when the shunt converter is dedicated to provide zero sequence, reactive and harmonic current compensation.
- Power flow analysis was extended for the 4+4 leg UPFC to include harmonics.
- An equation is provided to calculate the DC bus capacitor size if the shunt converter is controlled to provide harmonic current compensation.

These additional features were confirmed by a series of simulation results conducted in Matlab Simulink. For the verification of the simulation results of the UPFC based compensator by experimental results, a laboratory scale prototype of the UPFC was developed, with initial hardware developed and constructed by Peter Wolfs and Ben Sneath. The necessary control software for the experimental test of the designed UPFC functions was developed. The experimental system demonstrated the key fundamental operations of the converter controls such as voltage regulation, parallel current control and DC bus voltage control. The sequence based synchronous reference frame control method is used for the series voltage regulation, while the parallel converter current control and the DC bus voltage control are performed in abc coordinates. The effectiveness of the control loops and the accuracy of the developed software were confirmed by the successful operation of the control loops.

6.3. Future Work

Our work will focus on experimental demonstration of additional controls for zero sequence, reactive and harmonic current compensation and 2ω voltage ripple suppression from the DC bus voltage. Future work will be focused on the experimental demonstration of the advanced control methods including:

- Active filtering/harmonic current control: This will provide harmonic compensation current for nonlinear loads by allowing the four-leg shunt converter to draw harmonic currents.
- Zero sequence current control: This will provide zero sequence/neutral current compensation in a four-wire LV distribution system during any unbalanced operation by allowing the shunt converter to draw zero sequence current.
- 2ω bus voltage control: The 2ω or 100 Hz ripple voltage can be removed by the action of 2ω control loops.

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Chapter 7 APPENDIX A: DETAILS OF THE DEVELOPMENT BOARD

A. 1 The experimental development board

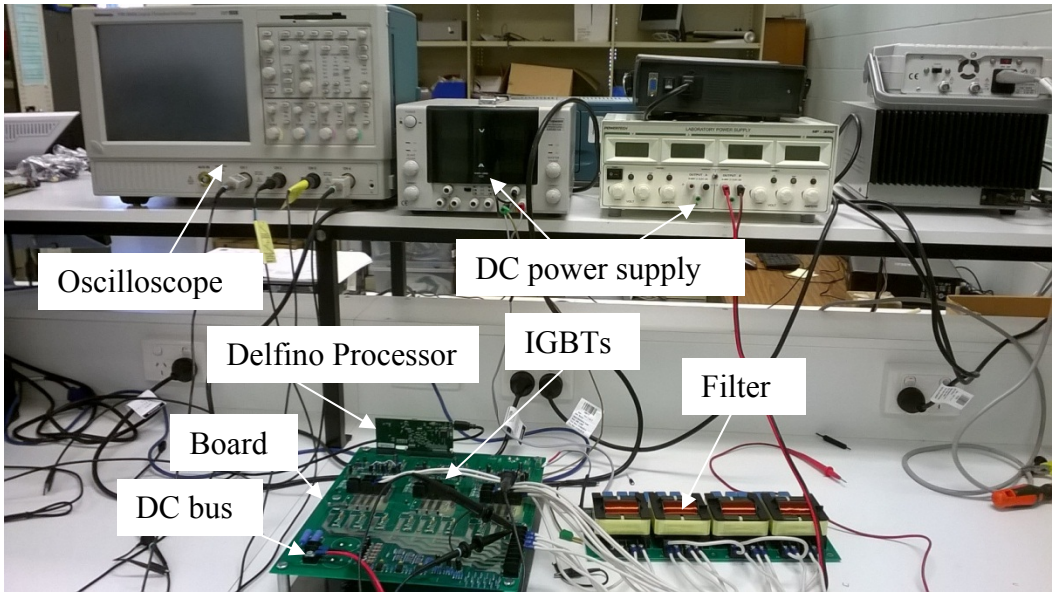

Figure A.1 Photograph of the development board of UPFC based compensator under testing

The development board of the proposed UPFC based compensator and the experimental set-up arrangements are shown in Figures A.1 to A.3. The development board with the input filter inductor is shown in Figure A.1. In this stage, the 3-D-SVM is programmed for the open loop PWM output signals from the Delfino processor and applied to the four legs of the series and shunt converter of the proposed UPFC based compensator to get the open loop modulated sinusoidal wave from the output terminal of the converters. An external DC power supply is used to power up the DC bus and IGBTs and the Delfino processor. The input filter is to remove the ripple due to the grid side disturbances. Figure A.2 represents the complete experimental set-up used for control of the UPFC based compensator to provide voltage and current compensation for the load within an electrical equipment cabinet. The cabinet has four slots. In the top slot, a DC power supply is placed to supply the DC bus and the inverter development board, with some measurement points placed in the second slot.

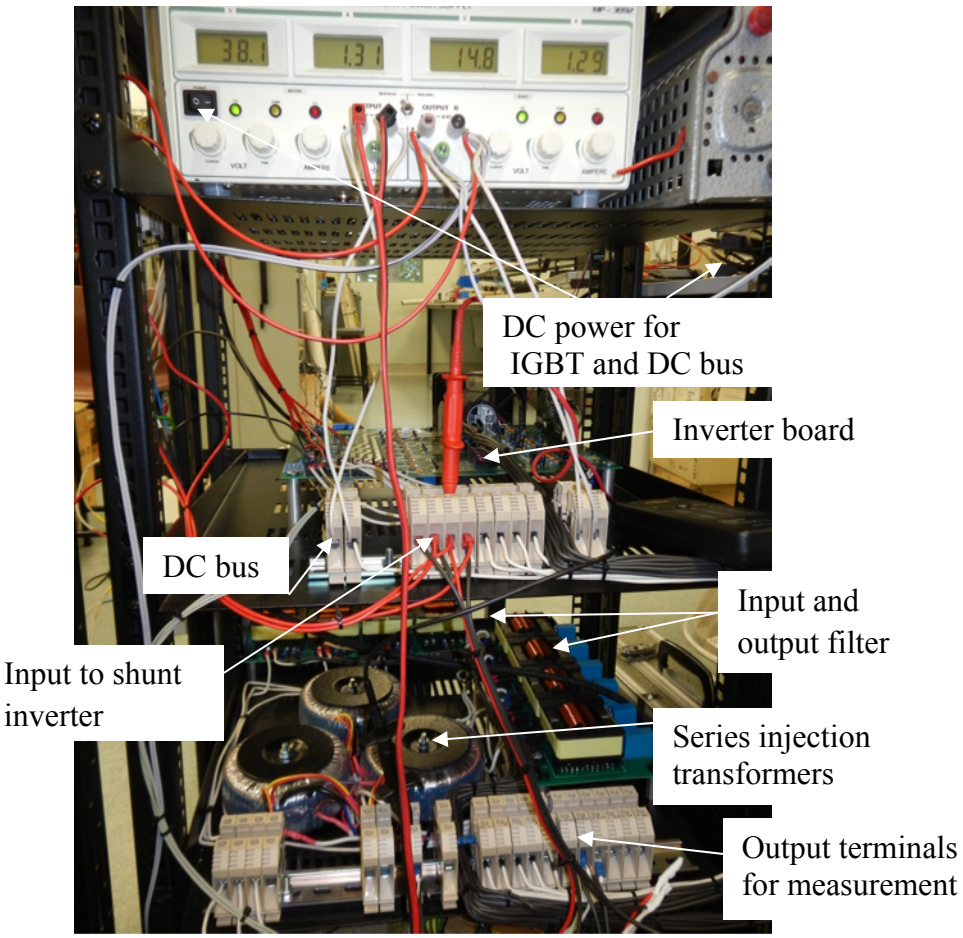

Figure A.2 View of the experimental set-up for UPFC based voltage compensator in the power engineering laboratory at CQUniversity

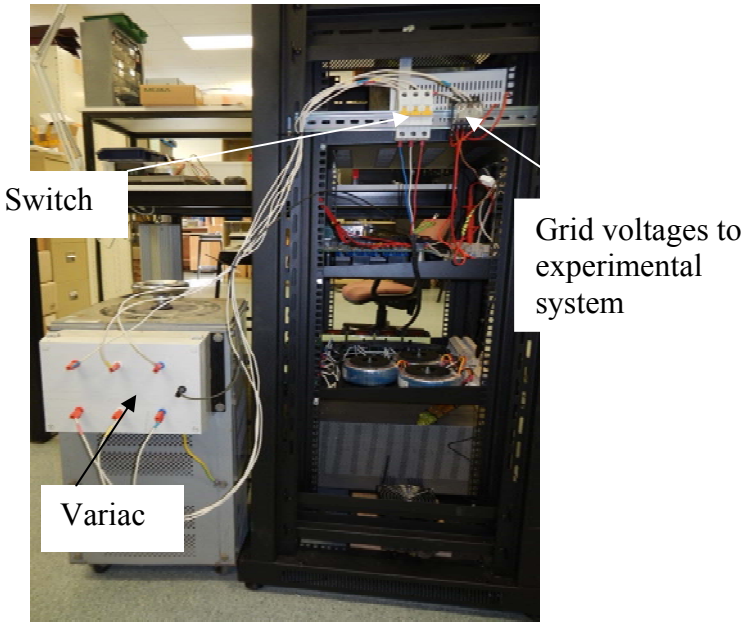

Figure A.3 View of the experimental set-up for UPFC based voltage compensator in the power engineering laboratory at CQUniversity

The series injection transformer and the input and output filter are placed in the third slot, with some loads placed at the bottom slot of the cabinet. Figure A.3 shows the other side of the case where a switch is used between the incoming source voltage and the input of the variac. The output of the variac is supplied through a relay to the designed experimental system.

A. 2 Schematic diagrams of the development board

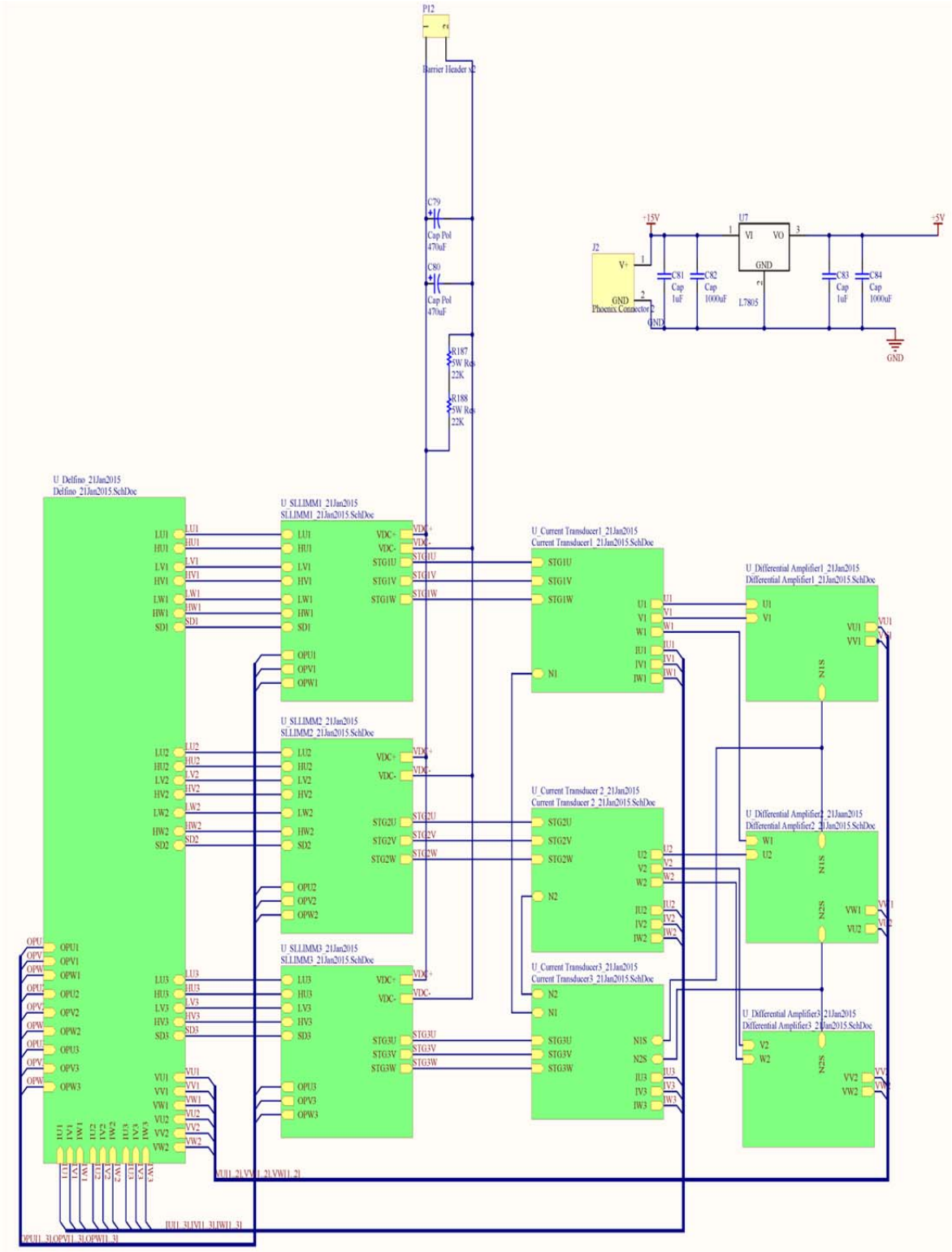

Figure A.4 Internal circuit diagram of the UPFC based compensator development board

The complete schematic of the UPFC development board is shown in Figure A.4. The UPFC development board uses commercial small low loss intelligent moulded modules (SLLIMM), STGIPL14K60 inverter modules. Each inverter module, STGIPL14K60 module has six IGBTs and a total of three modules are used to construct four phase legs for both series and shunt converters. These two converters are equipped with current and voltage measurement channels provided by the current and voltage transducer as seen from Figure A.4. The two converters are controlled by the Delfino processor from the DSP Texas family. A DC internal power supply is shown in the top right corner of Figure A.4. The internal architecture and the connection of the Delfino processor with the IGBTs, current and voltage transducers are shown in Figure A.5. The pins of the Delfino processor used are represented by the yellow coloured arrow shapes. Figures A.6 to A.8 show the connection diagram of three independent 3-phase inverter modules. To build the series and shunt converters of the UPFC based compensator, three inverters are used which are rated at 15A, 600V and commonly used for domestic applications such as refrigerators, air conditioners, washing machines and sewing machines. Each STGIPL1460 IGBT module has three phase legs and three independent STGIPL1460 IGBTs are used to produce a total of eight phase legs. These eight phase legs are used to construct series and shunt converters of the UPFC based compensator with four phase legs. The inputs to the IGBTs are modulated PWM signals generated from the Delfino processor and these are represented as LU1 and HU1 for phase leg U, LV1 and HV1 for phase leg V, and LW1 and HW1 for phase leg W of STGIPL1460 IGBT 1. Since there is an internal built in logic for inversion in each phase leg, the pointers are externally wired such that only one input (either low or high logic) from the processor is applied to each phase leg. SD represents smart shut down function.

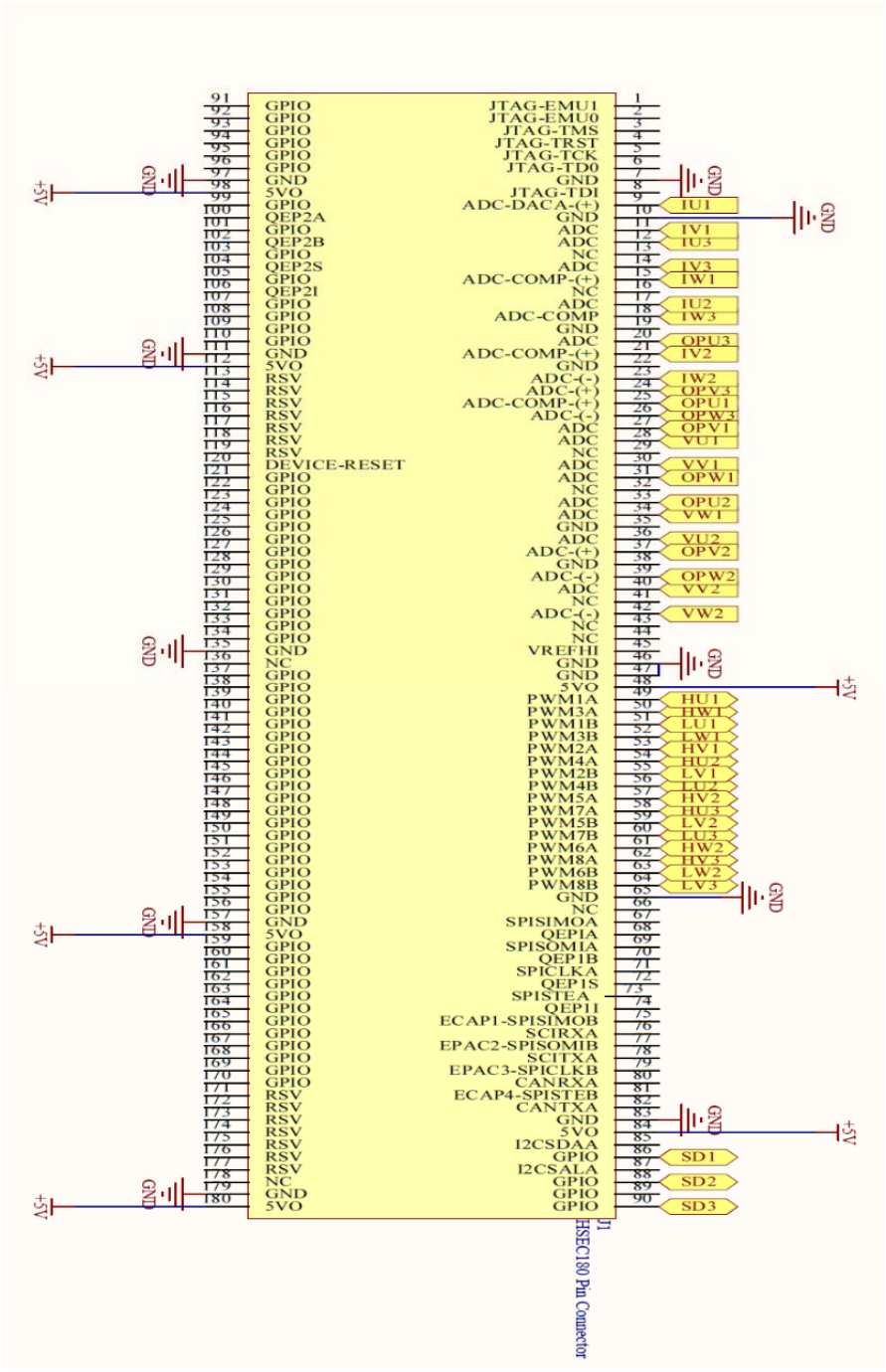

Figure A.5 Connection diagram of the Delfino processor with the inverters, voltage and current transducers

The duty of this control circuit is to measure the temperature of the STGIPL1460 module stage and, if it overheats to a certain temperature, the shutdown unit becomes active and shuts down the inverter stage. For each logic input channel of the converter, there are some resistors and capacitors branch of identical values for each channel used for filtering purposes to remove noise. The outputs from each of the phase legs of STGIPL1460

inverter module 1 are represented by STG1W for phase leg W, STG1V for phase leg V and STG1U for phase leg U. Figures A.9 to A.11 show the internal connections of the current transformers with the STGIPL1460 module. Each current transducer has three channels, and three independent current transducers are used to measure the currents from each phase leg of the series and shunt converters of the UPFC based compensator.

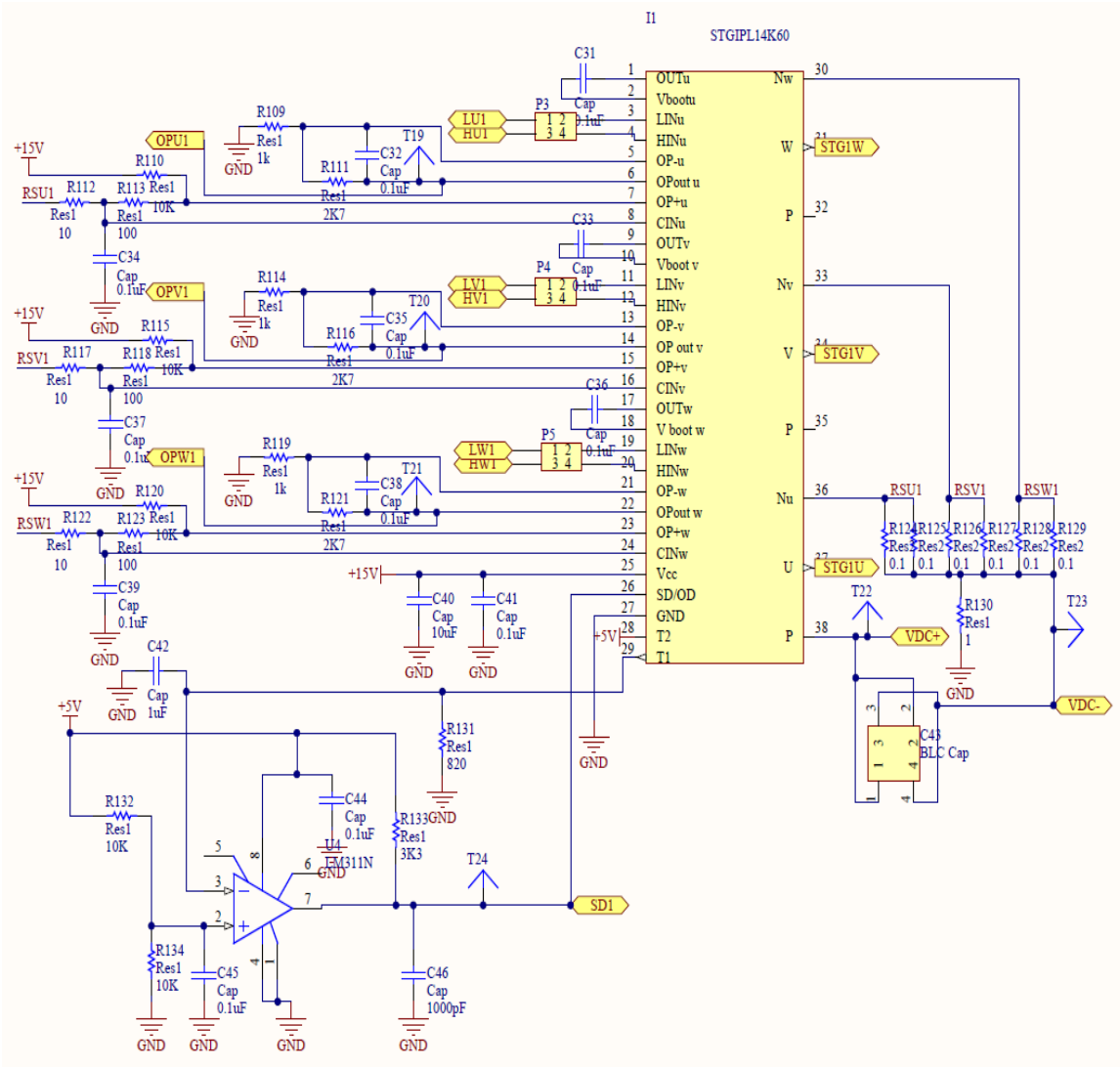

Figure A.6 Internal connection diagram of STGIPL1460 inverter module 1

From the a total of nine phase legs, six phase legs are used for the series and shunt converter phases, and two legs are used as neutrals for both converters and one leg could be used for other purposes.

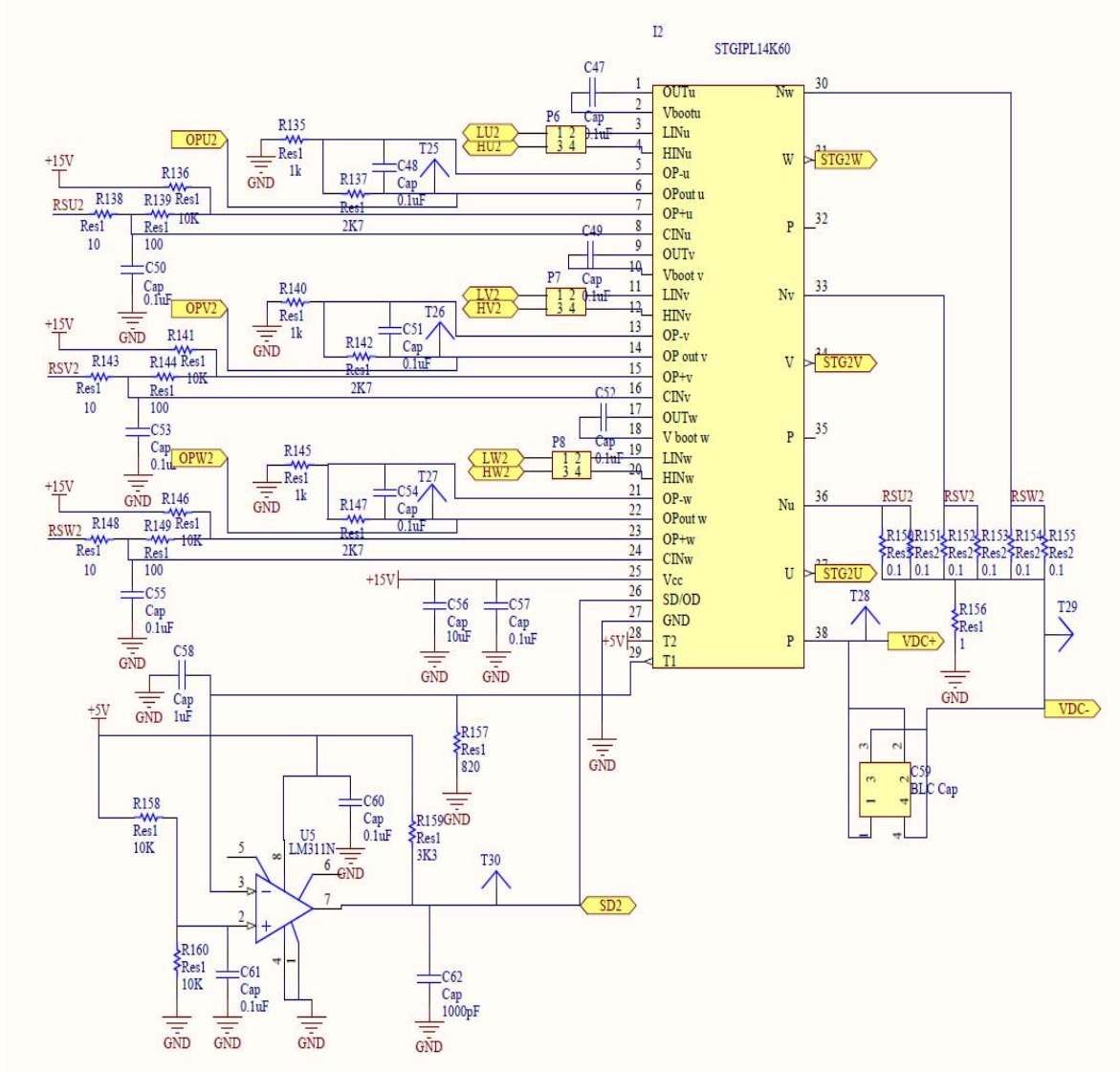

Figure A.7 Internal connection diagram of STGIPL1460 inverter module 2

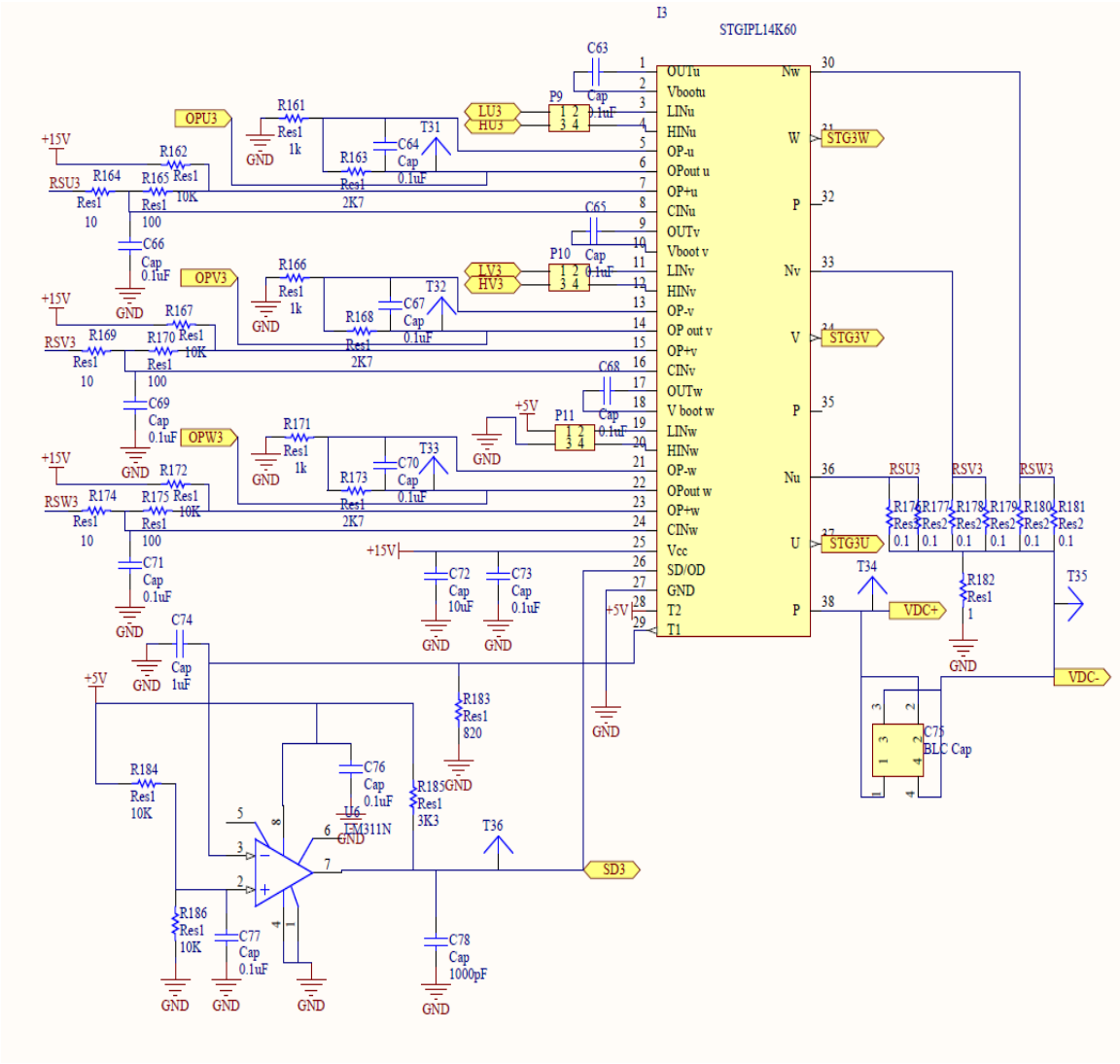

Figure A.8 Internal connection diagram of STGIPL1460 inverter module 3

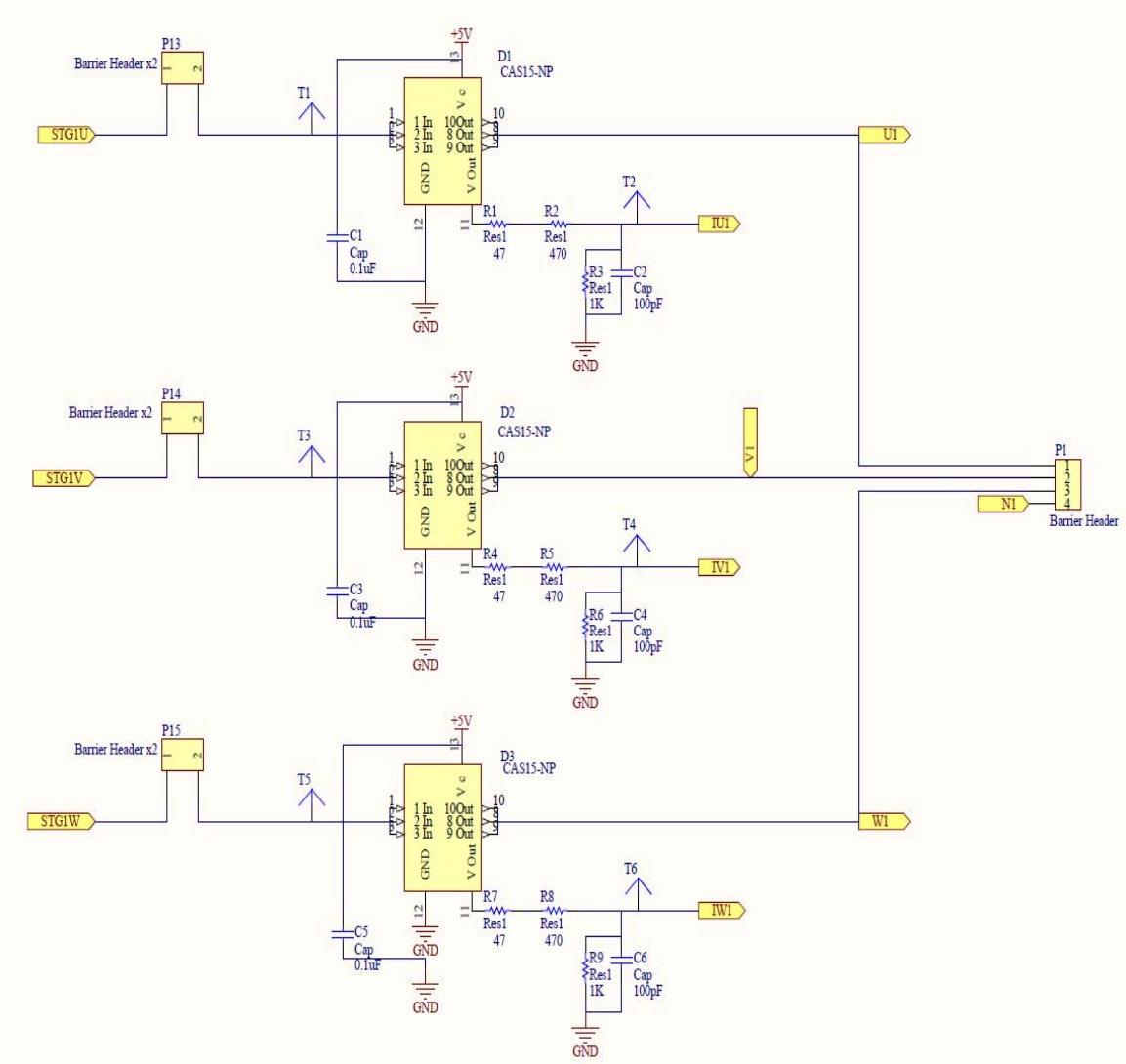

Figure A.9 Internal connection diagram of current transducer 1 with the STGIPL1460 inverter module 1

The inputs to the current transformer are represented by STG1U, STG1V, STG1W for current transducer 1, STG2U, STG2V, STG2W for current transducer 2 and STG3U, STG3V, STG3W for current transducer 3. The output currents of the transducers (IU1, IV1, IW1 to IU3, IV3, IW3) are fed to ADC channels of the Delfino processor and the six voltages of converters are fed to the three differential amplifiers. The resistors R10 to R18 are used for voltage divider for the current transducer. The capacitors C1 to C17 are the decoupling capacitors.

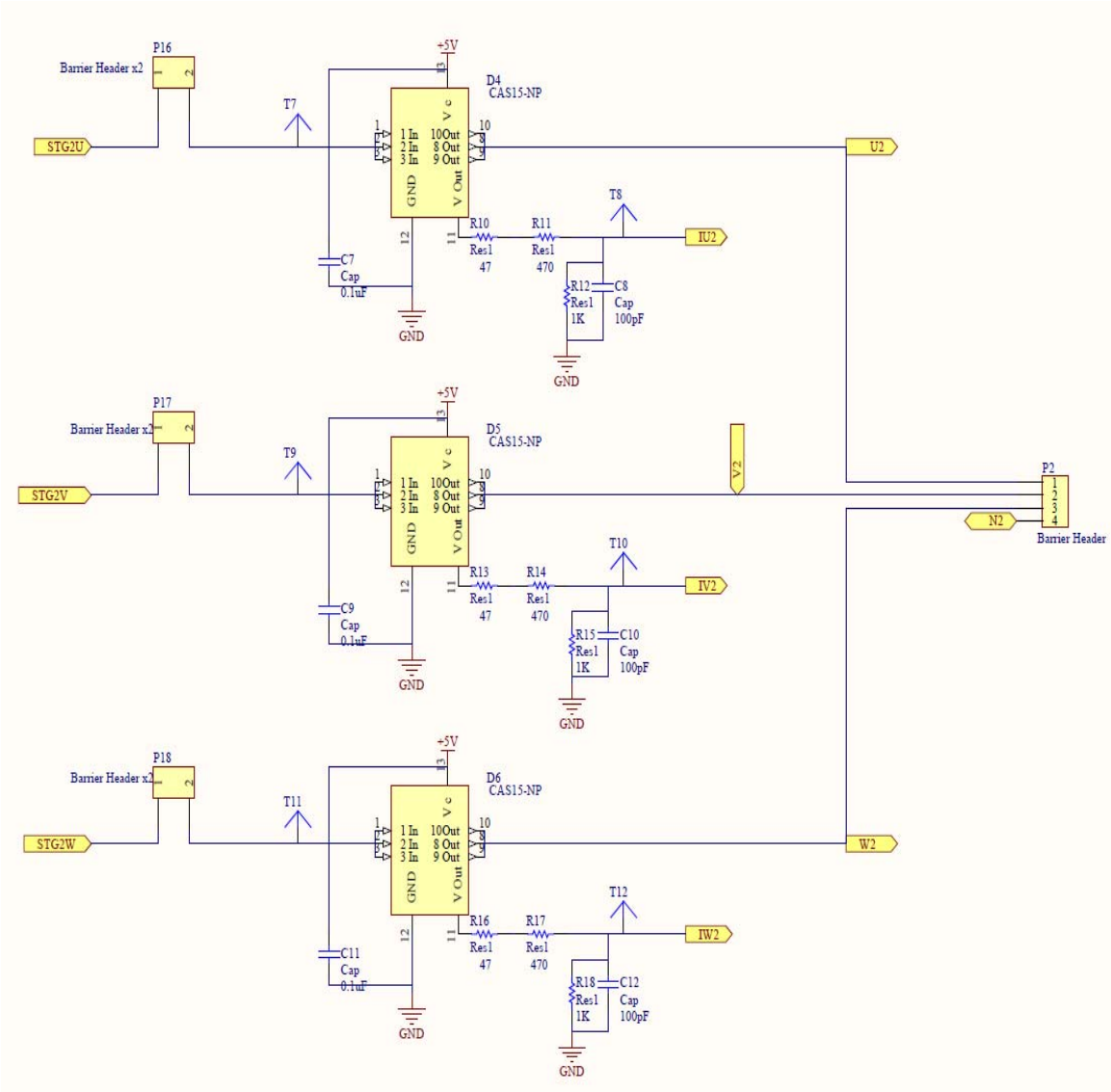

Figure A.10 Internal connection diagram of current transducer 2 with the STGIPL1460 inverter module 2

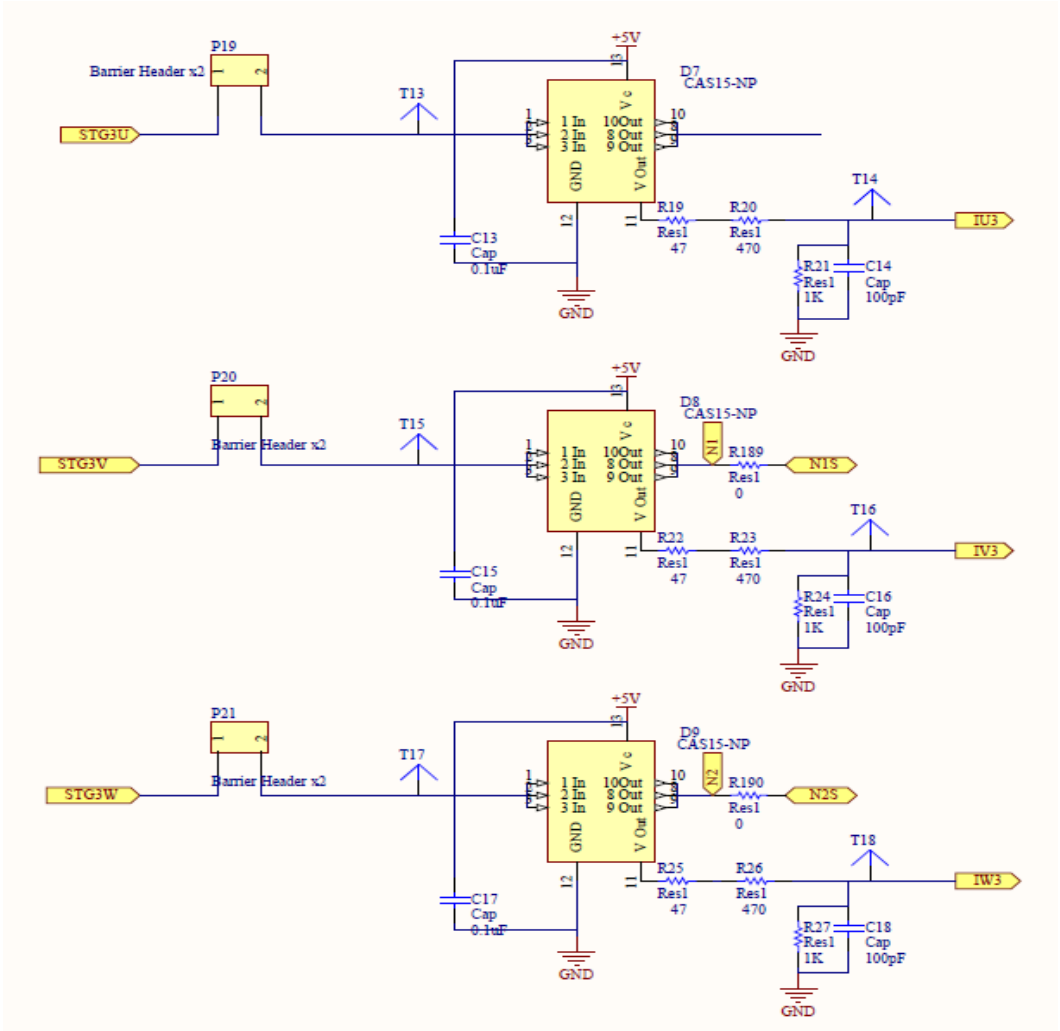

Figure A.11 Internal connection diagram of current transducer 3 with the STGIPL1460 inverter module 3

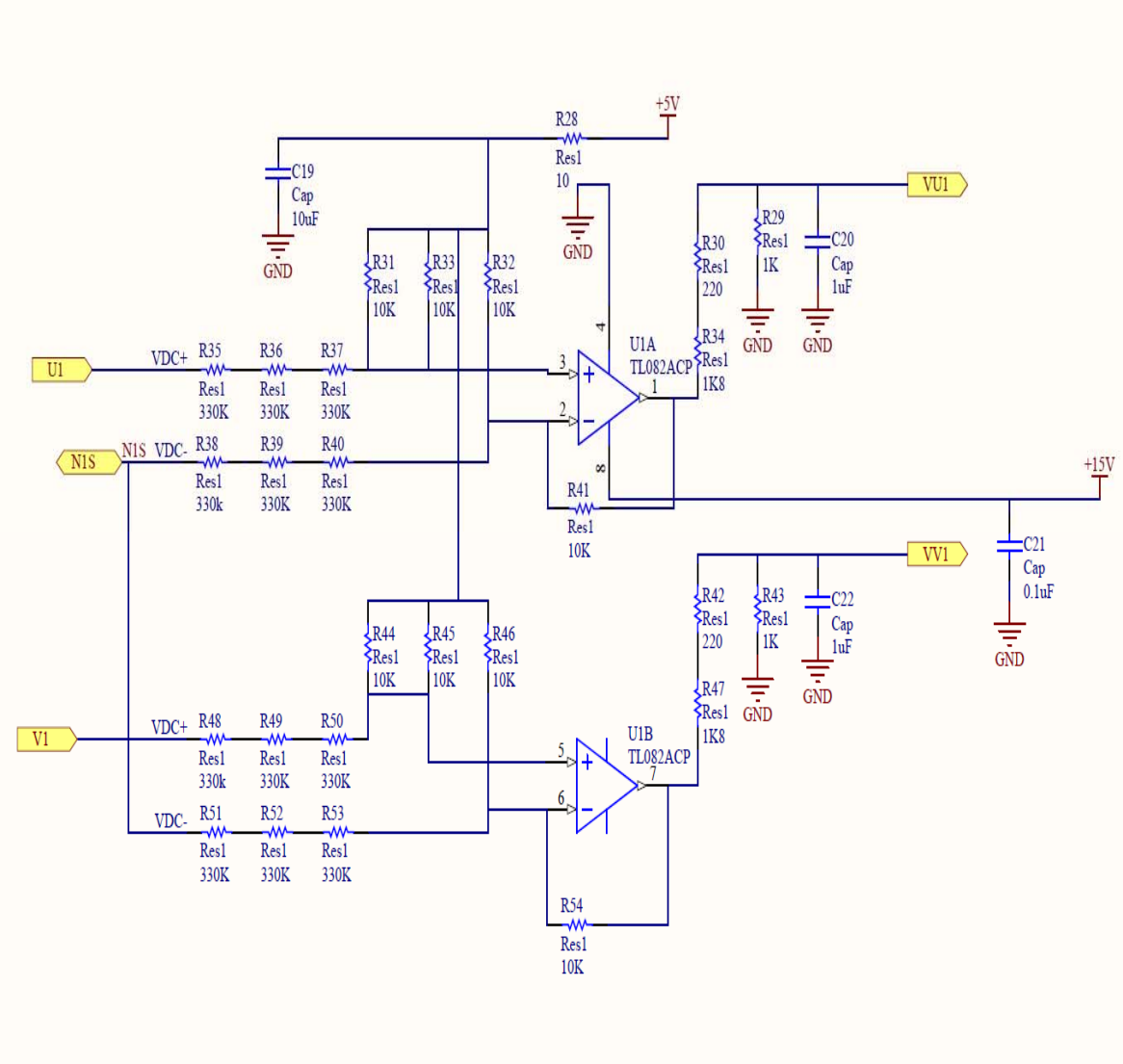

Figure A.12 Internal connection diagram of high impedance differential voltage amplifier 1 with current transducer 1

The internal connection diagrams of differential voltage amplifiers 1,2,3 with current transducers 1,2,3 are shown in Figures A.12 to A.14 respectively. Three differential amplifiers are used to measure the output voltages of three phase series and shunt converters. The input to differential amplifiers for the series converter are represented by U1, V1, W1 for the three phase legs, whereas U2, V2, W2 are used for the shunt converter. The output from differential amplifiers for the series converter are represented by VU1, VV1, VW1 for the three phase legs, whereas VU2, VV2, VW2 are used for the shunt converter. These are connected with the Delfino ADC channels for analogue to digital

conversion. Resistors R28 to R101 are used for the differential amplifiers for the voltage divider at the input and output of the amplifiers. In addition to these, there are some capacitors used for filtering.

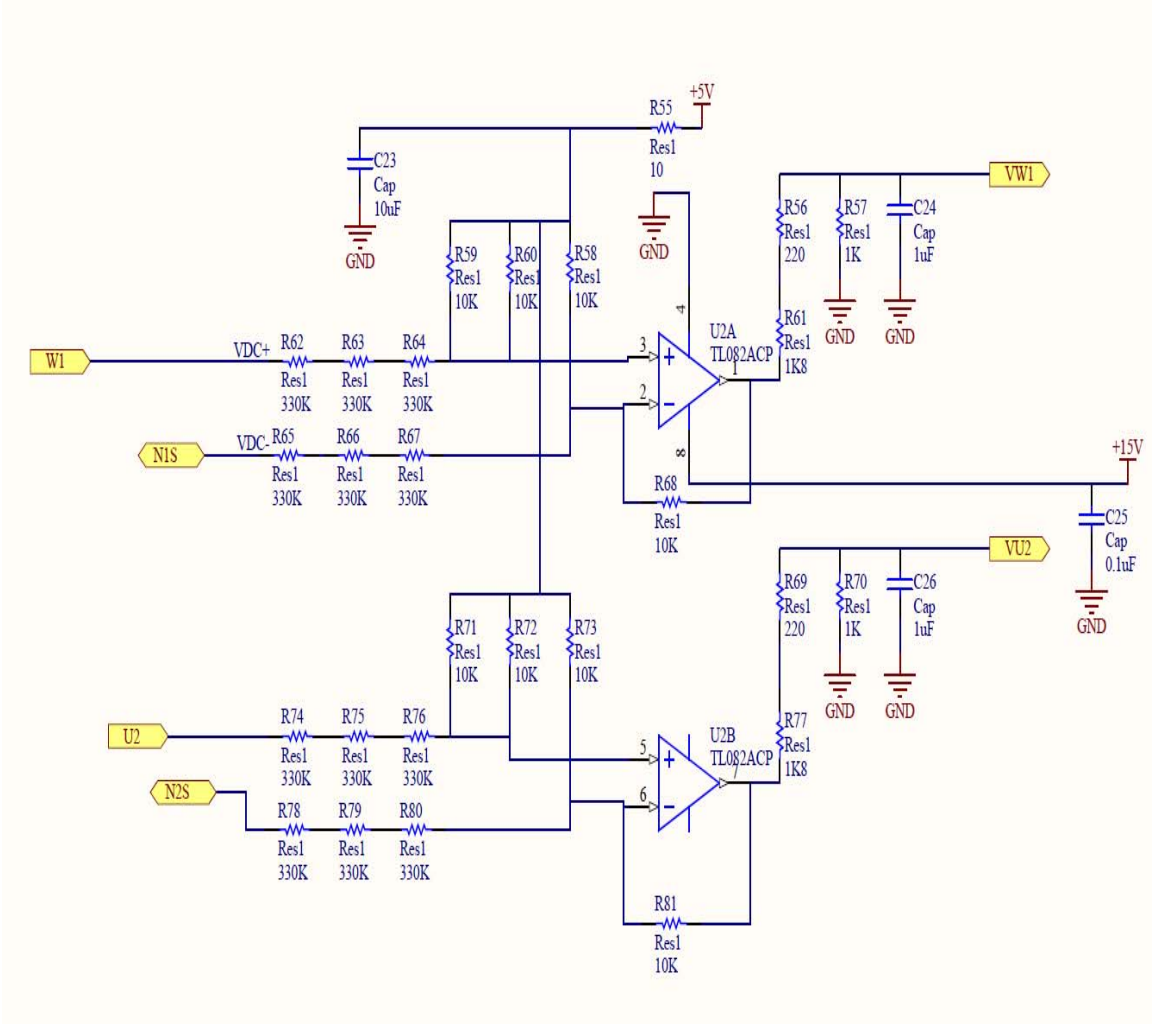

Figure A.13 Internal connection diagram of high impedance differential voltage amplifier 2 with current transducer 2

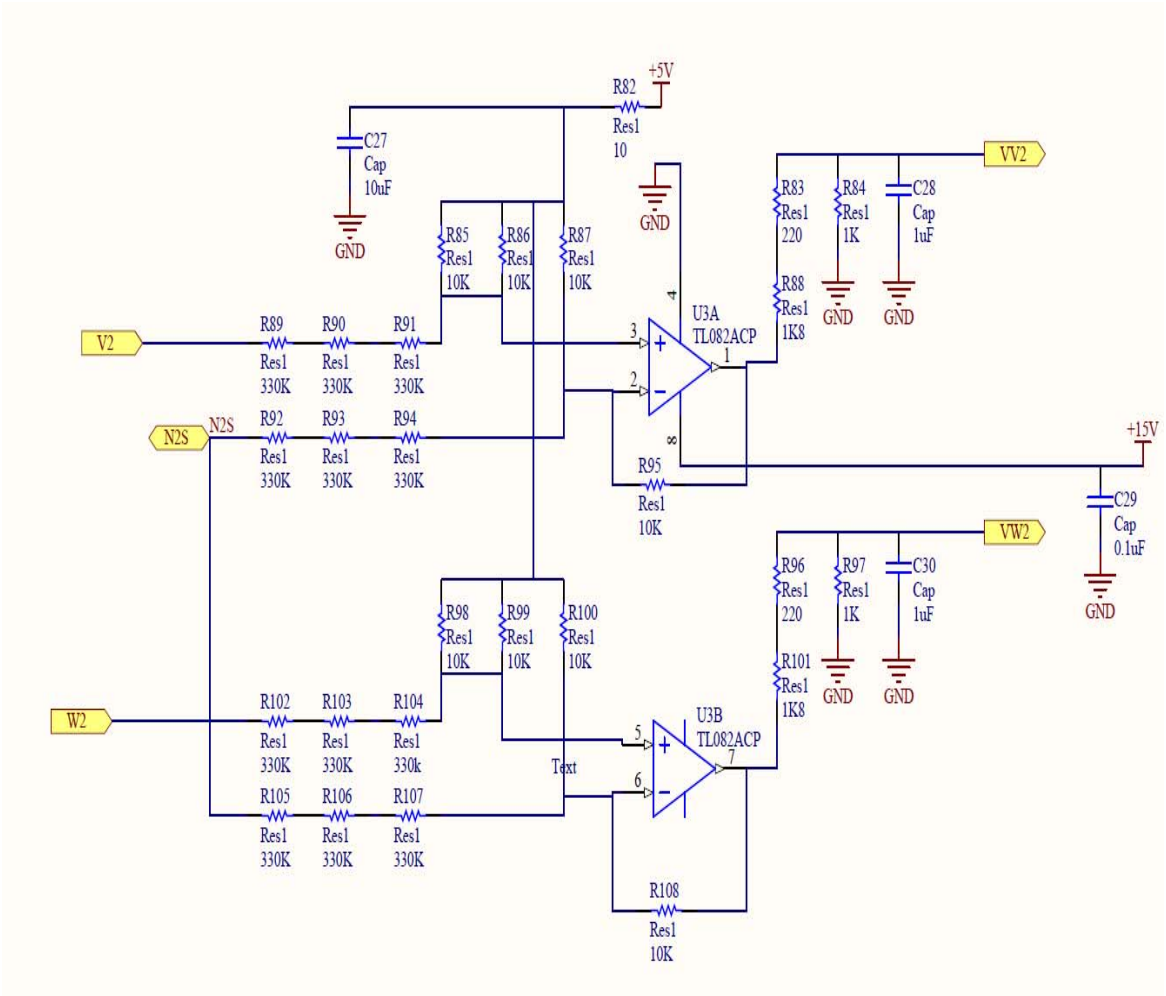

Figure A.14 Internal connection diagram of high impedance differential voltage amplifier 3 with current transducer 3

A. 3 PCB layout of the development board

A PCB layout of the UPFC based compensator is shown in Figure A.15.

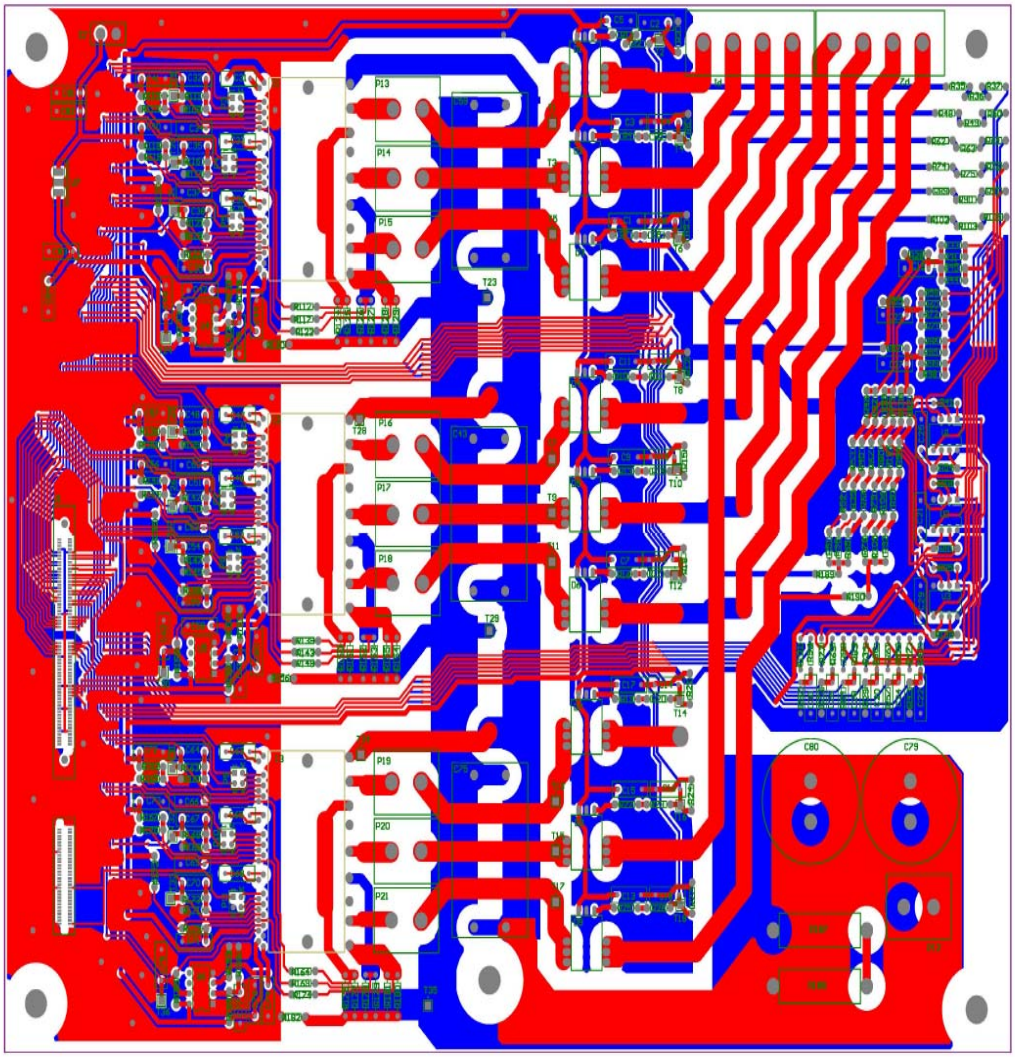

Figure A.15 PCB layout of the UPFC based compensator