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Recent Development in the Topologies for Photovoltaic Module Integrated Converters

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Abstract—The annual world PV cell/module production is growing at almost an exponential rate and has reached 1727 MW in 2005. Building Integrated PV (BIPV) projects are emerging as the strongest part of the PV market and grid interactive inverters are a key component in determining the total system cost. Module Integrated Converter (MIC) technology is one approach that may assist in driving down the balance of system costs to secure an improved total system cost. This paper concentrates on the topology study of the photovoltaic MICs in the power range below 500 W and covers most topologies recently proposed for MIC applications. The MIC topologies are classified into three different arrangements based on the dc link configurations. A systematic discussion is also provided at the end of the paper that focuses on the major advantages and disadvantages of each MIC arrangement. These are considered in detail and will provide a useful framework and point of reference for the next generation MIC designs and applications.

I. INTRODUCTION

Global demand for electrical energy is constantly growing. Among a variety of the renewable energy sources, Photovoltaic (PV) sources have no supply limitations and are predicted to become the biggest contributors to electricity generation among all renewable energy candidates by 2040 [1]. The price per watt of a crystalline PV module has dropped from \$4.23 US in 1992 to \$1.72 US in 2002 [2]. PV cell manufacturing technologies which allow the price to reach \$1 US per watt are evolving [3]. Electronic power inverters are one of the enabling technologies required for utilizing PV energy [4]. Grid interactive PV is the fastest growing segment in the world PV market. There are three widely used systems: the centralized inverter system, the string inverter system and the ac module or the Module Integrated Converter (MIC) system [5]–[7]. Among these, the MIC concept is the trend for the future development but challenges remain in terms of cost and reliability [8].

Globally government subsidized large projects aiming at boosting the solar energy usage have emerged over the last decade including the 70,000 Roofs Program launched in Japan in 1994, the Million Solar Roofs Initiative announced in US in 1997, the 100,000 Roofs Program conducted in Germany from 1998 to 2003, the 10,000 Roofs Program promoted in Italy in 2001 and the 100,000 Solar Roof Program approved in China in 2005. Among these Building Integrated PV (BIPV) projects [9], the MIC technology has significantly benefited the project implementations [10], [11].

A number of single-phase power inverter topologies have been reviewed recently and the interest has been mainly focused on the number of the conversion stages and the design specifications [6], [7], [11]–[13]. This paper concentrates on the topology study of the single-phase PV converters with up to 500-W power rating and attempts to cover a comprehensive set of the MIC topologies proposed in the recent publications. According to the dc link configurations, the proposed MIC topologies can be classified into three different arrangements:

- 1) MIC with a constant dc link,
- 2) MIC with a pseudo dc link,
- 3) MIC without a dc link.

The reviewed MIC topologies in this paper are based on a range of generic converter topologies including half bridge converter, full bridge converter, push-pull converter, buck boost converter, flyback converter, Cuk converter, Zeta converter, D2 converter and two-inductor boost converter. Finally, the discussion for the three different arrangements is provided thoroughly and the favourable features of each arrangement are clearly identified as a sound foundation for future MIC applications.

II. POSSIBLE MIC TOPOLOGIES

In order to achieve good system performance, at least four issues must be considered in the MIC design:

- 1) Power density
One of the highest MIC power densities achieved to date is 0.6 W/cm^3 for a 110-W converter [10]. The goal for the next generation MIC aims at around 1 W/cm^3 [14].
- 2) Efficiency
The highest reported MIC efficiency seen is 94% achieved by NKF OK4-100 at 40% of the maximum input power [15]. A “future” target of 95% was set in 1998 [14]. It is not known if this has been achieved.
- 3) Reliability
The MIC reliability can be measured by Mean Time Between Failures (MTBF) or Mean Time to First Failure (MTFF). Currently a typical figure for MTBF is ten years [16] and that for MTFF is five years [17].
- 4) Balance of system
OK4-100 has achieved \$1 US per watt-peak [15] and PV2GO has a prediction of €0.5 per watt-peak [18]. The objective of less than \$0.5 US per watt-peak set more than a decade ago has not yet been achieved [19].

As the solar panel most often supplies low level dc voltage to the MIC, it is required that both the voltage amplification and the dc-ac inversion be accomplished in the power conversion process. Generally, a MIC can be implemented with either a line frequency or a high frequency transformer respectively shown in Figs. 1 and 2.

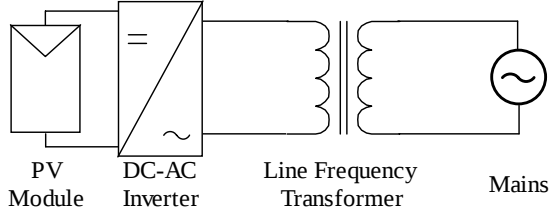


Fig. 1. MIC with a line frequency transformer

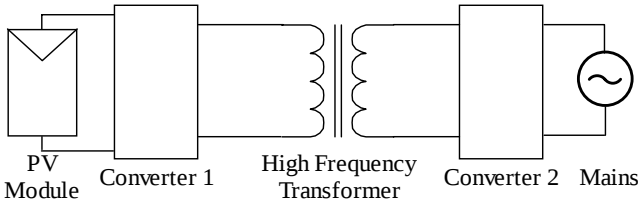


Fig. 2. MIC with a high frequency transformer

In Fig. 1, the dc-ac inversion is implemented first followed by the voltage amplification through a line frequency transformer. Although the topologies recently proposed in [20]-[22] and as well as some other commercial MICs such as Philips EVO series and Dormmuller DMI series still employ this arrangement, the topology shown in Fig. 1 is regarded as a poor solution for the next generation MIC applications because the line frequency transformer is bulky and lossy and almost makes it impossible to develop MICs targeting at over 1-W/cm^3 power density and 95% efficiency.

In Fig. 2, voltage amplification is largely obtained through a high frequency transformer instead and this topology will be the focus of this paper. MICs with high frequency transformers can be classified into three arrangements according to the dc link configurations and these will be discussed in detail in the following sections.

III. MIC WITH A CONSTANT DC LINK

Fig. 3 shows the MIC implementation with a constant dc link, where the dc voltage is amplified to a higher level compatible with the ac grid by a dc-dc converter and a self-commutated dc-ac converter follows. Four topologies have been proposed as shown in Figs. 4 to 7 [23]-[27].

The topology in Fig. 4 utilizes a soft-switched dc-ac inverter [23]. The detailed dc-dc converter topology is not provided as the improvement is concentrated on the dc-ac conversion stage, where a Zero-Voltage-Transition (ZVT) pulse-width modulated (PWM) inverter is employed to remove the switching loss in the conventional design.

The topology in Fig. 5 employs a series resonant half bridge converter in the dc-dc conversion stage [24]. Also a modified full bridge converter is used for the dc-ac conversion and this allows the switching loss to be reduced compared with the conventional PWM converter.

The inverter in Fig. 6 is a flyback converter as the dc-dc conversion stage cascaded with a current PWM inverter as the dc-ac conversion stage [25], [26].

The topology in Fig. 7 employs a Zero-Voltage Switching (ZVS) two-inductor boost converter in the dc-dc conversion stage [27]. A conventional PWM converter follows to convert the dc voltage to the grid compatible ac voltage.

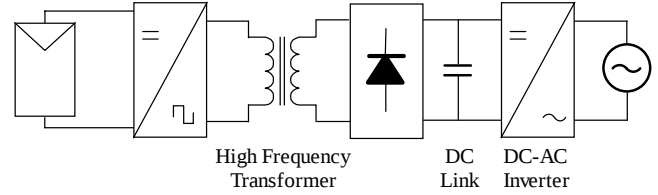


Fig. 3. MIC with a constant dc link

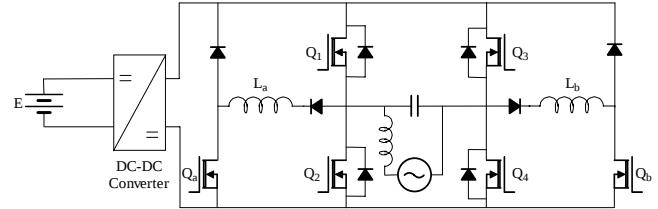


Fig. 4. Topology proposed in [23]

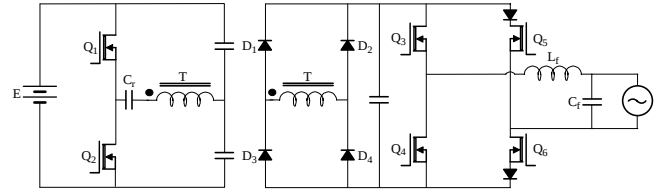


Fig. 5. Topology proposed in [24]

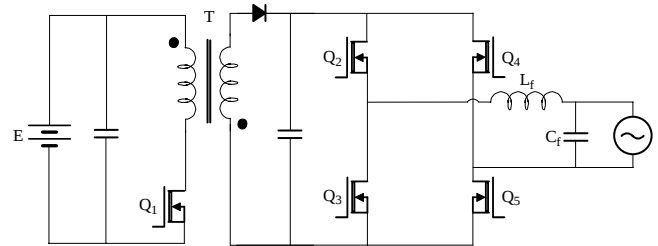


Fig. 6. Topology proposed in [25] and [26]

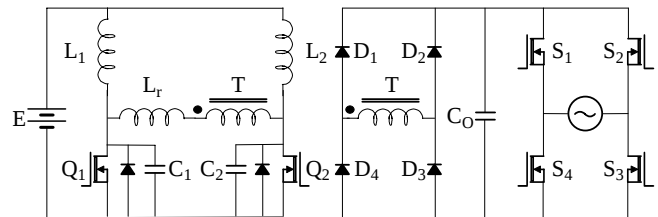


Fig. 7. Topology proposed in [27]

IV. MIC WITH A PSEUDO DC LINK

Fig. 8 shows the MIC implementation with a pseudo dc link, where the dc-dc converter produces a rectified sinusoidal voltage on the dc link and a grid-commutated dc-ac converter with the square-wave control unfolds the link voltage to the sinusoidal form compatible with the grid. Ten topologies have been proposed as shown in Figs. 9 to 17 [28]-[40].

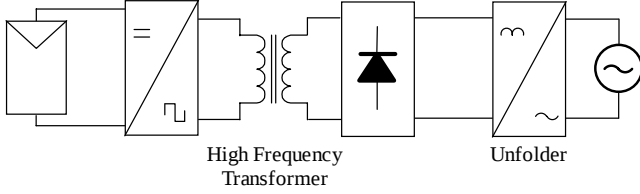


Fig. 8. MIC with a pseudo dc link

The topology in Fig. 9 utilizes a boost converter to increase the voltage level [28]. A push-pull converter is then modulated to generate a rectified sinusoidal waveform, which is finally unfolded by a Current Source Inverter (CSI).

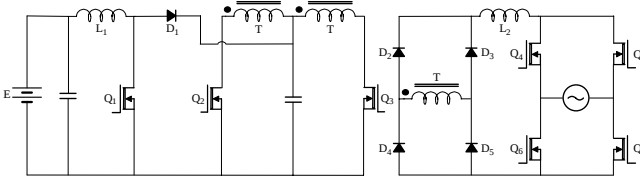


Fig. 9. Topology proposed in [28]

The topology in Fig. 10 is a current fed push-pull converter, which boosts the voltage level, followed by a modulated buck converter, which produces a rectified sinusoidal waveform [29]. This is finally unfolded by a CSI.

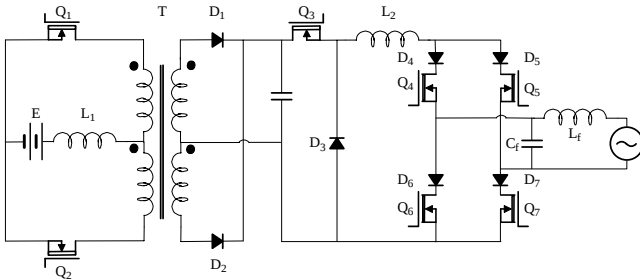


Fig. 10. Topology proposed in [29]

The inverter in Fig. 11 employs a modulated flyback converter to generate a rectified sinusoidal waveform, which is unfolded by the following CSI [30], [31]. This topology is very similar to that shown in Fig. 6 except for the control strategy. The sinusoidal modulation is applied to the operation of the flyback converter in this topology therefore a grid-commutated line frequency unfolders can be utilized.

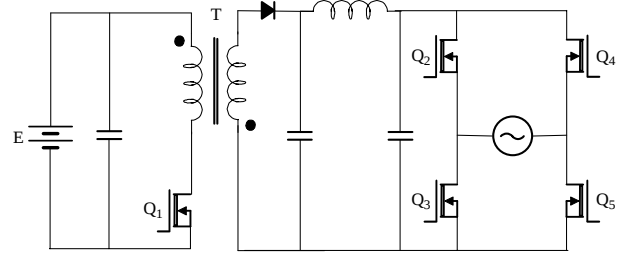


Fig. 11. Topology proposed in [30] and [31]

The inverter in Fig. 12 is a modulated series-parallel resonant full bridge converter with lossless snubbers [32]. This topology is originally based on the topology previously proposed in [33]. A CSI follows to unfold the rectified sinusoidal current produced by the dc-dc conversion stage.

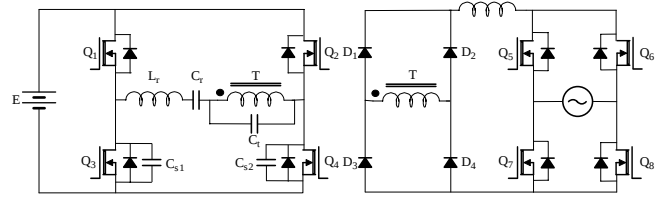


Fig. 12. Topology proposed in [32] and [33]

The topology in Fig. 13 is based on the cascade of the buck boost and the flyback converter [34]. This topology can be improved as shown in Fig. 14 [35]. In this topology, the energy is transferred to the transformer magnetising inductance through the buck boost switch and then to the intermediate capacitor through the flyback switch. Finally, the energy is transferred to the output grid through the centre-tapped transformer and the two ac switches. Compared with that in Fig. 13, the topology in Fig. 14 offers an important feature in recovering the energy stored in the transformer leakage inductance into the intermediate capacitor.

The dc-dc conversion stage in Fig. 15 is a modulated flyback converter and this is the same as that in Fig. 11 [36]. However, a centre-tapped transformer is used in this topology to generate the sinusoidal waveforms. A similar topology is also proposed in [37], where the polarities of the dc voltage source and the primary side MOSFET are reversed.

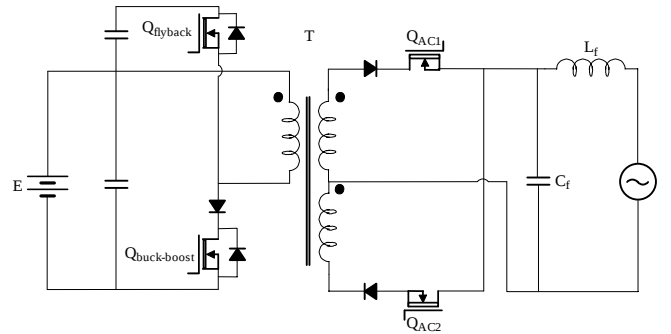


Fig. 13. Topology proposed in [34]

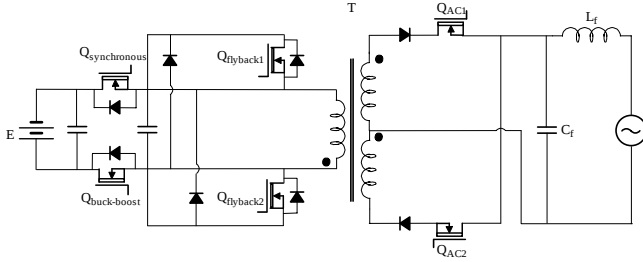


Fig. 14. Topology proposed in [35]

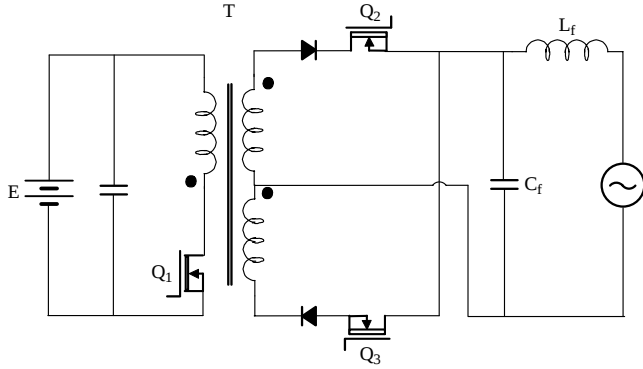


Fig. 15. Topology proposed in [36]

The topology in Fig. 16 is also based on the flyback converter with the centre-tapped transformer [38]. In the converter primary side, an auxiliary switch is added to offer ZVT so that the total switching loss can be reduced.

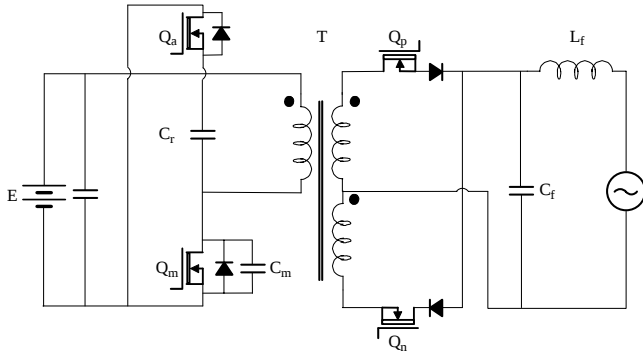


Fig. 16. Topology proposed in [38]

The topology in Fig. 17 employs a highly efficient and sinusoidally modulated two-phase synchronous buck converter cascaded with a two-inductor boost converter to produce a rectified sinusoidal waveform and a voltage unfolding stage follows [39]. Passive non-dissipative snubbers are also used in the converter to partly recover the switching loss in the two-inductor boost converter. The ZVS two-inductor boost topology shown in Fig. 7 can also be employed as part of the dc-dc conversion stage in order to avoid the switching loss in the two-inductor boost converter under high frequency operations [40].

In the MIC arrangement with a pseudo dc link, if a non-isolated dc-dc converter is employed, high frequency

transformer can be removed to offer space and cost saving. Four topologies based on the buck boost converter have been proposed for the multiple-stage inverter as shown in Figs. 18 to 21 [41]-[44]. In these topologies, the buck boost converter is modulated to generate the rectified sinusoidal current, which is unfolded by the following CSI.

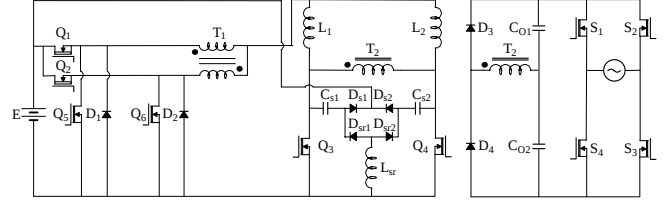


Fig. 17. Topology proposed in [39]

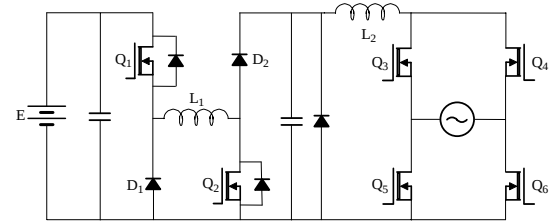


Fig. 18. Topology proposed in [41]

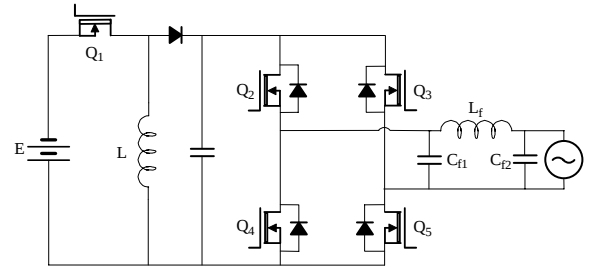


Fig. 19. Topology proposed in [42]

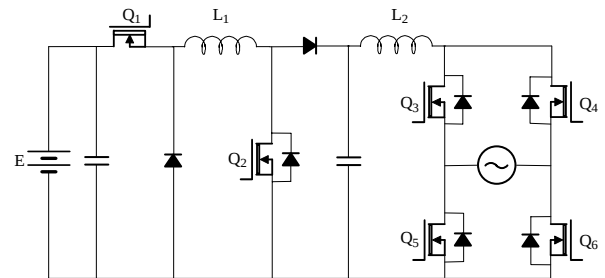


Fig. 20. Topology proposed in [43]

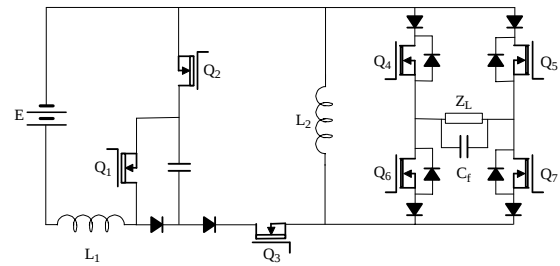


Fig. 21. Topology proposed in [44]

Further size and cost reduction of the MICs can be achieved by the single-stage converter topology. Eight topologies have been proposed as shown in Figs. 22 to 27 [45]-[55]. These topologies normally consist of two relatively independent converters with possible shared passive components and each converter produces a half cycle sinusoidal waveform 180° out of phase.

The topologies in Figs. 22 to 24 are based on the buck boost converter [45]-[49]. The topologies in Figs. 25 and 26 are respectively based on the Cuk converter, the Zeta converter and the D2 converter [50]-[54]. The topology in Fig. 27 is based on the flyback converter [55].

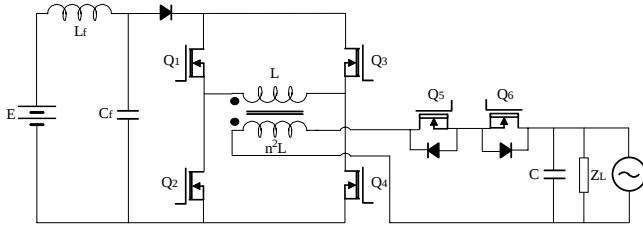


Fig. 22. Topology proposed in [45]

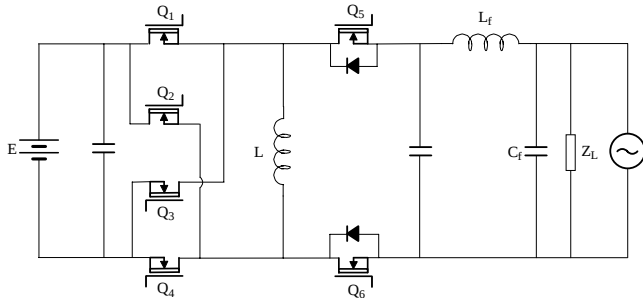


Fig. 23. Topology proposed in [46] and [47]

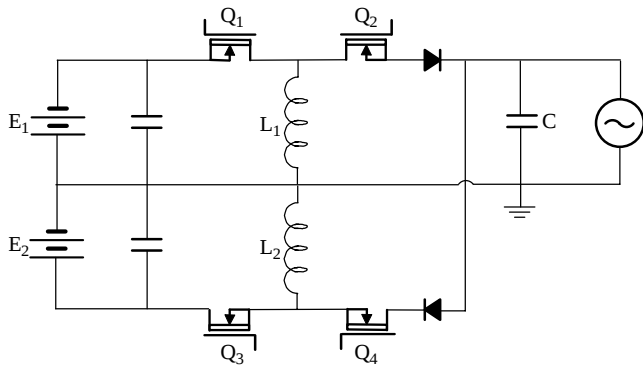


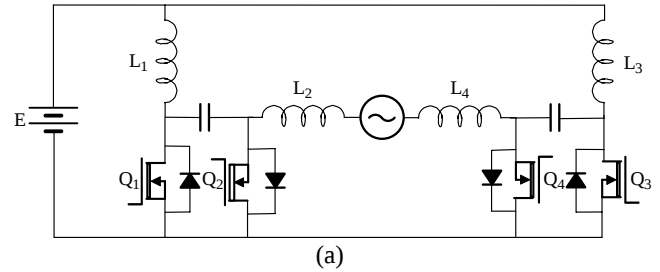
Fig. 24. Topology proposed in [48] and [49]

V. MIC WITHOUT A DC LINK

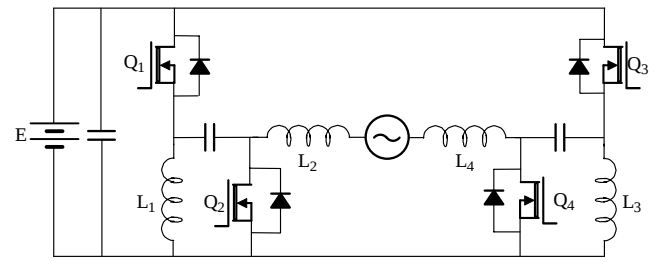
Fig. 28 shows the MIC implementation without a dc link, where the dc voltage is transformed to a high frequency ac voltage and amplified to a higher level compatible with the ac grid. A frequency changer follows and directly translates the ac voltage or current of the high frequency to that of the grid frequency in the absence of any kinds of the dc links.

Three topologies have been proposed as shown in Figs. 29 to 31 [56]-[58].

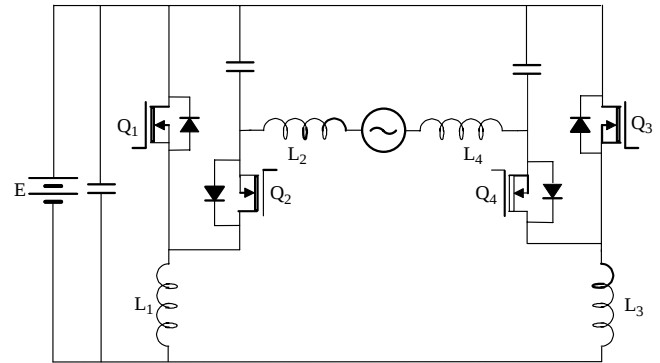
In Fig. 29, a Voltage Source Inverter (VSI) transforms the dc voltage to the ac voltage of the high frequency and this is converted to current source through an impedance-admittance conversion circuit [56]. Finally, a cycloconverter transforms the current of the high frequency to that of the line frequency.



(a)



(b)



(c)

Fig. 25. Topology proposed in [50]-[53]

(a) Cuk-converter-based topology

(b) Zeta-converter-based topology

(c) D2-converter-based topology

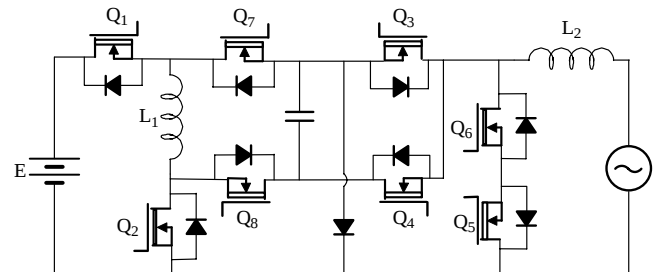


Fig. 26. Topology proposed in [54]

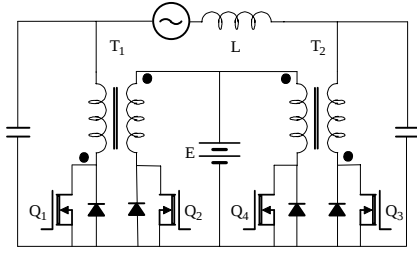


Fig. 27. Topology proposed in [55]

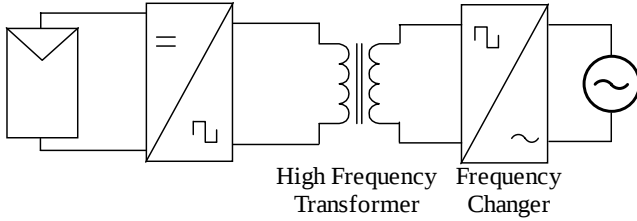


Fig. 28. MIC without a dc link

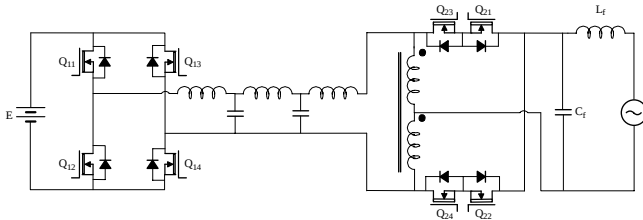


Fig. 29. Topology proposed in [56]

The topology in Fig. 30 is a push-pull converter, which transforms the dc voltage to the ac waveform [57]. The high frequency ac voltage is then converted directly to the ac voltage of the grid frequency through a cycloconverter.

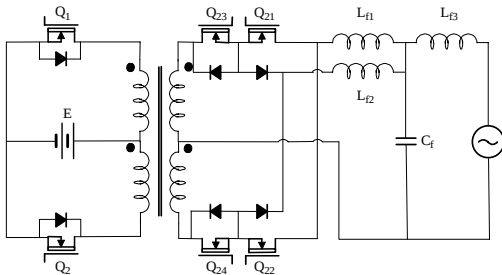


Fig. 30. Topology proposed in [57]

The topology in Fig. 31 is based on the two-inductor boost converter [58]. The two-inductor boost converter first transforms the dc voltage to the high frequency ac current. A frequency changer made up of three bi-directional switches then converts the ac current of the high frequency to the ac voltage of the grid frequency. Another attractive feature of this converter is the non-polarised capacitor as a second phase in the load, which provides the power balance and removes the need of the electrolytic capacitor normally required at the converter input to handle the 100-Hz power ripple common to the single-phase inverter applications.

However, a diode is required to be series connected with the primary side MOSFET in the practical implementation as negative drain source voltages exist due to the power balance design.

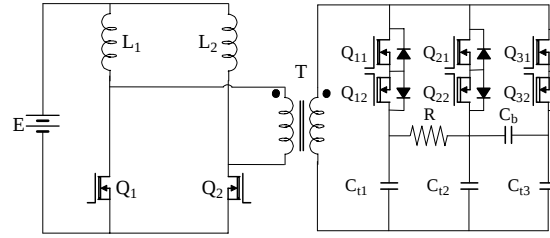


Fig. 31. Topology proposed in [58]

VI. DISCUSSION ON THE MIC TOPOLOGIES

In this paper, MIC topologies are categorised into three different arrangements. This section will discuss the important features for the individual arrangements, which will form a useful reference for future applications.

In the MIC with a constant dc link, the power conversion process can be easily divided into two separate stages – dc-dc and dc-ac conversions. In this case, the dc-dc converter may be controlled to track the maximum power point of the PV module and the dc-ac converter may be controlled to produce ac power of the unity power factor [59]. However, two major drawbacks do exist in this arrangement:

- 1) The dc-ac converter generally requires PWM control in order to meet the harmonic requirements by the grid however this control technique is relatively complex to implement.
- 2) If only the hard-switching topologies are used, the switching loss tends to be high as the semiconductors in both conversion stages switch under high frequencies.

To minimize the drawback of this arrangement, soft-switching technique can be utilized in both conversion stages. However, the trade-off could be a higher component count therefore a higher cost and a lower reliability.

Like other single phase converters, the MICs have the inherent power balance issue and require an energy storage element, more often an electrolytic capacitor, to deal with the 100-Hz power ripple.

In this first MIC arrangement, the power balancing capacitor is preferably to be placed at the constant dc link. As the dc link voltage is of the grid level, the energy stored by the capacitor per unit volume is high and this assists in achieving an overall compact design.

Amongst the three possible MIC arrangements, the MIC with a pseudo dc link has received the greatest interest and a large number of the reviewed topologies employ this arrangement. In the multiple-stage inverters, other than the simple controller design as in the MIC with a constant dc link, the major advantage is that the dc-ac conversion stage operates at the line frequency. Simple square-wave control can be employed and high switching losses can be avoided even with the hard-switched design. However, more

challenging control techniques may be required in the dc-dc conversion stage due to the modulation need.

It is worth mentioning that many transformerless or even single-stage inverters have been proposed under this arrangement. Although they are more compact and efficient due to a smaller component count and lower power loss, these topologies do suffer from the following drawbacks:

- 1) The transformerless inverters have only limited voltage gains without the help of the transformer turns ratio.
- 2) The dual grounding becomes a difficult issue in the transformerless inverters.
- 3) Single-stage inverters have the limited power capacity, the compromised output quality and the limited operation range imposed to dc sources [60].

In this MIC arrangement, the power balancing capacitor is normally placed at the converter input as the dc link needs to provide a wide voltage control range and be free of any large capacitors. Compared with the capacitive energy storage at the dc link, this solution has an obvious disadvantage of lower energy storage per unit volume.

The third MIC arrangement completely removes the dc link in the power conversion process. The major advantage of the frequency-changer-based MIC is the reduction of the total power conversion stages to two. With the current technology, the construction of the bi-directional switches remains a challenge and this greatly hinders the development of the MIC topologies with frequency changers. However, this arrangement does open the possibility of lower component count and higher overall efficiency along with the technology advancement. An obvious trade-off in this arrangement is the requirement of more sophisticated and higher bandwidth controls as no intermediate energy storage stage is present and the power conversion can no longer be identified as independent dc-dc and dc-ac conversion stages.

In this MIC arrangement, the power balancing capacitor normally needs to be placed at the converter input as no intermediate dc link is available. Some improvement can be made if a second phase output can be provided in addition to the load as shown in Fig. 31. In this case the second independently controlled phase adjusts the capacitor voltage to cancel the 100-Hz power ripple. As the capacitor experiences an ac voltage, the capacitor can be easily implemented by a small non-polarized capacitor and the volume and the lifetime issues of the large electrolytic capacitors can be avoided.

The authors hold strong beliefs that the third MIC topology where no dc link exists may become the trend for the development of the next generation MIC with the recent upswing of the research interest in matrix converters and a better semiconductor technology.

VII. CONCLUSIONS

PV energy is one of the favourable renewable energy resources for the mankind and MIC has been proved to be

one of the important enabling technologies in PV utilization. A variety of topologies which have been proposed in the recent publications for the MICs with ratings up to 500 W are reviewed in this paper. Different MIC topologies are categorised into three arrangements based on the dc link configurations. Finally, the important advantages and disadvantages of the individual MIC arrangements are also discussed in detail. Among three different MIC arrangements, the MIC with a line frequency dc-ac inverter currently seems to be the best topology and the frequency-changer-based MIC may be a better candidate for the next generation MIC designs. The thorough discussion of the MIC topologies will form a clear guideline and a useful foundation for future MIC development considerations.

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