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A Current Fed Two-Inductor Boost Converter with Lossless Snubbing for Photovoltaic Module Integrated Converter Applications

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***Abstract*-In this paper, a photovoltaic Module Integrated Converter (MIC) is implemented with a current fed two-inductor boost converter cascaded with a line frequency unfolder. The two-inductor boost cell is fed from a sinusoidally modulated two-phase buck converter with an interphase transformer and operates at a fixed duty cycle. The boost cell features the magnetic integration approach to combine the three cores of the two inductors and the transformer, the lossless snubbers to recover the switching losses and the silicon carbide rectifiers to avoid the reverse recovery losses. The two-inductor boost converter output interfaces with the mains via an unfolding stage, where the MOSFETs are driven by the photovoltaic gate drivers. Experimental results are provided for a 100 W converter developing a single phase 240 V 50 Hz output.**

I. INTRODUCTION

Module Integrated Converters (MICs) provide an alternate solution to interface photovoltaic (PV) systems with ac distribution networks and have become increasingly popular in recent years [1]. Modules of up to a few hundred watts rating are equipped with a small inverter and a Maximum Power Point Tracker (MPPT). Key system requirements are compactness, high reliability and low cost [2].

The two-inductor boost converter, derived by applying the duality principle to the conventional voltage fed half bridge converter [3], has been previously developed as a dc-dc conversion stage to supply a dc-ac inverter in MIC applications [4]. The converter is shown in Fig. 1. In this arrangement, as the voltage fed two-inductor boost converter generates a constant dc link, the Pulse-Width Modulation (PWM) must be used in the dc-ac inversion stage to produce ac waveforms that meet the IEEE standard. However, the PWM control technique requires a relatively complex circuit and introduces additional switching loss.

In order to avoid the penalties associated with a pulse-width modulated inversion stage, this paper proposes a two-inductor boost converter, which has a current source supply from a two-phase buck converter and generates rectified sinusoidal waveforms on the dc link. This makes it possible to reduce the output stage inverter to an unfolder using a more straightforward square-wave control. The proposed topology is shown in Fig. 2.

The front-end two-phase buck converter functions as the current source and feeds the two-inductor boost cell through an auto transformer. The rectification stage of the boost cell employs a voltage doubler. The unfolder operates at the line frequency and the switching losses are removed.

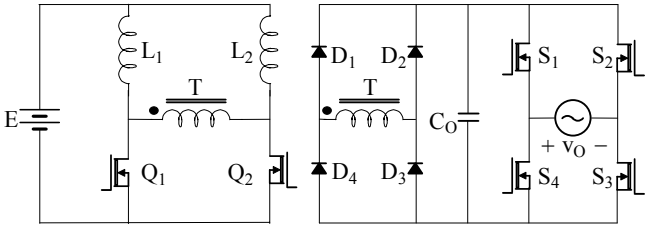

Fig. 1. The two-inductor boost converter with an inverter

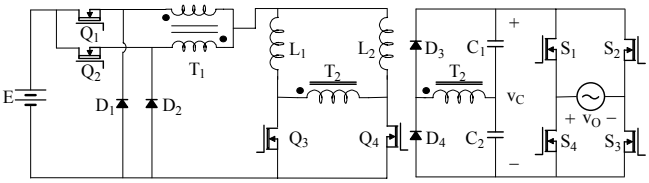

Fig. 2. The current fed two-inductor boost converter with an unfolder

The paper studies thoroughly the operation of the individual stages of the converter including the buck stage, the boost stage and the inversion stage. The beneficial features in each stage are also discussed in detail. The theoretical switching waveforms for the buck and the boost stages are demonstrated to explain their operations. Experimental results of a 100 W converter with 20 V input and 240 V rms output are also provided.

II. THE TWO-PHASE BUCK CONVERTER

In the original hard-switched voltage fed two-inductor boost converter shown in Fig. 1, a variable output voltage can be achieved by varying the switching duty ratios. Because the inductors act as the current sources, however, they require a minimum switch duty ratio of 50%. This results in a minimum output voltage of twice the input voltage and obviously zero output voltage cannot be reached. In order to achieve a zero output voltage, a buck converter must be placed before the boost-derived converter. In Fig. 2, a two-phase buck converter is used to obtain the advantages of higher equivalent switching frequencies without the presence of higher switching losses of the buck converter MOSFETs.

Multi-phase converter arrangements have recently been widely adopted as an efficient approach to parallel multiple converters to provide high current output [5]. Under the multi-phase operation, the currents with an equal phase shift are added together and the equivalent input and output ripple current frequency will be multiplied by the number of the phases. The converter also has less input or output current

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ripple as those in each phase cancel [6]. These benefits ease the requirement on bulky filter components such as inductors and capacitors.

The topology shown in Fig. 2 can be further improved by using synchronous rectifiers as shown in Fig. 3, where a resistive load is used. In Fig. 2, the conduction loss is high as it is partly determined by the diode forward voltage drop. In the synchronous rectifier, the diode is replaced by the MOSFET. This design is able to largely reduce the conduction loss, as the forward resistance of the synchronous MOSFET can be very low [7]. Dead time must be applied to prevent "shoot-through". A Schottky diode is placed in reverse parallel with the synchronous MOSFET in a standard design to avoid the load current flowing through the body diode during the dead time [8].

The output of the two-phase synchronous buck rectifier is fed to the two-inductor boost converter through an interphase transformer (IPT), with 1:1 turns ratio. The IPT enables the equivalent switching frequency of the buck stage to be doubled but not at the cost of a higher switching loss in the hard-switched buck converter. The use of an IPT does require current mode control to ensure good current sharing between the two phases.

III. The Two-Inductor Boost Cell

As the duty ratio of the two-phase synchronous buck converter is modulated in a sinusoidal manner, the two-inductor boost cell, produces the rectified sinusoidal waveform on the dc link with a fixed duty ratio. The output voltage of the two-inductor boost converter is:

$$v_C = \frac{2D_{buck}}{1-D_{boost}} n_{T2} E \tag{1}$$

where D_{buck} is the duty ratio of the buck stage control MOSFETs Q_1 and Q_2, D_{boost} is that of the boost stage MOSFETs Q_3 and Q_4, n_{T2} is the turns ratio of the transformer T_2 and E is the input voltage of the converter. In this case, D_{boost} is fixed at a value slightly greater than 50%.

The boost cell employs the integrated magnetics, the non-dissipative snubber and the silicon carbide rectifiers to serve the purpose of reducing the converter size or loss. These features will be respectively discussed below.

A. Integrated Magnetics

Magnetic integration, which merges more than one discrete magnetic components into a single core configuration, assists in reducing the size of the switched mode power converters [9], [10]. Application of the KVL in the primary side of the two-inductor boost cell in Fig. 3 yields:

$$v_{T2p} = v_{L2} - v_{L1} \tag{2}$$

where v_{T2p}, v_{L2} and v_{L1} are respectively the voltages across the transformer T_2 primary, the inductors L_2 and L_1. Applying Faraday's Law respectively to the windings of the two inductors and the transformer primary gives:

$$N_{p2} \cdot \dot{\phi}_{T2} = N_{L2} \cdot \dot{\phi}_{L2} - N_{L1} \cdot \dot{\phi}_{L1} \tag{3}$$

where N_{p2} and $\dot{\phi}_{T2}$ are respectively the number of turns and the derivative of the flux in the transformer T_2 primary winding, N_{L2} and $\dot{\phi}_{L2}$ are respectively the number of turns and the derivative of the flux in the inductor L_2 winding and N_{L1} and $\dot{\phi}_{L1}$ are respectively the number of turns and the derivative of the flux in the inductor L_1 winding. If $N_{p2} = N_{L1} = N_{L2}$, (3) can be simplified to (4), which allows the magnetic integration to be carried out.

$$\dot{\phi}_{T2} = \dot{\phi}_{L2} - \dot{\phi}_{L1} \tag{4}$$

Three cores for the two inductors and the transformer can be integrated if a three-leg core structure is selected and the individual windings are configured in a way such that the relationship between the individual fluxes given in (4) is fulfilled. An ETD core with equal air gaps in both of the two outer legs is used. A top-view diagram of the winding construction, the equivalent magnetic circuit and the equivalent electrical circuit according to [11] are given in Fig. 4.

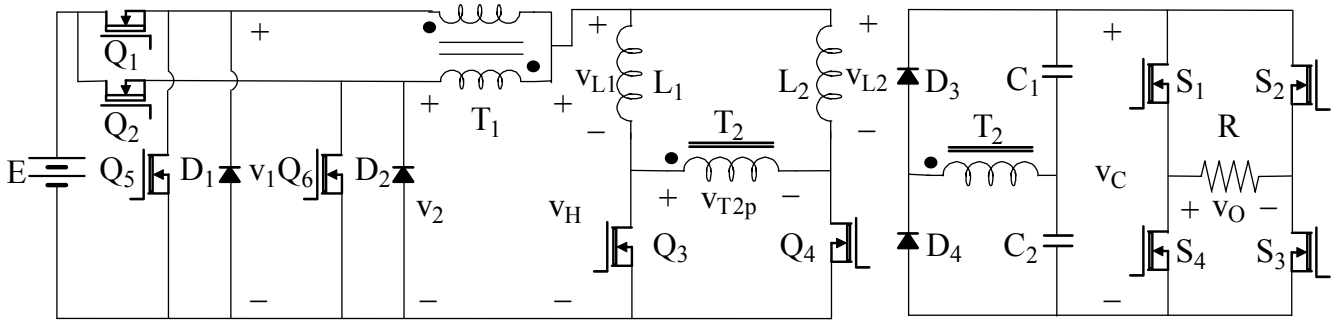

Fig. 3. The converter with the synchronous buck converters

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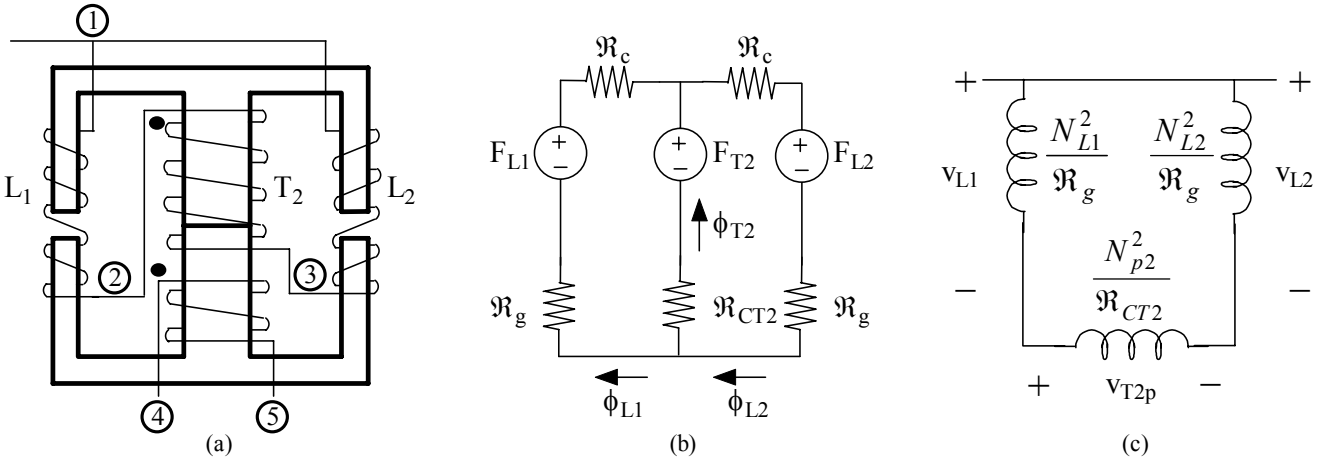

Fig. 4. The integrated transformer and inductors. (a) Top-view. (b) Magnetic circuit. (c) Electrical circuit.

In Fig. 4, $\Re_g$, $\Re_{CT2}$ and $\Re_c$ are respectively the reluctances of the air gap in the outer core leg, the centre core leg and the section of the outer core leg other than the air gap. F_{L1}, F_{L2} and F_{T2} are respectively the magnetomotive forces of the two inductor windings and the transformer winding. In Fig. 4(a), the windings between terminals 1 and 2 form the inductor L_1, those between terminals 1 and 3 form the inductor L_2, those between terminals 2 and 3 form the transformer T_2 primary and those between terminals 4 and 5 form the transformer T_2 secondary. The transformer primary and the two inductor windings have the same number of turns. The equivalent electrical circuit in Fig. 4(c) can be derived from the magnetic circuit shown in Fig. 4(b) as $\Re_g >> \Re_c$. It can be clearly seen that the two input inductances are inversely proportional to the reluctance of the air gap in the outer core leg and the magnetising inductance is inversely proportional to that of the centre core leg. The air gaps in the outer core legs are used to store energy as required by the normal inductor design.

B. The Non-Dissipative Snubber

In the operation of the hard-switched two-inductor boost converter, the transformer leakage inductance is an adverse factor and causes switch over voltage at the MOSFET turn-off. In order to utilize MOSFETs with low voltage ratings or recover the associated loss terms, voltage clamping or snubber circuits must be used. A non-dissipative snubber, which does not require additional control circuit, has been previously introduced with the two-inductor boost converter [3]. Fig. 5 shows the converter with a variation of the non-dissipative snubber. While the original snubber circuit uses two snubber inductors, two snubber capacitors and four diodes, the proposed snubber circuit utilizes only one snubber inductor, two snubber capacitors and four diodes. Space-saving is possible as the inductors are generally in bigger packages than the capacitors and the diodes.

As the input voltage and current to the boost cell follow the rectified sinusoidal waveforms, the peak switch voltage varies. The snubber circuit is therefore only active when the buck stage duty ratio is relatively high. This avoids the energy circulation in the snubber circuit under lower buck stage duty ratios, which could potentially cause additional power losses due to the parasitic effects.

If V_{Cs0} is defined as the initial voltage across the snubber capacitor C_{s1} before Q_3 turns off, it is established that the snubber circuit can operate in three modes under different V_{Cs0} values.

- $V_{Cs0} = -E$

In this mode, the snubber circuit is active and returns energy to the supply. At Q_3 turn-off, the diode D_{s1} is forward biased and input current linearly charges the capacitor C_{s1}. The MOSFET drain voltage linearly increases till it reaches the output voltage reflected to the transformer primary while v_{s1} stays at E. Then the transformer leakage inductance resonates with C_{s1} so that the drain voltage overshoot is controlled by the characteristic impedance and the current in L_1. At Q_3 turn-on, the diode D_{sr1} is forward biased to provide the resonant loop for L_{sr} and C_{s1}. In this mode, the snubber inductor has enough energy to charge the voltage across C_{s1} to –E. At this time, the diode D_{s1} conducts, allowing the current in the snubber inductor to return to E.

- $-E < V_{Cs0} < 0$

In this mode, the snubber circuit is active but does not return energy to the supply. At Q_3 turn-off, the diode D_{s1} is not forward biased instantly as v_{s1} is higher than -E. The input current charges the Q_3 output capacitance till the voltage at the anode of D_{s1} reaches E and the diode D_{s1} is forward biased. Then the snubber operates in the same manner as in the first mode. After Q_3 turns on, L_{sr} and C_{s1} still resonate. However, the diode D_{s1} will stay reverse biased as the snubber inductor does not have enough energy to charge the voltage across C_{s1} to -E and the snubber inductor current will circulate through Q_3 until it reaches zero.

- $V_{Cs0} = 0$

In this mode, the snubber circuit is not active as v_{Cs1} is always zero. All four diodes in the snubber circuit remain reverse biased at all times.

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C. The Silicon Carbide Rectifier

The rectification stage of the two-inductor boost cell is configured as a voltage doubler. Normal PN junction diodes present a relatively long reverse recovery time and result in additional power losses. SiC Schottky diodes have high reverse breakdown voltage ratings and near-zero reverse recovery time [12]. If SiC Schottky diodes are used as the rectifiers, the power losses related to the reverse recovery can be removed.

IV. The Unfolder

As the input of the dc-ac inverter is the rectified sinusoidal waveform, the square-wave control can be applied and the dc-ac inverter is reduced to an unfolder. In the unfolding stage, the switches turn on and off under the line frequency and this avoids high switching losses within the PWM control.

To avoid the high side drivers and the additional control circuitry for the MOSFETs, electrically isolated optical MOSFET drivers are used to provide the gate signals. The MOSFET gate charging current from the optical MOSFET drivers must reach a certain level for short turn-on transitions. The optical MOSFET drivers must also have an embedded active discharge circuit to discharge the MOSFET gate capacitance to obtain fast turn-off behaviours.

V. Design of the Magnetic Components

The IPT is implemented with an EFD15 core. The primary and the secondary windings are respectively made of 14 turns of wire. In order to protect the IPT from being saturated by the unbalanced current from the two phases, an air gap of 0.35 mm is inserted in each of the three core legs.

As it is required that the number of turns of the transformer T_2 primary winding be equal to those of the inductor L_1 and L_2 windings, a larger core, ETD39, is used for the integrated magnetic component to provide a sufficient space for the four windings. The number of turns of the transformer primary winding or the inductor winding is 23 and that of the transformer secondary winding is 98. There is an air gap of 0.5 mm in each of the two outer core legs.

The snubber inductor is designed to be 10 μH. This is made by winding 7 turns of wire onto an RM7 core with 0.16 mm air gap in the centre pole.

VI. The Theoretical and Experimental Results

The switching frequency of the buck stage MOSFETs f_{buck} and that of the boost stage MOSFETs f_{boost} are respectively selected to be $f_{buck} = 150\ kHz$ and $f_{boost} = 75\ kHz$. The theoretical waveforms of the converter with above parameters over high frequency cycles are given in Fig. 6, where T_{buck} and T_{boost} are respectively the switching periods of the buck and the boost stages. Figs. 6(a) and (b) respectively shows the converter waveforms when $D_{buck} < 50\%$ and $D_{buck} > 50\%$. The voltage after the IPT swings between zero and the half input voltage when $D_{buck} < 50\%$, while it swings between the half and the full input voltage when $D_{buck} > 50\%$. The three voltage levels and the frequency doubling effect can be seen in v_H waveform in both cases.

The buck conversion stage is based upon a commercial two-phase synchronous step-down switching regulator – Linear Technology LTC1929CG. Minor modifications are required to the normal control loop to obtain a widely variable output voltage range. The switching of the buck converter is synchronized through the switching controller in the two-inductor boost cell.

Fig. 7 shows the buck converter waveforms under static tests. From top to bottom, Figs. 7(a) and (b) respectively shows the waveforms of v_1, v_2 and v_H with duty ratio D_{buck} lower and greater than 50%. The voltage after the IPT swings between zero and the half input voltage or the half and the full input voltage depending on the value of D_{buck}. In both cases, the frequency of the voltage v_H after the IPT is twice that of voltage v_1 or v_2 before.

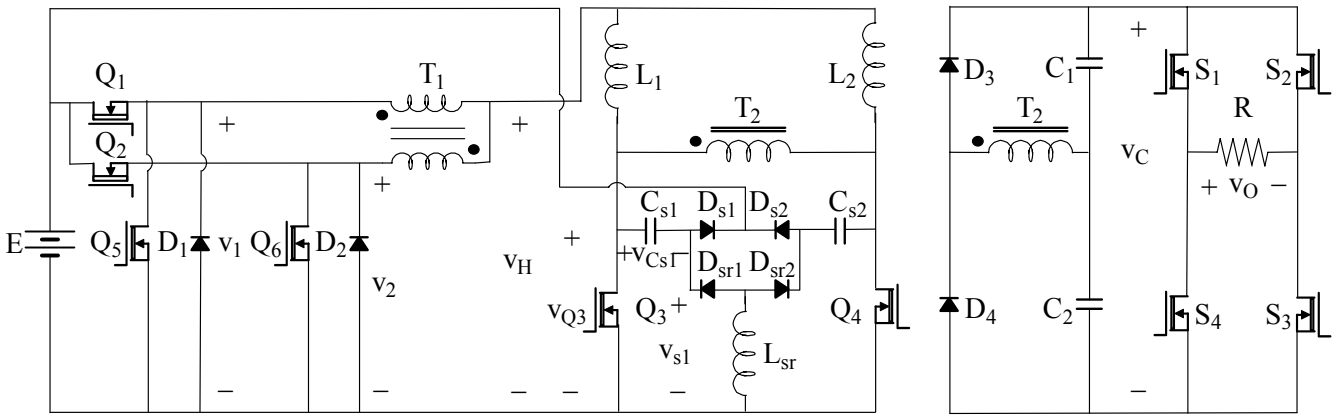

Fig. 5. The converter with the non-dissipative snubber

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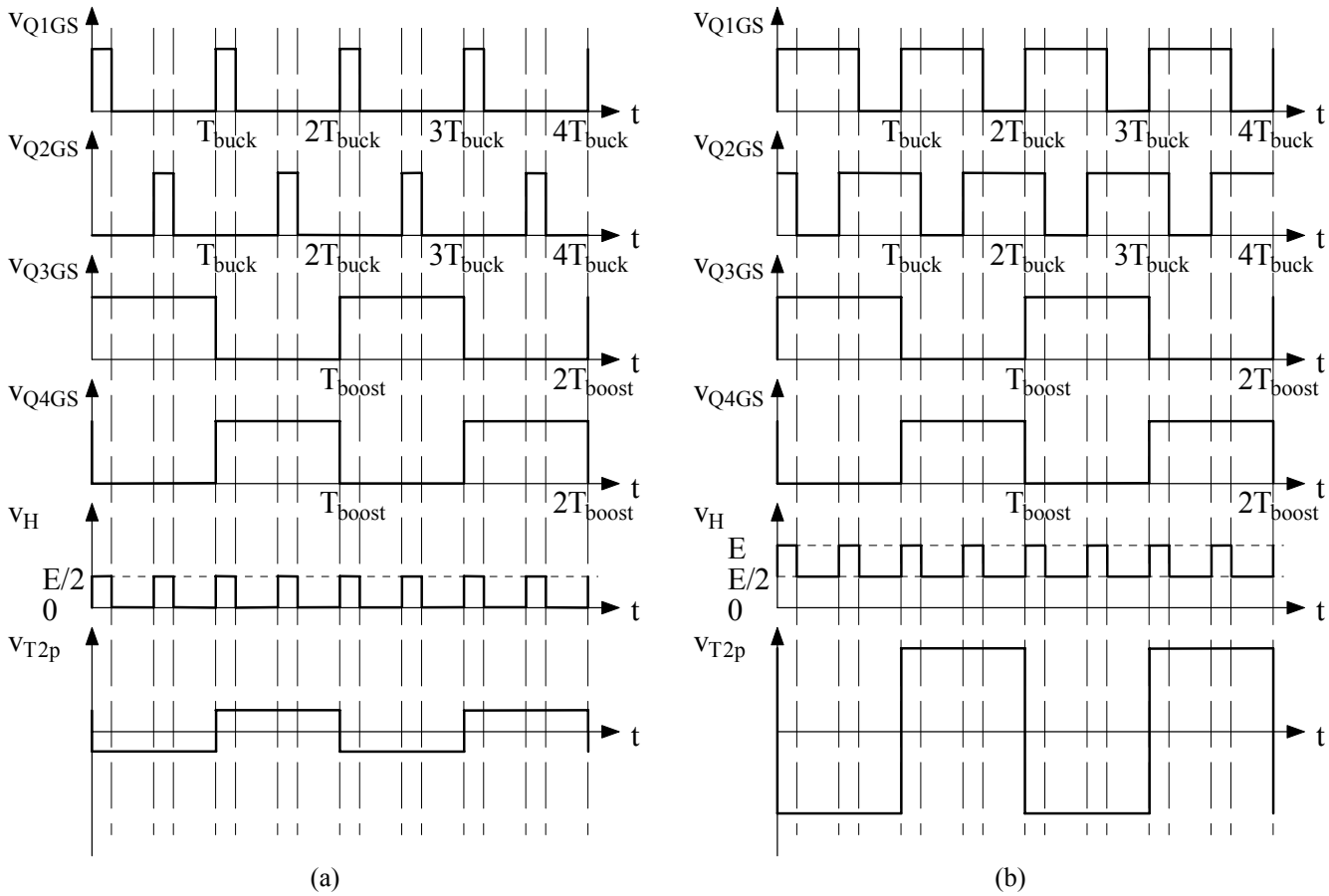

Fig. 6. Theoretical waveforms. (a) $D_{buck} < 50\%$. (b) $D_{buck} > 50\%$.

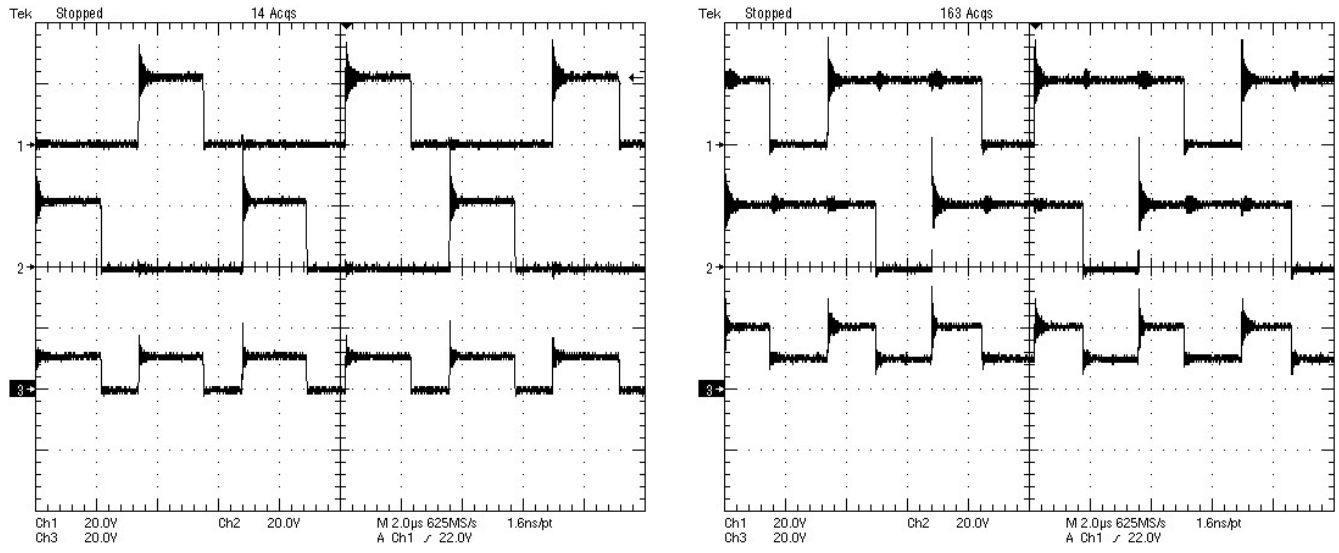

Fig. 7. Two-phase synchronous buck converter waveforms. (a) $D_{buck} < 50\%$. (b) $D_{buck} > 50\%$.

Fig. 8 shows the two-inductor boost converter output voltage v_C and the input voltage v_H from top to bottom during sinusoidal modulation. A three-level modulation can be clearly seen from the v_H waveform although the captured waveform is heavily aliased. Small voltage spikes appear between the half sinusoidal waveforms because all four switches in the unfolder turn off around the zero crossing of the sinusoidal waveforms.

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Fig. 9 shows the gate waveforms of the low frequency unfolder switches and the output voltage V_O from top to bottom. In this case a resistive load is supplied and this is adjusted to give the rated power, 100 W average, at 240 V ac, which is equivalent to the nominal mains voltage. A conversion efficiency of 92% was obtained for the three-stage converter. Input and output powers were measured using the mathematical functions of a Tektronix TDS5034 four-channel oscilloscope equipped with converter input and output voltage and current probes. The current probes are Tektronix TCP202. The power loss includes the losses in all three conversion stages – the buck, the boost and the unfolding stages.

Fig. 10 shows the MOSFETs Q_3, Q_4 drain source voltages and voltage across the SiC Schottky diode when the converter output voltage is close to its peak. The snubber circuit controls the maximum peak switch voltage in a low frequency cycle to around 50 V. This allows the MOSFETs with drain-source breakdown voltage ratings of 55 V to be used in the two-inductor boost cell. MOSFET forward resistances are low under low voltage ratings and this minimize the conduction losses. The SiC diode voltage waveform is relatively clean although some high frequency oscillations exist due to the resonance between the transformer leakage inductance and the diode junction capacitance.

Fig. 11 shows the MOSFET Q_3 drain source voltage v_{Q3} and the voltage v_{s1} from top to bottom when the snubber circuit operates in the first mode. Due to the effect of the snubber circuit, the MOSFET drain source voltage rising slope becomes less steep.

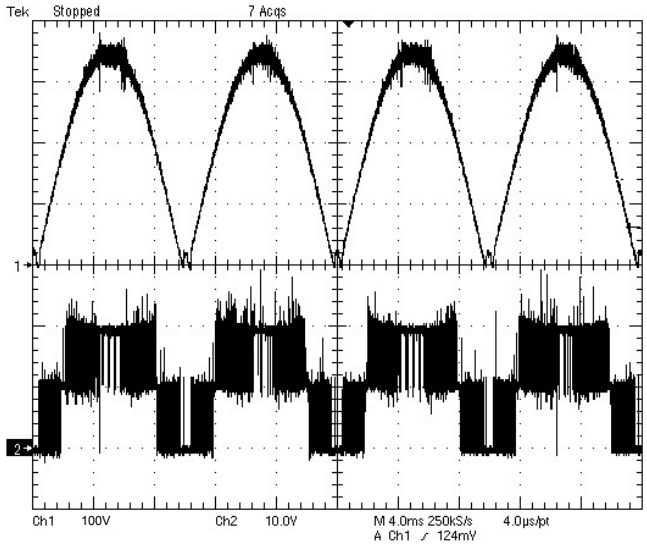

Fig. 8. Sinusoidal modulation waveforms

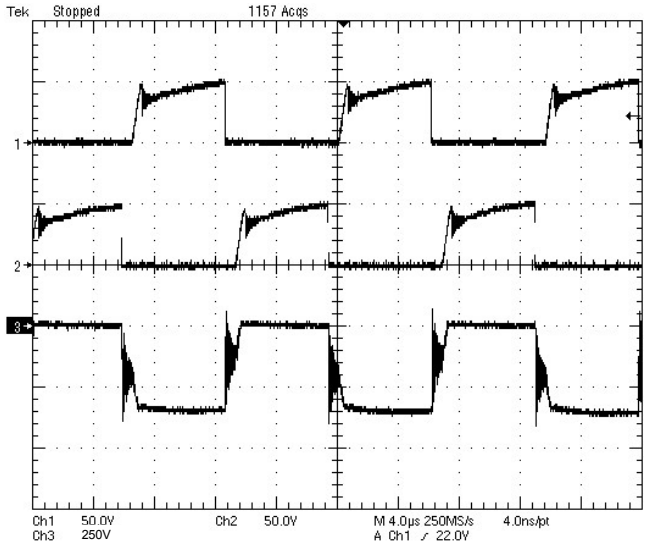

Fig. 10. Mosfet and diode waveforms

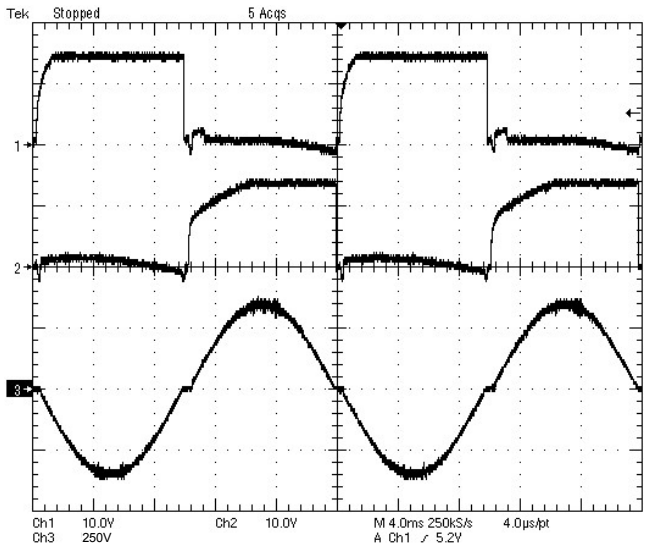

Fig. 9. Low frequency unfolder waveforms

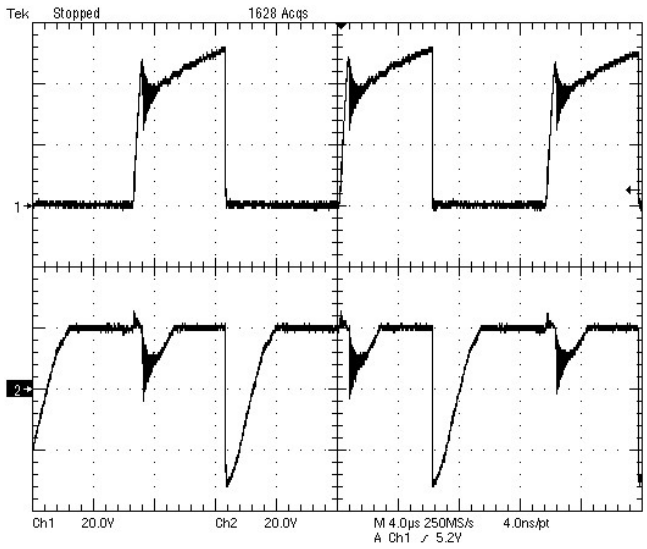

Fig. 11. Snubber waveforms

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VII. CONCLUSIONS

In this paper, a current fed two-inductor boost converter with an unfolder is proposed for the MIC applications for grid interactive PV systems. The two-phase synchronous buck converter is sinusoidally modulated and supplys rectified sinusoidal current to the two-inductor boost cell. Therefore the boost stage is able to generate the rectified sinusoidal voltage on the dc link and this eases the design of the dc-ac inversion stage to an unfolding stage operating at the line frequency.

Some technologies such as the multiphase converter, the synchronous rectifier, the magnetic integration, the non-dissipative snubber, the Silicon Carbide Schottky diodes and the electrically isolated optical MOSFET drivers are employed in the converter to achieve a compact design with an overall high efficiency.

Finally, some experimental waveforms are provided for a 100 W 240 V rms converter. The measurement through the oscilloscope shows that an efficiency of 92% has been achieved for the module integrated PV converter.

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